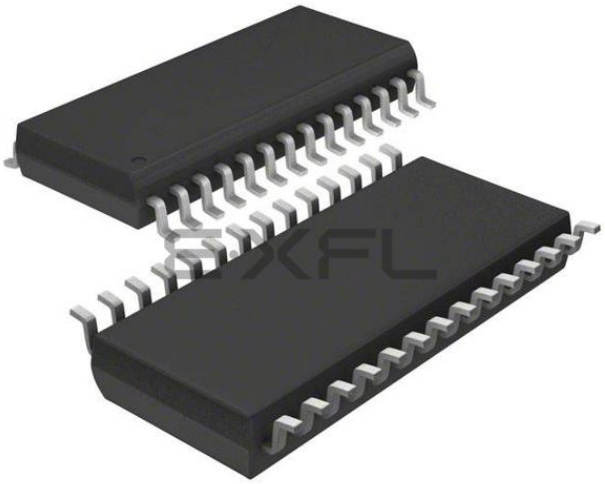

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	M8C
Core Size	8-Bit
Speed	24MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	24
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.25V
Data Converters	A/D 12x14b; D/A 4x9b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	28-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c29466-24pvxit

PSoC Functional Overview

The PSoC family consists of many Programmable System-on-Chip controller devices. These devices are designed to replace multiple traditional microcontroller unit (MCU)-based system components with one, low-cost single-chip programmable device. PSoC devices include configurable blocks of analog and digital logic, as well as programmable interconnects. This architecture allows you to create customized peripheral configurations that match the requirements of each individual application. Additionally, a fast central processing unit (CPU), flash program memory, SRAM data memory, and configurable I/O are included in a range of convenient pinouts and packages.

The PSoC architecture, as illustrated in the Logic Block Diagram on page 1, consists of four main areas: PSoC core, digital system, analog system, and system resources. Configurable global busing allows all of the device resources to be combined into a complete custom system. The PSoC CY8C29x66 family can have up to five I/O ports that connect to the global digital and analog interconnects, providing access to 8 digital blocks and 12 analog blocks.

PSoC Core

The PSoC core is a powerful engine that supports a rich feature set. The core includes a CPU, memory, clocks, and configurable GPIOs.

The M8C CPU core is a powerful processor with speeds up to 24 MHz, providing a 4 million instructions per second (MIPS) 8-bit Harvard-architecture microprocessor. The CPU uses an interrupt controller with 17 vectors, to simplify programming of real-time embedded events. Program execution is timed and protected using the included sleep and watchdog timers (WDT).

Memory uses 32 KB of flash for program storage, 2 KB of SRAM for data storage, and up to 2 KB of EEPROM emulated using the flash. Program flash uses four protection levels on blocks of 64 bytes, allowing customized software information protection (IP).

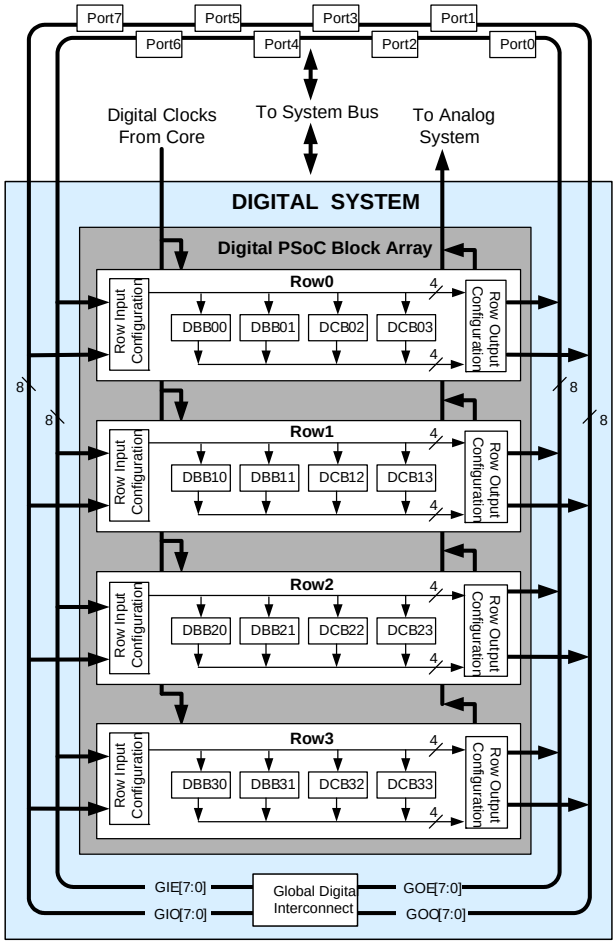
The PSoC device incorporates flexible internal clock generators, including a 24 MHz internal main oscillator (IMO) accurate to 5% [2] over temperature and voltage. The 24 MHz IMO can also be doubled to 48 MHz for use by the digital system. A low-power 32 kHz internal low speed oscillator (ILO) is provided for the sleep timer and WDT. If crystal accuracy is desired, the 32.768 kHz external crystal oscillator (ECO) is available for use as a real-time clock (RTC) and can optionally generate a crystal-accurate 24 MHz system clock using a PLL. The clocks, together with programmable clock dividers (as a system resource), provide the flexibility to integrate almost any timing requirement into the PSoC device.

PSoC GPIOs provide connection to the CPU, and digital and analog resources of the device. Each pin's drive mode may be selected from eight options, allowing great flexibility in external interfacing. Every pin also has the capability to generate a system interrupt on high level, low level, and change from last read.

Digital System

The digital system is composed of 16 digital PSoC blocks. Each block is an 8-bit resource that can be used alone or combined with other blocks to form 8-, 16-, 24-, and 32-bit peripherals, which are called user modules.

Figure 2. Digital System Block Diagram



Note
2. Errata: When the device is operated within 0 °C to 70 °C, the frequency tolerance is reduced to ±2.5%, but if operated at extreme temperature (below 0 °C or above 70 °C), frequency tolerance deviates from ±2.5% to ±5%. For more information, see Errata on page 63.

Digital peripheral configurations include:

- PWMs (8- and 16-bit)
- PWMs with dead band (8- and 16-bit)
- Counters (8- to 32-bit)
- Timers (8- to 32-bit)
- UART 8-bit with selectable parity (up to 2)
- SPI slave and master (up to 2)
- I^2C slave and multi-master (one available as a system resource)
- CRC generator (8- to 32-bit)
- IrDA (up to 2)
- PRS generators (8- to 32-bit)

The digital blocks can be connected to any GPIO through a series of global buses that can route any signal to any pin. The buses also allow for signal multiplexing and for performing logic operations. This configurability frees your designs from the constraints of a fixed peripheral controller.

Digital blocks are provided in rows of four, where the number of blocks varies by PSoC device family. This allows you the optimum choice of system resources for your application. Family resources are shown in the table titled “PSoC Device Characteristics” on page 6.

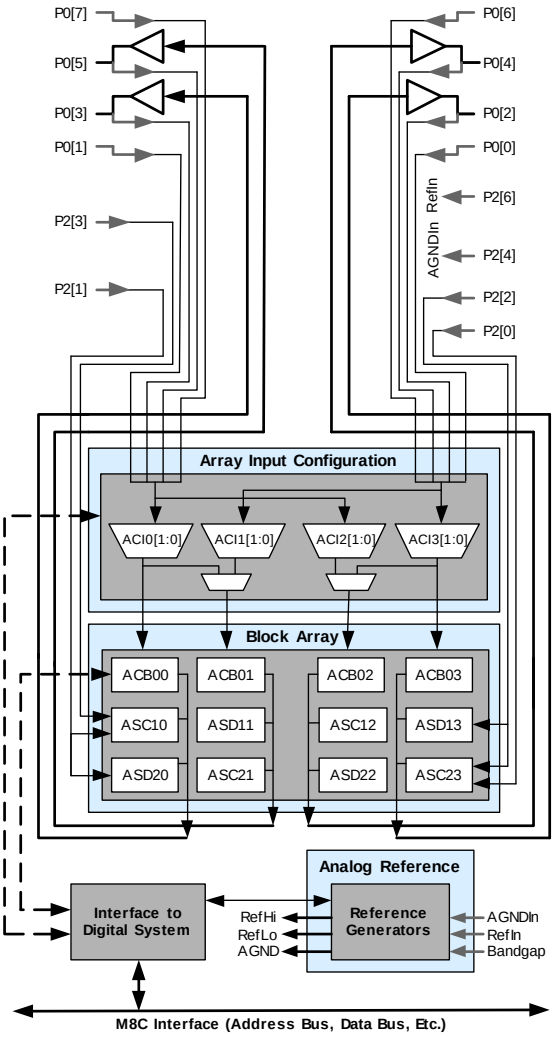
Analog System

The analog system is composed of 12 configurable blocks, each containing an opamp circuit that allows the creation of complex analog signal flows. Analog peripherals are very flexible and can be customized to support specific application requirements. Some of the more common PSoC analog functions (most available as user modules) are:

- ADCs (up to 4, with 6- to 14-bit resolution; selectable as incremental, delta sigma, and SAR)
- Filters (2-, 4-, 6-, and 8-pole band pass, low pass, and notch)
- Amplifiers (up to 4, with selectable gain to 48x)
- Instrumentation amplifiers (up to 2, with selectable gain to 93x)
- Comparators (up to 4, with 16 selectable thresholds)
- DACs (up to 4, with 6-bit to 9-bit resolution)
- Multiplying DACs (up to 4, with 6-bit to 9-bit resolution)
- High current output drivers (four with 30-mA drive as a core resource)
- 1.3-V reference (as a system resource)
- DTMF Dialer
- Modulators
- Correlators
- Peak detectors
- Many other topologies possible

Analog blocks are provided in columns of three, which includes one continuous time (CT) and two switched capacitor (SC) blocks, as shown in Figure 3.

Figure 3. Analog System Block Diagram



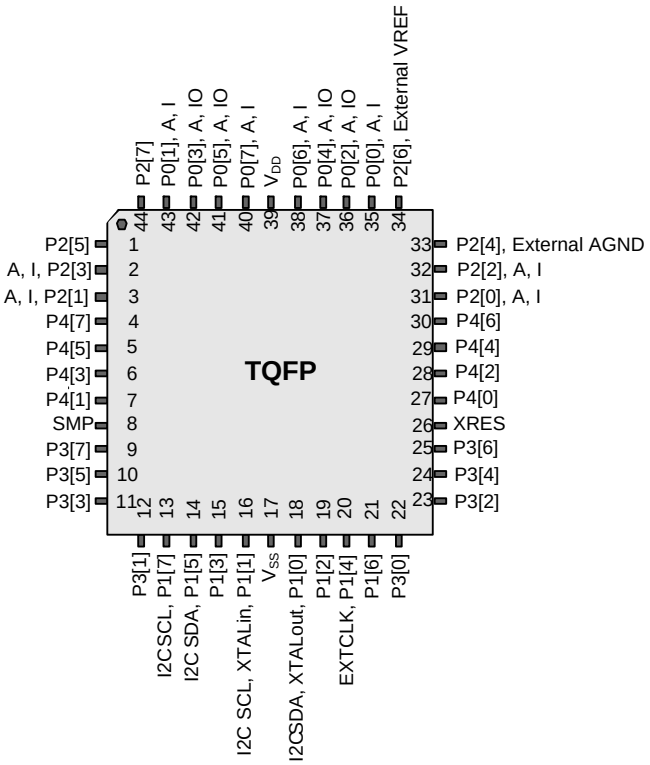
44-Pin Part Pinout

Table 3. 44-Pin Part Pinout (TQFP)

Pin No.	Type		Pin Name	Description
	Digital	Analog		
1	I/O		P2[5]	
2	I/O	I	P2[3]	Direct switched capacitor block input
3	I/O	I	P2[1]	Direct switched capacitor block input
4	I/O		P4[7]	
5	I/O		P4[5]	
6	I/O		P4[3]	
7	I/O		P4[1]	
8	Power		SMP	Switch mode pump (SMP) connection to external components required
9	I/O		P3[7]	
10	I/O		P3[5]	
11	I/O		P3[3]	
12	I/O		P3[1]	
13	I/O		P1[7]	I^2C SCL
14	I/O		P1[5]	I^2C SDA
15	I/O		P1[3]	
16	I/O		P1[1]	Crystal (XTALin), I^2C SCL, ISSP-SCLK[6]
17	Power		V_{SS}	Ground connection
18	I/O		P1[0]	Crystal (XTALout), I^2C SDA, ISSP-SDATA[6]
19	I/O		P1[2]	
20	I/O		P1[4]	Optional EXTCLK
21	I/O		P1[6]	
22	I/O		P3[0]	
23	I/O		P3[2]	
24	I/O		P3[4]	
25	I/O		P3[6]	
26	Input		XRES	Active high external reset with internal pull-down
27	I/O		P4[0]	
28	I/O		P4[2]	
29	I/O		P4[4]	
30	I/O		P4[6]	
31	I/O	I	P2[0]	Direct switched capacitor block input
32	I/O	I	P2[2]	Direct switched capacitor block input
33	I/O		P2[4]	External analog ground (AGND)
34	I/O		P2[6]	External voltage reference (VREF)
35	I/O	I	P0[0]	Analog column mux input
36	I/O	I/O	P0[2]	Analog column mux input and column output
37	I/O	I/O	P0[4]	Analog column mux input and column output
38	I/O	I	P0[6]	Analog column mux input
39	Power		V_{DD}	Supply voltage
40	I/O	I	P0[7]	Analog column mux input
41	I/O	I/O	P0[5]	Analog column mux input and column output
42	I/O	I/O	P0[3]	Analog column mux input and column output
43	I/O	I	P0[1]	Analog column mux input
44	I/O		P2[7]	

LEGEND: A = Analog, I = Input, and O = Output.

Figure 5. CY8C29566 44-Pin PSoC Device



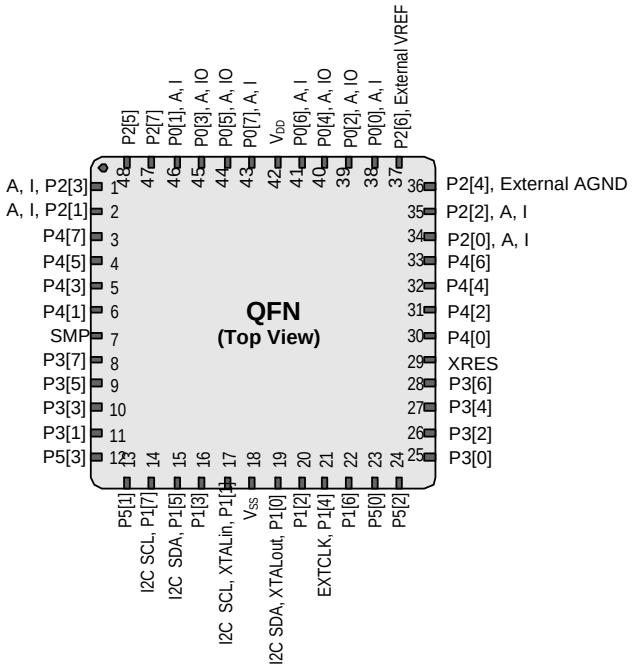
Note
6. These are the ISSP pins, which are not High Z at POR. See the *PSoC Programmable System-on-Chip Technical Reference Manual* for details.

Table 5. 48-Pin Part Pinout (QFN) [9]

Pin No.	Type		Pin Name	Description
	Digital	Analog		
1	I/O	I	P2[3]	Direct switched capacitor block input
2	I/O	I	P2[1]	Direct switched capacitor block input
3	I/O		P4[7]	
4	I/O		P4[5]	
5	I/O		P4[3]	
6	I/O		P4[1]	
7	Power		SMP	Switch mode pump (SMP) connection to external components required
8	I/O		P3[7]	
9	I/O		P3[5]	
10	I/O		P3[3]	
11	I/O		P3[1]	
12	I/O		P5[3]	
13	I/O		P5[1]	
14	I/O		P1[7]	I^2C SCL
15	I/O		P1[5]	I^2C SDA
16	I/O		P1[3]	
17	I/O		P1[1]	Crystal (XTALin), I^2C SCL, ISSP-SCLK[8]
18	Power		V_{SS}	Ground connection
19	I/O		P1[0]	Crystal (XTALout), I^2C SDA, ISSP-SDATA[8]
20	I/O		P1[2]	
21	I/O		P1[4]	Optional EXTCLK
22	I/O		P1[6]	
23	I/O		P5[0]	
24	I/O		P5[2]	
25	I/O		P3[0]	
26	I/O		P3[2]	
27	I/O		P3[4]	
28	I/O		P3[6]	
29	Input		XRES	Active high external reset with internal pull-down
30	I/O		P4[0]	
31	I/O		P4[2]	
32	I/O		P4[4]	
33	I/O		P4[6]	
34	I/O	I	P2[0]	Direct switched capacitor block input
35	I/O	I	P2[2]	Direct switched capacitor block input
36	I/O		P2[4]	External analog ground (AGND)
37	I/O		P2[6]	External voltage reference (VREF)
38	I/O	I	P0[0]	Analog column mux input
39	I/O	I/O	P0[2]	Analog column mux input and column output
40	I/O	I/O	P0[4]	Analog column mux input and column output
41	I/O	I	P0[6]	Analog column mux input
42	Power		V_{DD}	Supply voltage
43	I/O	I	P0[7]	Analog column mux input
44	I/O	I/O	P0[5]	Analog column mux input and column output
45	I/O	I/O	P0[3]	Analog column mux input and column output
46	I/O	I	P0[1]	Analog column mux input
47	I/O		P2[7]	
48	I/O		P2[5]	

LEGEND: A = Analog, I = Input, and O = Output.

Figure 7. CY8C29666 48-Pin PSoC Device



Notes
8. These are the ISSP pins, which are not High Z at POR. See the *PSoC Programmable System-on-Chip Technical Reference Manual* for details.
9. The QFN package has a center pad that must be connected to ground (V_{SS}).

Register Reference

This section lists the registers of the CY8C29x66 PSoC device. For detailed register information, refer to the *PSoC Programmable System-on-Chip Technical Reference Manual*.

Register Conventions

The register conventions specific to this section are listed in Table 8.

Table 8. Register Conventions

Convention	Description
R	Read register or bit(s)
W	Write register or bit(s)
L	Logical register or bit(s)
C	Clearable register or bit(s)
#	Access is bit specific

Register Mapping Tables

The PSoC device has a total register address space of 512 bytes. The register space is referred to as I/O space and is divided into two banks. The XOI bit in the flag register (CPU_F) determines which bank the user is currently in. When the XOI bit is set the user is in Bank 1.

Note In the register mapping tables, blank fields are reserved and should not be accessed.

Table 16. 3.3-V DC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Unit	Notes
V_{OSOA}	Input offset voltage (absolute value) Power = Low, Opamp bias = Low Power = Low, Opamp bias = High Power = Medium, Opamp bias = Low Power = Medium, Opamp bias = High Power = High, Opamp bias = Low Power = High, Opamp bias = High	 – – – – – –	 1.4 1.4 1.4 1.4 1.4 –	 10 10 10 10 10 –	 mV mV mV mV mV mV	Power = High, Opamp bias = High setting is not allowed for 3.3 V V_{DD} operation.
TCV_{OSOA}	Average input offset voltage drift	–	7	40	µV/°C	
I_{EBOA}	Input leakage current (port 0 analog pins)	–	200	–	pA	Gross tested to 1 µA.
C_{INOA}	Input capacitance (port 0 analog pins)	–	4.5	9.5	pF	Package and pin dependent. Temp = 25 °C
V_{CMOA}	Common mode voltage range	0	–	V_{DD}	V	The common-mode input voltage range is measured through an analog output buffer. The specification includes the limitations imposed by the characteristics of the analog output buffer.
$CMRR_{OA}$	Common mode rejection ratio	60	–	–	dB	
G_{OLOA}	Open loop gain	80	–	–	dB	
$V_{OHIGHOA}$	High output voltage swing (internal signals)	V_{DD} – 0.01	–	–	V	
V_{OLOWOA}	Low output voltage swing (internal signals)	–	–	0.01	V	
I_{SOA}	Supply current (including associated AGND buffer) Power = Low, Opamp bias = Low Power = Low, Opamp bias = High Power = Medium, Opamp bias = Low Power = Medium, Opamp bias = High Power = High, Opamp bias = Low Power = High, Opamp bias = High	 – – – – – –	 150 300 600 1200 2400 –	 200 400 800 1600 3200 –	 µA µA µA µA µA µA	Power = High, Opamp bias = High setting is not allowed for 3.3 V V_{DD} operation.
$PSRR_{OA}$	Supply voltage rejection ratio	54	80	–	dB	$V_{SS} \le V_{IN} \le (V_{DD} – 2.25)$ or $(V_{DD} – 1.25\ V) \le V_{IN} \le V_{DD}$

DC Low-Power Comparator Specifications

Table 17 lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V at 25 °C and are for design guidance only.

Table 17. DC Low-Power Comparator Specifications

Symbol	Description	Min	Typ	Max	Unit
V_{REFLPC}	Low-power comparator (LPC) reference voltage range	0.2	–	V_{DD} – 1	V
I_{SLPC}	LPC supply current	–	10	40	µA
V_{OSLPC}	LPC voltage offset	–	2.5	30	mV

Table 21. 5-V DC Analog Reference Specifications (continued)

Reference ARF_CR[5:3]	Reference Power Settings	Symbol	Reference	Description	Min	Typ	Max	Unit
0b001	RefPower = High Opamp bias = High	V_{REFHI}	Ref High	P2[4] + P2[6] ($P2[4] = V_{DD}/2$, P2[6] = 1.3 V)	P2[4] + P2[6] – 0.085	P2[4] + P2[6] – 0.016	P2[4] + P2[6] + 0.044	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4] – P2[6] ($P2[4] = V_{DD}/2$, P2[6] = 1.3 V)	P2[4] – P2[6] – 0.022	P2[4] – P2[6] + 0.010	P2[4] – P2[6] + 0.055	V
	RefPower = High Opamp bias = Low	V_{REFHI}	Ref High	P2[4] + P2[6] ($P2[4] = V_{DD}/2$, P2[6] = 1.3 V)	P2[4] + P2[6] – 0.077	P2[4] + P2[6] – 0.010	P2[4] + P2[6] + 0.051	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4] – P2[6] ($P2[4] = V_{DD}/2$, P2[6] = 1.3 V)	P2[4] – P2[6] – 0.022	P2[4] – P2[6] + 0.005	P2[4] – P2[6] + 0.039	V
	RefPower = Med Opamp bias = High	V_{REFHI}	Ref High	P2[4] + P2[6] ($P2[4] = V_{DD}/2$, P2[6] = 1.3 V)	P2[4] + P2[6] – 0.070	P2[4] + P2[6] – 0.010	P2[4] + P2[6] + 0.050	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4] – P2[6] ($P2[4] = V_{DD}/2$, P2[6] = 1.3 V)	P2[4] – P2[6] – 0.022	P2[4] – P2[6] + 0.005	P2[4] – P2[6] + 0.039	V
	RefPower = Med Opamp bias = Low	V_{REFHI}	Ref High	P2[4] + P2[6] ($P2[4] = V_{DD}/2$, P2[6] = 1.3 V)	P2[4] + P2[6] – 0.070	P2[4] + P2[6] – 0.007	P2[4] + P2[6] + 0.054	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4] – P2[6] ($P2[4] = V_{DD}/2$, P2[6] = 1.3 V)	P2[4] – P2[6] – 0.022	P2[4] – P2[6] + 0.002	P2[4] – P2[6] + 0.032	V
0b010	RefPower = High Opamp bias = High	V_{REFHI}	Ref High	V_{DD}	V_{DD} – 0.037	V_{DD} – 0.009	V_{DD}	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.061	$V_{DD}/2$ – 0.006	$V_{DD}/2$ + 0.047	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.007	V_{SS} + 0.028	V
	RefPower = High Opamp bias = Low	V_{REFHI}	Ref High	V_{DD}	V_{DD} – 0.039	V_{DD} – 0.006	V_{DD}	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.049	$V_{DD}/2$ – 0.005	$V_{DD}/2$ + 0.036	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.005	V_{SS} + 0.019	V
	RefPower = Med Opamp bias = High	V_{REFHI}	Ref High	V_{DD}	V_{DD} – 0.037	V_{DD} – 0.007	V_{DD}	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.054	$V_{DD}/2$ – 0.005	$V_{DD}/2$ + 0.041	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.006	V_{SS} + 0.024	V
	RefPower = Med Opamp bias = Low	V_{REFHI}	Ref High	V_{DD}	V_{DD} – 0.042	V_{DD} – 0.005	V_{DD}	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.046	$V_{DD}/2$ – 0.004	$V_{DD}/2$ + 0.034	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.004	V_{SS} + 0.017	V

Table 21. 5-V DC Analog Reference Specifications (continued)

Reference ARF_CR[5:3]	Reference Power Settings	Symbol	Reference	Description	Min	Typ	Max	Unit
0b011	RefPower = High Opamp bias = High	V_{REFHI}	Ref High	3 × Bandgap	3.788	3.891	3.986	V
		V_{AGND}	AGND	2 × Bandgap	2.500	2.604	2.699	V
		V_{REFLO}	Ref Low	Bandgap	1.257	1.306	1.359	V
	RefPower = High Opamp bias = Low	V_{REFHI}	Ref High	3 × Bandgap	3.792	3.893	3.982	V
		V_{AGND}	AGND	2 × Bandgap	2.518	2.602	2.692	V
		V_{REFLO}	Ref Low	Bandgap	1.256	1.302	1.354	V
	RefPower = Med Opamp bias = High	V_{REFHI}	Ref High	3 × Bandgap	3.795	3.894	3.993	V
		V_{AGND}	AGND	2 × Bandgap	2.516	2.603	2.698	V
		V_{REFLO}	Ref Low	Bandgap	1.256	1.303	1.353	V
	RefPower = Med Opamp bias = Low	V_{REFHI}	Ref High	3 × Bandgap	3.792	3.895	3.986	V
		V_{AGND}	AGND	2 × Bandgap	2.522	2.602	2.685	V
		V_{REFLO}	Ref Low	Bandgap	1.255	1.301	1.350	V
0b100	RefPower = High Opamp bias = High	V_{REFHI}	Ref High	2 × Bandgap + P2[6] (P2[6] = 1.3 V)	2.495 + P2[6]	2.586 + P2[6]	2.657 + P2[6]	V
		V_{AGND}	AGND	2 × Bandgap	2.502	2.604	2.719	V
		V_{REFLO}	Ref Low	2 × Bandgap – P2[6] (P2[6] = 1.3 V)	2.531 – P2[6]	2.611 – P2[6]	2.681 – P2[6]	V
	RefPower = High Opamp bias = Low	V_{REFHI}	Ref High	2 × Bandgap + P2[6] (P2[6] = 1.3 V)	2.500 + P2[6]	2.591 + P2[6]	2.662 + P2[6]	V
		V_{AGND}	AGND	2 × Bandgap	2.519	2.602	2.693	V
		V_{REFLO}	Ref Low	2 × Bandgap – P2[6] (P2[6] = 1.3 V)	2.530 – P2[6]	2.605 – P2[6]	2.666 – P2[6]	V
	RefPower = Med Opamp bias = High	V_{REFHI}	Ref High	2 × Bandgap + P2[6] (P2[6] = 1.3 V)	2.503 + P2[6]	2.592 + P2[6]	2.662 + P2[6]	V
		V_{AGND}	AGND	2 × Bandgap	2.517	2.603	2.698	V
		V_{REFLO}	Ref Low	2 × Bandgap – P2[6] (P2[6] = 1.3 V)	2.529 – P2[6]	2.606 – P2[6]	2.665 – P2[6]	V
	RefPower = Med Opamp bias = Low	V_{REFHI}	Ref High	2 × Bandgap + P2[6] (P2[6] = 1.3 V)	2.505 + P2[6]	2.594 + P2[6]	2.665 + P2[6]	V
		V_{AGND}	AGND	2 × Bandgap	2.525	2.602	2.685	V
		V_{REFLO}	Ref Low	2 × Bandgap – P2[6] (P2[6] = 1.3 V)	2.528 – P2[6]	2.603 – P2[6]	2.661 – P2[6]	V

Table 22. 3.3-V DC Analog Reference Specifications (continued)

Reference ARF_CR[5:3]	Reference Power Settings	Symbol	Reference	Description	Min	Typ	Max	Unit
0b010	RefPower = High Opamp bias = High	V_{REFHI}	Ref High	V_{DD}	V_{DD} – 0.06	V_{DD} – 0.010	V_{DD}	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.05	$V_{DD}/2$ – 0.002	$V_{DD}/2$ + 0.040	V
		V_{REFLO}	Ref Low	Vss	Vss	Vss + 0.009	Vss + 0.056	V
	RefPower = High Opamp bias = Low	V_{REFHI}	Ref High	V_{DD}	V_{DD} – 0.060	V_{DD} – 0.006	V_{DD}	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.028	$V_{DD}/2$ – 0.001	$V_{DD}/2$ + 0.025	V
		V_{REFLO}	Ref Low	Vss	Vss	Vss + 0.005	Vss + 0.034	V
	RefPower = Med Opamp bias = High	V_{REFHI}	Ref High	V_{DD}	V_{DD} – 0.058	V_{DD} – 0.008	V_{DD}	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.037	$V_{DD}/2$ – 0.002	$V_{DD}/2$ + 0.033	V
		V_{REFLO}	Ref Low	Vss	Vss	Vss + 0.007	Vss + 0.046	V
	RefPower = Med Opamp bias = Low	V_{REFHI}	Ref High	V_{DD}	V_{DD} – 0.057	V_{DD} – 0.006	V_{DD}	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.025	$V_{DD}/2$ – 0.001	$V_{DD}/2$ + 0.022	V
		V_{REFLO}	Ref Low	Vss	Vss	Vss + 0.004	Vss + 0.030	V
0b011	All power settings. Not allowed for 3.3 V	–	–	–	–	–	–	–
0b100	All power settings. Not allowed for 3.3 V	–	–	–	–	–	–	–

DC POR, SMP, and LVD Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 26. DC POR, SMP, and LVD Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
	V_{DD} value for PPOR trip (positive ramp)					
V_{PPOR0R}	PORLEV[1:0] = 00b		2.91		V	
V_{PPOR1R}	PORLEV[1:0] = 01b	–	4.39	–	V	
V_{PPOR2R}	PORLEV[1:0] = 10b		4.55		V	
	V_{DD} value for PPOR trip (negative ramp)					
V_{PPOR0}	PORLEV[1:0] = 00b		2.82		V	
V_{PPOR1}	PORLEV[1:0] = 01b	–	4.39	–	V	
V_{PPOR2}	PORLEV[1:0] = 10b		4.55		V	
	PPOR hysteresis					
V_{PH0}	PORLEV[1:0] = 00b	–	92	–	mV	
V_{PH1}	PORLEV[1:0] = 01b	–	0	–	mV	
V_{PH2}	PORLEV[1:0] = 10b	–	0	–	mV	
	V_{DD} value for LVD trip					
V_{LVD0}	VM[2:0] = 000b	2.86	2.92	2.98[16]	V	
V_{LVD1}	VM[2:0] = 001b	2.96	3.02	3.08	V	
V_{LVD2}	VM[2:0] = 010b	3.07	3.13	3.20	V	
V_{LVD3}	VM[2:0] = 011b	3.92	4.00	4.08	V	
V_{LVD4}	VM[2:0] = 100b	4.39	4.48	4.57	V	
V_{LVD5}	VM[2:0] = 101b	4.55	4.64	4.74[17]	V	
V_{LVD6}	VM[2:0] = 110b	4.63	4.73	4.82	V	
V_{LVD7}	VM[2:0] = 111b	4.72	4.81	4.91	V	
	V_{DD} value for SMP trip					
V_{PUMP0}	VM[2:0] = 000b	2.96	3.02	3.08	V	
V_{PUMP1}	VM[2:0] = 001b	3.03	3.10	3.16	V	
V_{PUMP2}	VM[2:0] = 010b	3.18	3.25	3.32	V	
V_{PUMP3}	VM[2:0] = 011b	4.11	4.19	4.28	V	
V_{PUMP4}	VM[2:0] = 100b	4.55	4.64	4.74	V	
V_{PUMP5}	VM[2:0] = 101b	4.63	4.73	4.82	V	
V_{PUMP6}	VM[2:0] = 110b	4.72	4.82	4.91	V	
V_{PUMP7}	VM[2:0] = 111b	4.90	5.00	5.10	V	

Notes
16. Always greater than 50 mV above PPOR (PORLEV = 00) for falling supply.
17. Always greater than 50 mV above PPOR (PORLEV = 10) for falling supply.

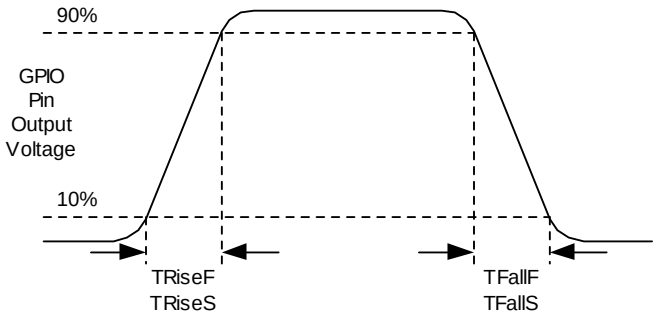
AC General Purpose I/O Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 30. AC GPIO Specifications

Symbol	Description	Min	Typ	Max	Unit	Notes
F_{GPIO}	GPIO operating frequency	0	–	12.3	MHz	Normal strong mode
tRiseF	Rise time, normal strong mode, Cload = 50 pF	3	–	18	ns	V_{DD} = 4.75 to 5.25 V, 10% to 90%
tFallF	Fall time, normal strong mode, Cload = 50 pF	2	–	18	ns	V_{DD} = 4.75 to 5.25 V, 10% to 90%
tRiseS	Rise time, slow strong mode, Cload = 50 pF	10	27	–	ns	V_{DD} = 3 to 5.25 V, 10% to 90%
tFallS	Fall time, slow strong mode, Cload = 50 pF	10	22	–	ns	V_{DD} = 3 to 5.25 V, 10% to 90%

Figure 16. GPIO Timing Diagram



AC Operational Amplifier Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Settling times, slew rates, and gain bandwidth are based on the analog continuous time PSoC block.

Power = High and Opamp bias = High is not supported at 3.3 V.

Table 31. 5-V AC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Unit
t_{ROA}	Rising settling time to 0.1% for a 1 V step (10 pF load, unity gain) Power = Low, Opamp bias = Low Power = Medium, Opamp bias = High Power = High, Opamp bias = High	 – – –	 – – –	 3.9 0.72 0.62	 µs µs µs
t_{SOA}	Falling settling time to 0.1% for a 1 V step (10 pF load, unity gain) Power = Low, Opamp bias = Low Power = Medium, Opamp bias = High Power = High, Opamp bias = High	 – – –	 – – –	 5.9 0.92 0.72	 µs µs µs
SR_{ROA}	Rising slew rate (20% to 80%) of a 1 V step (10 pF load, unity gain) Power = Low, Opamp bias = Low Power = Medium, Opamp bias = High Power = High, Opamp bias = High	 0.15 1.7 6.5	 – – –	 – – –	 V/µs V/µs V/µs
SR_{FOA}	Falling slew rate (20% to 80%) of a 1 V step (10 pF load, unity gain) Power = Low, Opamp bias = Low Power = Medium, Opamp bias = High Power = High, Opamp bias = High	 0.01 0.5 4.0	 – – –	 – – –	 V/µs V/µs V/µs
BW_{OA}	Gain bandwidth product Power = Low, Opamp bias = Low Power = Medium, Opamp bias = High Power = High, Opamp bias = High	 0.75 3.1 5.4	 – – –	 – – –	 MHz MHz MHz
E_{NOA}	Noise at 1 kHz (Power = Medium, Opamp bias = High)	–	100	–	nV/rt-Hz

Packaging Information

This section illustrates the packaging specifications for the CY8C29x66 PSoC device, along with the thermal impedances for each package and the typical package capacitance on crystal pins.

Important Note Emulation tools may require a larger area on the target PCB than the chip's footprint. For a detailed description of the emulation tools' dimensions, refer to the emulator pod drawings at http://www.cypress.com.

Packaging Dimensions

Figure 20. 28-pin PDIP (300 Mils) Package Outline, 51-85014

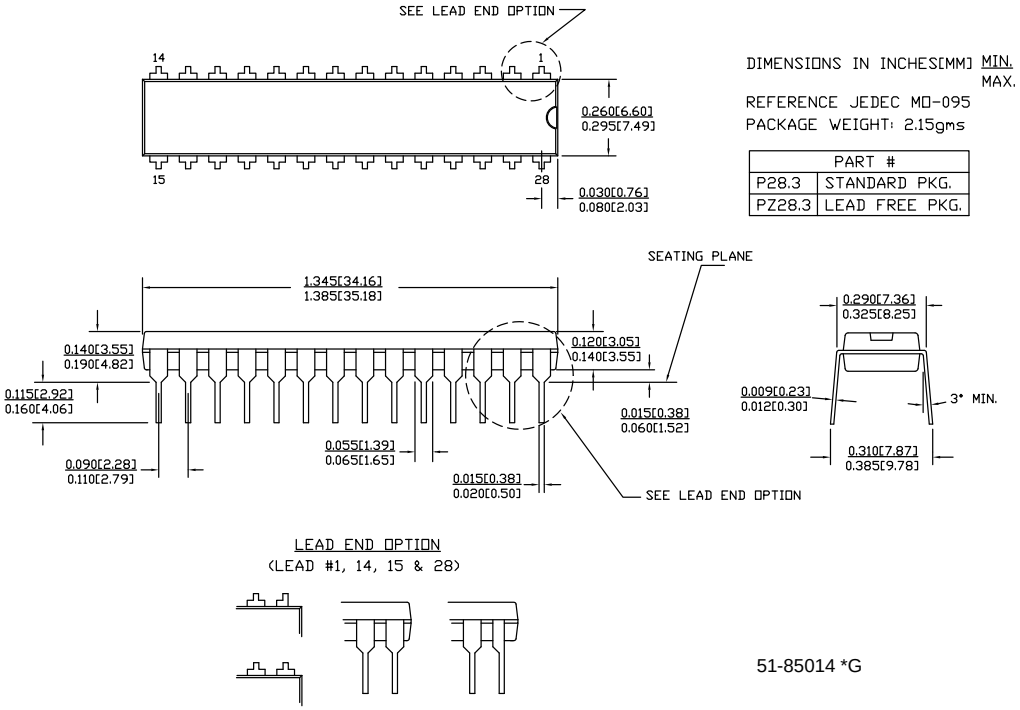


Figure 23. 44-pin TQFP (10 × 10 × 1.4 mm) Package Outline, 51-85064

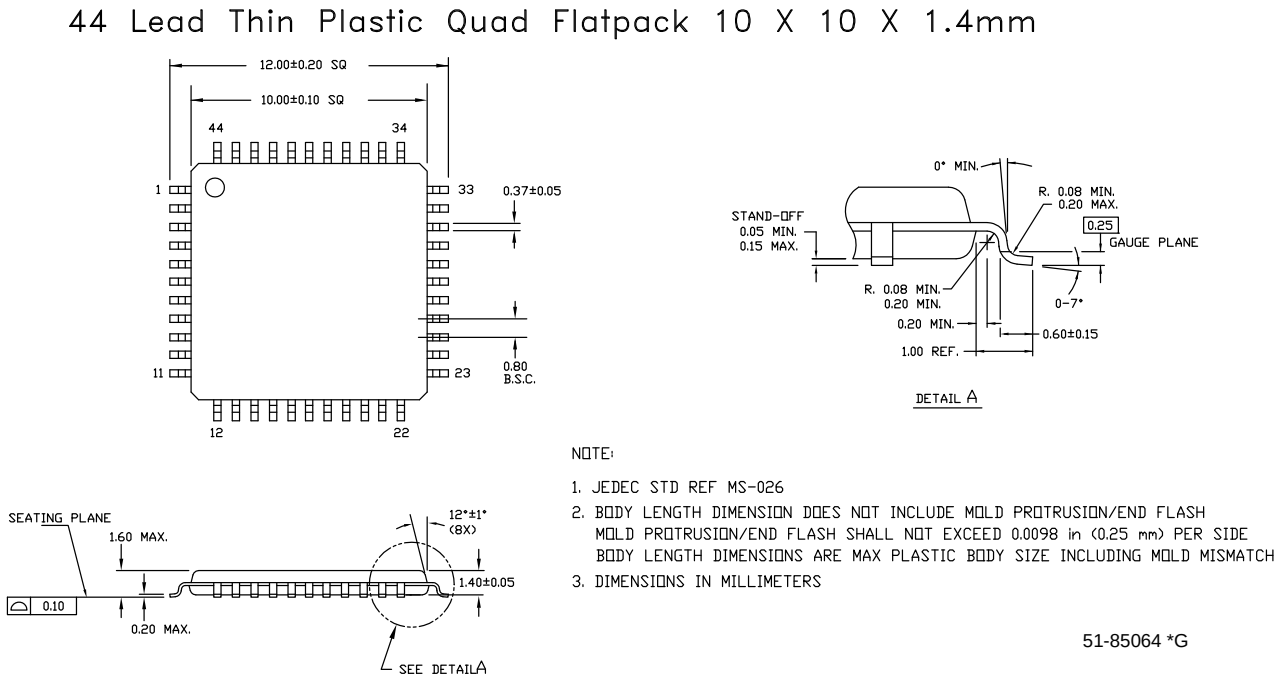


Figure 24. 48-pin SSOP (300 Mils) Package Outline, 51-85061

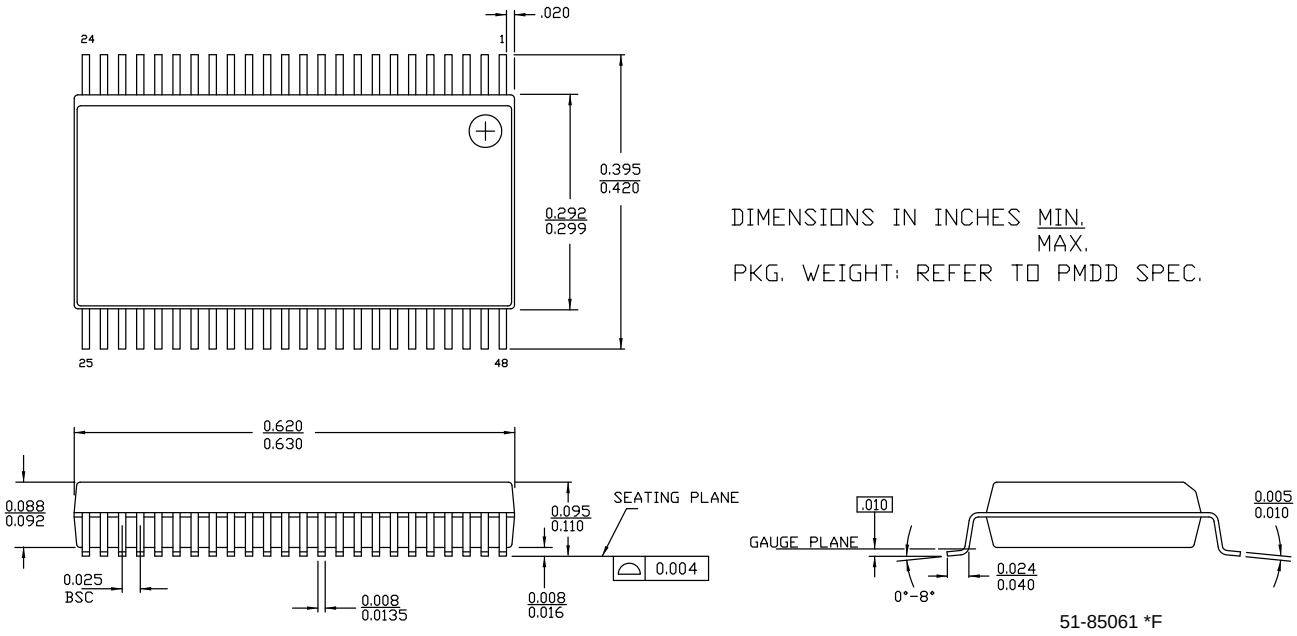


Figure 25. 48-pin QFN (7 × 7 × 1.0 mm) 5.1 × 5.1 E-Pad (Sawn) Package Outline, 001-13191

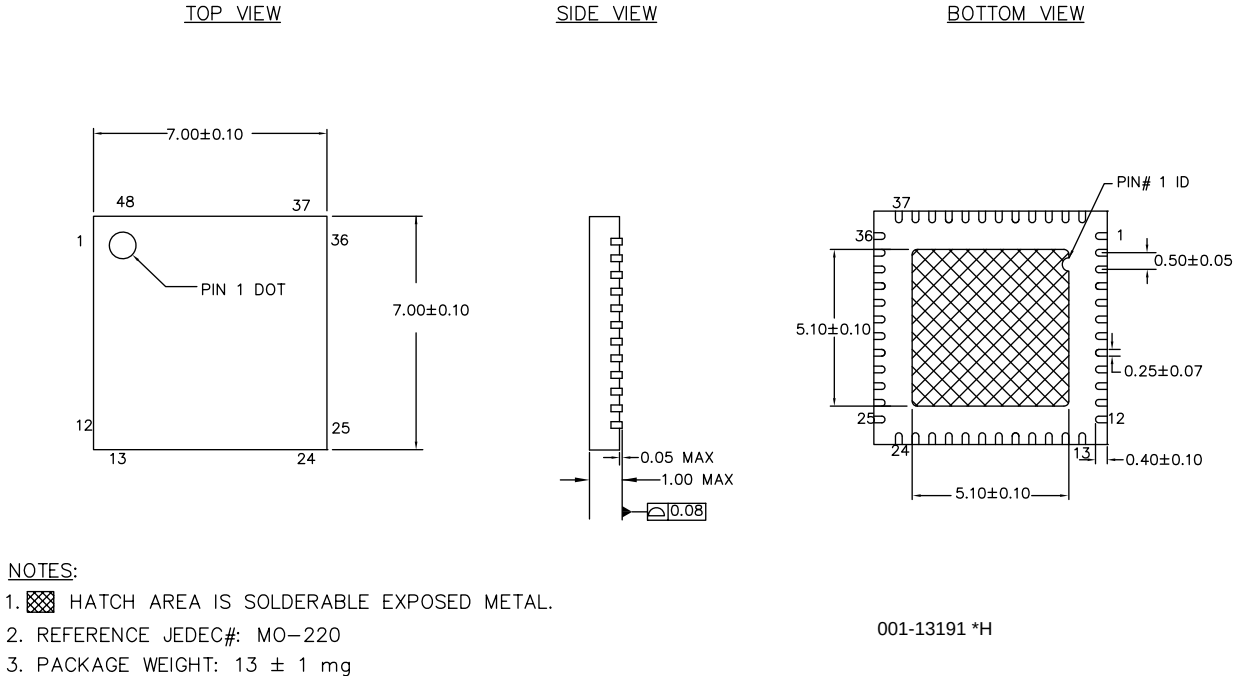
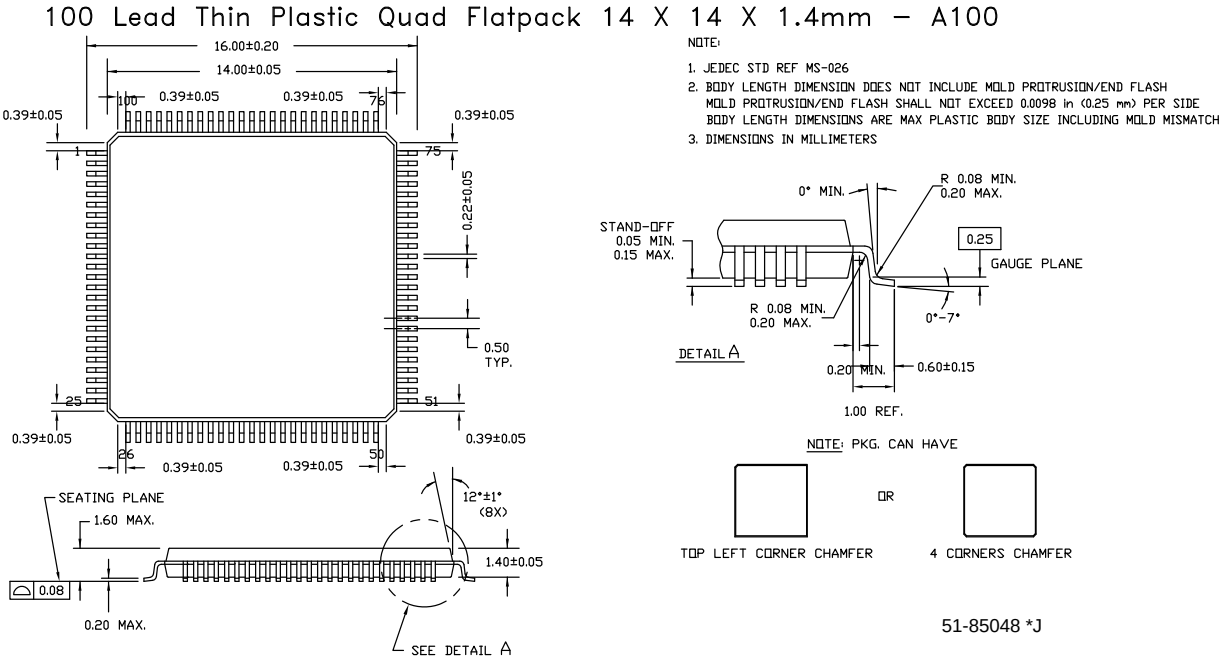


Figure 26. 100-pin TQFP (14 × 14 × 1.4 mm) Package Outline, 51-85048



Important Note For information on the preferred dimensions for mounting the QFN packages, see the application note *Design Guidelines for Cypress Quad Flat No Extended Lead (QFN) Packaged Devices – AN72845* available at http://www.cypress.com.

Important Note Pinned vias for thermal conduction are not required for the low-power PSoC device.

Thermal Impedances

Table 41. Thermal Impedances per Package

Package	Typical θ_{JA}[30]
28-pin PDIP	69 °C/W
28-pin SSOP	94 °C/W
28-pin SOIC	67 °C/W
44-pin TQFP	60 °C/W
48-pin SSOP	69 °C/W
48-pin QFN[31]	28 °C/W
100-pin TQFP	50 °C/W

Capacitance on Crystal Pins

Table 42. Typical Package Capacitance on Crystal Pins

Package	Package Capacitance
28-pin PDIP	3.5 pF
28-pin SSOP	2.8 pF
28-pin SOIC	2.7 pF
44-pin TQFP	2.6 pF
48-pin SSOP	3.3 pF
48-pin QFN	1.8 pF
100-pin TQFP	3.1 pF

Solder Reflow Specifications

Table 43 shows the solder reflow temperature limits that must not be exceeded.

Table 43. Solder Reflow Specifications

Package	Maximum Peak Temperature (T_C)	Maximum Time above T_C – 5 °C
28-pin PDIP	260 °C	30 seconds
28-pin SSOP	260 °C	30 seconds
28-pin SOIC	260 °C	30 seconds
44-pin TQFP	260 °C	30 seconds
48-pin SSOP	260 °C	30 seconds
48-pin QFN	260 °C	30 seconds
100-pin TQFP	260 °C	30 seconds

Notes
30. $T_J = T_A + POWER \times \theta_{JA}$.
31. To achieve the thermal impedance specified for the QFN package, refer to the application note *Design Guidelines for Cypress Quad Flat No Extended Lead (QFN) Packaged Devices – AN72845* available at http://www.cypress.com.

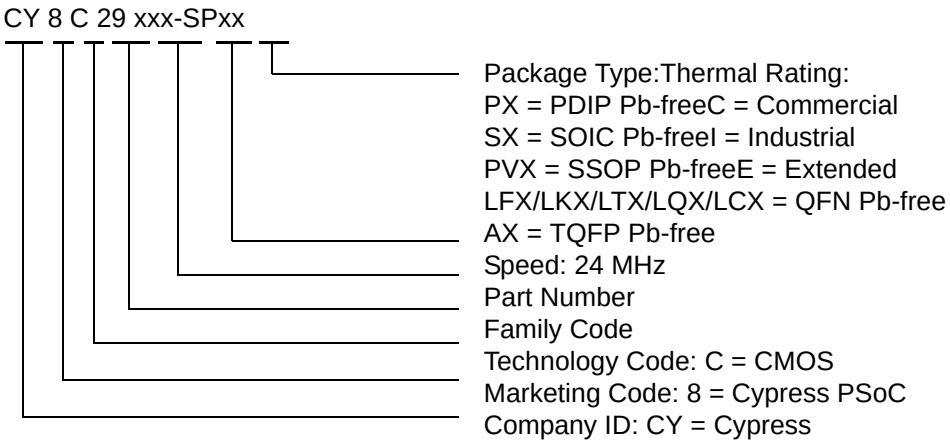
Ordering Information

The following table lists the CY8C29x66 PSoC device's key package features and ordering codes.

Package	Ordering Code	Flash (KB)	RAM (KB)	Switch Mode Pump	Temperature Range	Digital PSoC Blocks	Analog PSoC Blocks	Digital I/O Pins	Analog Inputs	Analog Outputs	XRES Pin
28-pin (300-mil) DIP	CY8C29466-24PXI	32	2	Yes	–40 °C to +85 °C	16	12	24	12	4	Yes
28-pin (210-mil) SSOP	CY8C29466-24PVXI	32	2	Yes	–40 °C to +85 °C	16	12	24	12	4	Yes
28-pin (210-mil) SSOP (Tape and Reel)	CY8C29466-24PVXIT	32	2	Yes	–40 °C to +85 °C	16	12	24	12	4	Yes
28-pin (300-mil) SOIC	CY8C29466-24SXI	32	2	Yes	–40 °C to +85 °C	16	12	24	12	4	Yes
28-pin (300-mil) SOIC (Tape and Reel)	CY8C29466-24SXIT	32	2	Yes	–40 °C to +85 °C	16	12	24	12	4	Yes
44-pin TQFP	CY8C29566-24AXI	32	2	Yes	–40 °C to +85 °C	16	12	40	12	4	Yes
44-pin TQFP (Tape and Reel)	CY8C29566-24AXIT	32	2	Yes	–40 °C to +85 °C	16	12	40	12	4	Yes
48-pin (300-mil) SSOP	CY8C29666-24PVXI	32	2	Yes	–40 °C to +85 °C	16	12	44	12	4	Yes
48-pin (300-mil) SSOP (Tape and Reel)	CY8C29666-24PVXIT	32	2	Yes	–40 °C to +85 °C	16	12	44	12	4	Yes
100-Pin TQFP	CY8C29866-24AXI	32	2	Yes	–40 °C to +85 °C	16	12	64	12	4	Yes
100-Pin OCD TQFP[35]	CY8C29000-24AXI	32	2	Yes	–40 °C to +85 °C	16	12	64	12	4	Yes
48-Pin (7 × 7 × 1.0 mm) QFN (Sawn)	CY8C29666-24LTXI	32	2	Yes	–40 °C to +85 °C	16	12	44	12	4	Yes
48-Pin (7 × 7 × 1.0 mm) QFN (Sawn)	CY8C29666-24LTXIT	32	2	Yes	–40 °C to +85 °C	16	12	44	12	4	Yes

Note For Die sales information, contact a local Cypress sales office or field applications engineer (FAE).

Ordering Code Definitions



Note
35. This part may be used for in-circuit debugging. It is NOT available for production.

Glossary (continued)

bias	1. A systematic deviation of a value from a reference value. 2. The amount by which the average of a set of values departs from a reference value. 3. The electrical, mechanical, magnetic, or other force (field) applied to a device to establish a reference level to operate the device.
block	1. A functional unit that performs a single function, such as an oscillator. 2. A functional unit that may be configured to perform one of several functions, such as a digital PSoC block or an analog PSoC block.
buffer	1. A storage area for data that is used to compensate for a speed difference, when transferring data from one device to another. Usually refers to an area reserved for IO operations, into which data is read, or from which data is written. 2. A portion of memory set aside to store data, often before it is sent to an external device or as it is received from an external device. 3. An amplifier used to lower the output impedance of a system.
bus	1. A named connection of nets. Bundling nets together in a bus makes it easier to route nets with similar routing patterns. 2. A set of signals performing a common function and carrying similar data. Typically represented using vector notation; for example, address[7:0]. 3. One or more conductors that serve as a common connection for a group of related devices.
clock	The device that generates a periodic signal with a fixed frequency and duty cycle. A clock is sometimes used to synchronize different logic blocks.
comparator	An electronic circuit that produces an output voltage or current whenever two input levels simultaneously satisfy predetermined amplitude requirements.
compiler	A program that translates a high level language, such as C, into machine language.
configuration space	In PSoC devices, the register space accessed when the XIO bit, in the CPU_F register, is set to ‘1’.
crystal oscillator	An oscillator in which the frequency is controlled by a piezoelectric crystal. Typically a piezoelectric crystal is less sensitive to ambient temperature than other circuit components.
cyclic redundancy check (CRC)	A calculation used to detect errors in data communications, typically performed using a linear feedback shift register. Similar calculations may be used for a variety of other purposes such as data compression.
data bus	A bi-directional set of signals used by a computer to convey information from a memory location to the central processing unit and vice versa. More generally, a set of signals used to convey data between digital functions.
debugger	A hardware and software system that allows you to analyze the operation of the system under development. A debugger usually allows the developer to step through the firmware one step at a time, set break points, and analyze memory.
dead band	A period of time when neither of two or more signals are in their active state or in transition.
digital blocks	The 8-bit logic blocks that can act as a counter, timer, serial receiver, serial transmitter, CRC generator, pseudo-random number generator, or SPI.
digital-to-analog (DAC)	A device that changes a digital signal to an analog signal of corresponding magnitude. The analog-to-digital (ADC) converter performs the reverse operation.

Glossary (continued)

shift register	A memory storage device that sequentially shifts a word either left or right to output a stream of serial data.
slave device	A device that allows another device to control the timing for data exchanges between two devices. Or when devices are cascaded in width, the slave device is the one that allows another device to control the timing of data exchanges between the cascaded devices and an external interface. The controlling device is called the master device.
SRAM	An acronym for static random access memory. A memory device where you can store and retrieve data at a high rate of speed. The term static is used because, after a value is loaded into an SRAM cell, it remains unchanged until it is explicitly altered or until power is removed from the device.
SROM	An acronym for supervisory read only memory. The SROM holds code that is used to boot the device, calibrate circuitry, and perform Flash operations. The functions of the SROM may be accessed in normal user code, operating from Flash.
stop bit	A signal following a character or block that prepares the receiving device to receive the next character or block.
synchronous	1. A signal whose data is not acknowledged or acted upon until the next active edge of a clock signal. 2. A system whose operation is synchronized by a clock signal.
tri-state	A function whose output can adopt three states: 0, 1, and Z (high-impedance). The function does not drive any value in the Z state and, in many respects, may be considered to be disconnected from the rest of the circuit, allowing another output to drive the same net.
UART	A UART or universal asynchronous receiver-transmitter translates between parallel bits of data and serial bits.
user modules	Pre-build, pre-tested hardware/firmware peripheral functions that take care of managing and configuring the lower level Analog and Digital PSoC Blocks. User Modules also provide high level ***API (Application Programming Interface)*** for the peripheral function.
user space	The bank 0 space of the register map. The registers in this bank are more likely to be modified during normal program execution and not just during initialization. Registers in bank 1 are most likely to be modified only during the initialization phase of the program.
V_{DD}	A name for a power net meaning “voltage drain.” The most positive power supply signal. Usually 5 V or 3.3 V.
V_{SS}	A name for a power net meaning “voltage source.” The most negative power supply signal.
watchdog timer	A timer that must be serviced periodically. If it is not serviced, the CPU resets after a specified period of time.

Errata

This section describes the errata for the PSoC Programmable System-on-Chip, CY8C29xxx family of devices. Details include errata trigger conditions, scope of impact, available workaround, and silicon revision applicability. Contact your local Cypress Sales Representative if you have questions.

Part Numbers Affected

Part Number	Ordering Information
CY8C29xxx	CY8C29466-24PXI
	CY8C29466-24PVXI
	CY8C29466-24PVXIT
	CY8C29466-24SXI
	CY8C29466-24SXIT
	CY8C29566-24AXI
	CY8C29566-24AXIT
	CY8C29666-24PVXI
	CY8C29666-24PVXIT
	CY8C29666-24LFXI
	CY8C29866-24AXI
	CY8C29000-24AXI

Qualification Status

Product Status: In Production

Errata Summary

The following table defines the errata applicability to available CY8C29xxx family devices.

Items	Part Number	Silicon Revision	Fix Status
[1]. Invalid Flash reads may occur if VDD is pulled to –0.5 V just before power-on	CY8C29xxx	A	No silicon fix is planned. Workaround is required.
[2]. Internal main oscillator (IMO) tolerance deviation at temperature extremes	CY8C29xxx	A	No silicon fix planned. Workaround is required.

1. Invalid Flash reads may occur if VDD is pulled to –0.5 V just before power-on

■ Problem Definition

When V_{DD} of the device is pulled below ground just before power-on; the first read from each 8 K Flash bank may be corrupted. This issue does not affect Flash bank 0 because it is the selected bank upon reset.

■ Parameters Affected

When VDD is pulled below ground prior to power-on, an internal Flash reference may deviate from its nominal voltage. The reference deviation tends to result in the first Flash read from that bank returning 0xFF. During the first read from each bank, the reference is reset resulting in all future reads returning the correct value. A short delay of 5 µs before the first real read provides time for the reference voltage to stabilize. When V_{DD} of the device is pulled below ground just before power-on; the first read from each 8K Flash bank may be corrupted apart from Flash bank 0. This can be solved by doing a dummy read from each Flash bank prior to use of the Flash banks.

■ Workaround

To prevent an invalid Flash read, a dummy read from each Flash bank must occur prior to use of the Flash banks. A delay of 5 µs must occur after the dummy read and before a real read. The dummy reads should occur as soon as possible and must be located in Flash bank 0 prior to a read from any other Flash bank. An example for reading a byte of memory from each Flash bank is listed below and should be placed in boot.tpl and boot.asm immediately after the ‘start:’ label.

```
// dummy read from each 8 K Flash bank
// bank 1
mov A, 0x20     // MSB
mov X, 0x00     // LSB
romx
// bank 2
mov A, 0x40     // MSB
mov X, 0x00     // LSB
romx
// bank 3
mov A, 0x60     // MSB
mov X, 0x00     // LSB
romx
// wait at least 5 µs
mov X, 14
loop1:
dec X
jnz loop1
```

2. Internal main oscillator (IMO) tolerance deviation at temperature extremes

■ **Problem Definition**

Asynchronous digital communications interfaces may fail framing beyond 0 to 70 °C. This problem does not affect end-product usage between 0 and 70 °C.

■ **Parameters Affected**

The IMO frequency tolerance. The worst case deviation when operated below 0 °C and above +70 °C and within the upper and lower datasheet temperature range is ±5%.

■ **Trigger Condition(S)**

The asynchronous Rx/Tx clock source IMO frequency tolerance may deviate beyond the data sheet limit of ±2.5% when operated beyond the temperature range of 0 to +70 °C.

■ **Scope of Impact**

This problem may affect UART, IrDA, and FSK implementations.

■ **Workaround**

Implement a quartz crystal stabilized clock source on at least one end of the asynchronous digital communications interface.

■ **Fix Status**

Silicon fix is not planned. The workaround mentioned above should be used.