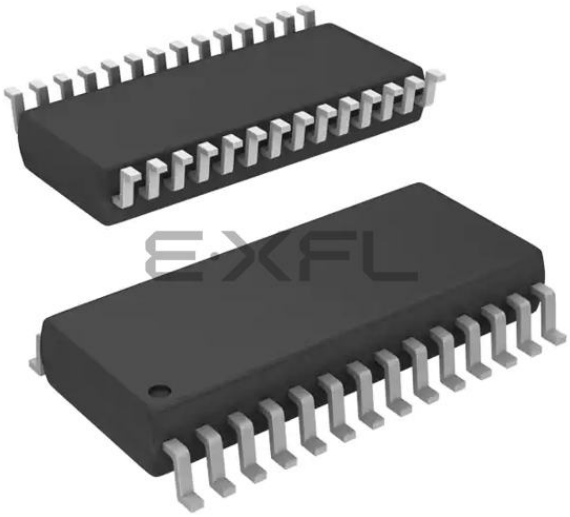


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	M8C
Core Size	8-Bit
Speed	24MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	24
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.25V
Data Converters	A/D 12x14b; D/A 4x9b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c29466-24sxi

More Information

Cypress provides a wealth of data at www.cypress.com to help you to select the right PSoC device for your design, and to help you to quickly and effectively integrate the device into your design. For a comprehensive list of resources, see the knowledge base article "How to Design with PSoC® 1, PowerPSoC®, and PLC – KBA88292". Following is an abbreviated list for PSoC 1:

- Overview: PSoC Portfolio, PSoC Roadmap
- Product Selectors: PSoC 1, PSoC 3, PSoC 4, PSoC 5LP
- In addition, PSoC Designer includes a device selection tool.
- Application notes: Cypress offers a large number of PSoC application notes covering a broad range of topics, from basic to advanced level. Recommended application notes for getting started with PSoC 1 are:
  - Getting Started with PSoC® 1 – AN75320
  - PSoC® 1 - Getting Started with GPIO – AN2094
  - PSoC® 1 Analog Structure and Configuration – AN74170
  - PSoC® 1 Switched Capacitor Analog Blocks – AN2041
  - Selecting Analog Ground and Reference – AN2219

Note: For CY8C29X66 devices related Application note please click here.

- Development Kits:
  - CY3210-PSoCEval1 supports all PSoC 1 Mixed-Signal Array families, including automotive, except CY8C25/26xxx devices. The kit includes an LCD module, potentiometer, LEDs, and breadboarding space.
  - CY3214-PSoCEvalUSB features a development board for the CY8C24x94 PSoC device. Special features of the board include USB and CapSense development and debugging support.

Note: For CY8C29X66 devices related Development Kits please click here.

The MiniProg1 and MiniProg3 devices provide interfaces for flash programming and debug.

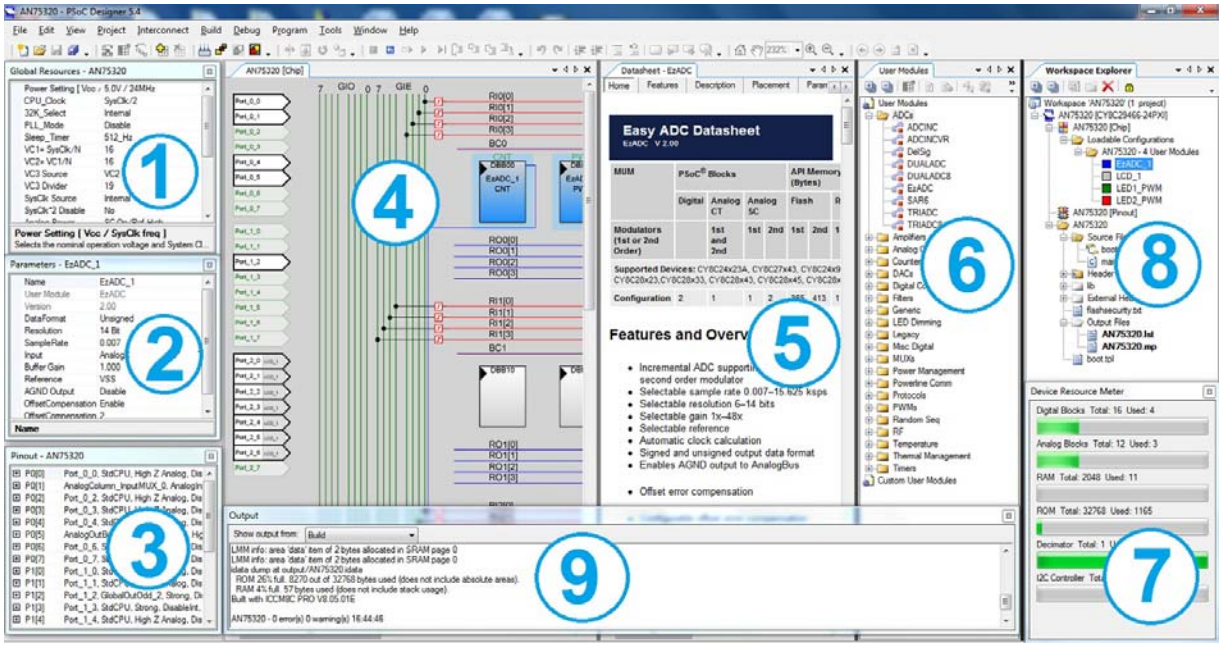
PSoC Designer

PSoC Designer is a free Windows-based Integrated Design Environment (IDE). Develop your applications using a library of pre-characterized analog and digital peripherals in a drag-and-drop design environment. Then, customize your design leveraging the dynamically generated API libraries of code. Figure 1 shows PSoC Designer windows. **Note:** This is not the default view.

1. **Global Resources –** all device hardware settings.
2. **Parameters –** the parameters of the currently selected User Modules.
3. **Pinout –** information related to device pins.
4. **Chip-Level Editor –** a diagram of the resources available on the selected chip.
5. **Datasheet –** the datasheet for the currently selected UM
6. **User Modules –** all available User Modules for the selected device.
7. **Device Resource Meter –** device resource usage for the current project configuration.
8. **Workspace –** a tree level diagram of files associated with the project.
9. **Output –** output from project build and debug operations.

Note: For detailed information on PSoC Designer, go to PSoC® Designer > Help > Documentation > Designer Specific Documents > IDE User Guide.

Figure 1. PSoC Designer Layout



Additional System Resources

System resources, some of which were previously listed, provide additional capability useful to complete systems. Additional resources include a multiplier, decimator, switch mode pump, low-voltage detection, and power-on-reset (POR).

- Digital clock dividers provide three customizable clock frequencies for use in applications. The clocks can be routed to both the digital and analog systems. Additional clocks can be generated using digital PSoC blocks as clock dividers.
- Multiply accumulate (MAC) provides a fast 8-bit multiplier with 32-bit accumulate, to assist in general math and digital filters.
- The decimator provides a custom hardware filter for digital signal processing applications including the creation of delta sigma ADCs.
- The I^2C module provides 100 and 400 kHz communication over two wires. Slave, master, and multi-master modes are all supported.
- LVD interrupts can signal the application of falling voltage levels, while the advanced POR circuit eliminates the need for a system supervisor.
- An internal 1.3 V reference provides an absolute reference for the analog system, including ADCs and DACs.
- An integrated switch-mode pump (SMP) generates normal operating voltages from a single 1.2 V battery cell, providing a low cost boost converter.

PSoC Device Characteristics

Depending on your PSoC device characteristics, the digital and analog systems can have 16, 8, or 4 digital blocks and 12, 6, or 4 analog blocks. The following table lists the resources available for specific PSoC device groups.The PSoC device covered by this datasheet is highlighted.

Table 1. PSoC Device Characteristics

PSoC Part Number	Digital I/O	Digital Rows	Digital Blocks	Analog Inputs	Analog Outputs	Analog Columns	Analog Blocks	SRAM Size	Flash Size
CY8C29x66	up to 64	4	16	up to 12	4	4	12	2 K	32 K
CY8C28xxx	up to 44	up to 3	up to 12	up to 44	up to 4	up to 6	up to 12 + 4[3]	1 K	16 K
CY8C27x43	up to 44	2	8	up to 12	4	4	12	256	16 K
CY8C24x94	up to 56	1	4	up to 48	2	2	6	1 K	16 K
CY8C24x23A	up to 24	1	4	up to 12	2	2	6	256	4 K
CY8C23x33	up to 26	1	4	up to 12	2	2	4	256	8 K
CY8C22x45	up to 38	2	8	up to 38	0	4	6[3]	1 K	16 K
CY8C21x45	up to 24	1	4	up to 24	0	4	6[3]	512	8 K
CY8C21x34	up to 28	1	4	up to 28	0	2	4[3]	512	8 K
CY8C21x23	up to 16	1	4	up to 8	0	2	4[3]	256	4 K
CY8C20x34	up to 28	0	0	up to 28	0	0	3[3,4]	512	8 K
CY8C20xx6	up to 36	0	0	up to 36	0	0	3[3,4]	up to 2 K	up to 32 K

Notes
3. Limited analog functionality.
4. Two analog blocks and one CapSense®.

100-Pin Part Pinout

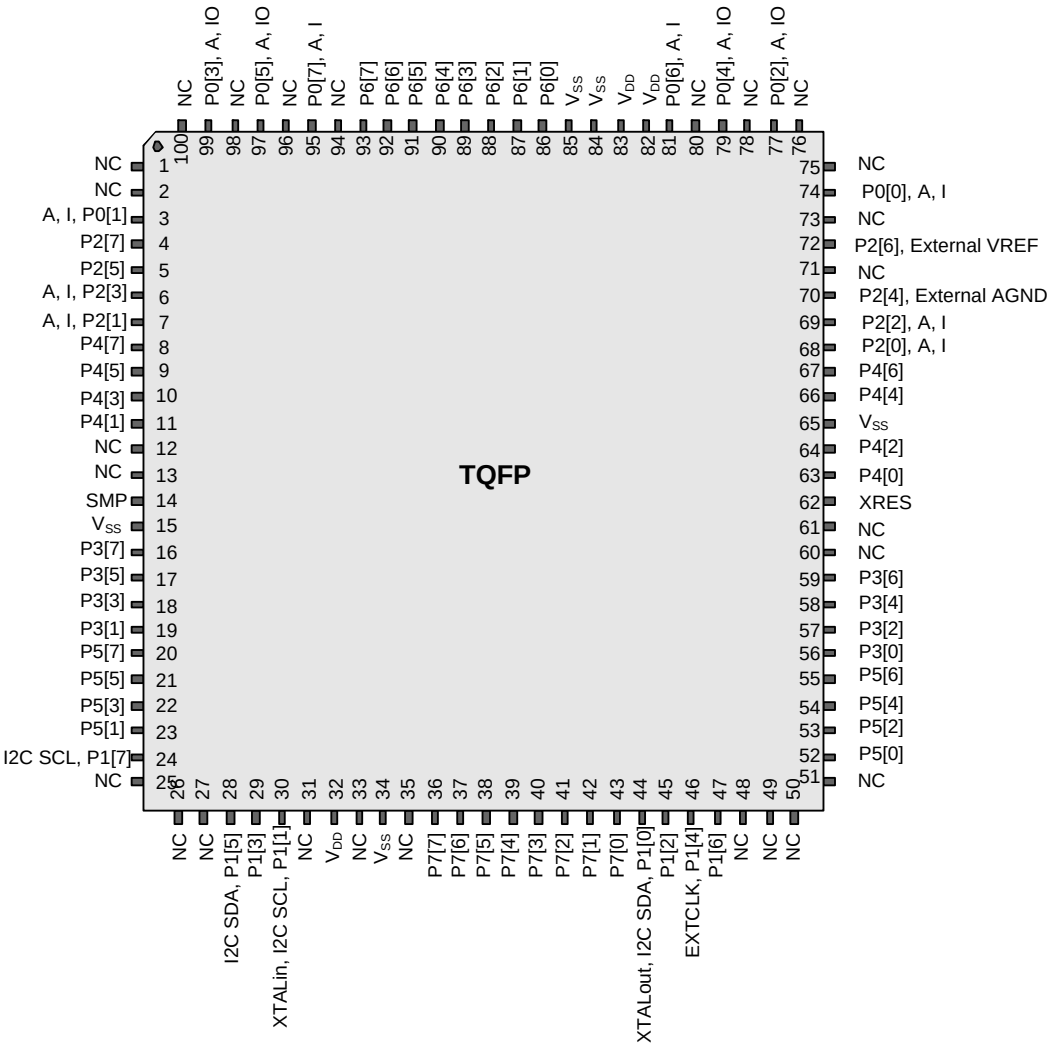
Table 6. 100-Pin Part Pinout (TQFP)

Pin No.	Type		Name	Description	Pin No.	Type		Name	Description
	Digital	Analog				Digital	Analog		
1			NC	No connection. Pin must be left floating	51			NC	No connection. Pin must be left floating
2			NC	No connection. Pin must be left floating	52	I/O		P5[0]	
3	I/O	I	P0[1]	Analog column mux input	53	I/O		P5[2]	
4	I/O		P2[7]		54	I/O		P5[4]	
5	I/O		P2[5]		55	I/O		P5[6]	
6	I/O	I	P2[3]	Direct switched capacitor block input	56	I/O		P3[0]	
7	I/O	I	P2[1]	Direct switched capacitor block input	57	I/O		P3[2]	
8	I/O		P4[7]		58	I/O		P3[4]	
9	I/O		P4[5]		59	I/O		P3[6]	
10	I/O		P4[3]		60			NC	No connection. Pin must be left floating
11	I/O		P4[1]		61			NC	No connection. Pin must be left floating
12			NC	No connection. Pin must be left floating	62	Input		XRES	Active high external reset with internal pull-down
13			NC	No connection. Pin must be left floating	63	I/O		P4[0]	
14	Power		SMP	Switch mode pump (SMP) connection to external components required	64	I/O		P4[2]	
15	Power		V_{SS}	Ground connection [10]	65	Power		V_{SS}	Ground connection [10]
16	I/O		P3[7]		66	I/O		P4[4]	
17	I/O		P3[5]		67	I/O		P4[6]	
18	I/O		P3[3]		68	I/O	I	P2[0]	Direct switched capacitor block input
19	I/O		P3[1]		69	I/O	I	P2[2]	Direct switched capacitor block input
20	I/O		P5[7]		70	I/O		P2[4]	External Analog Ground (AGND)
21	I/O		P5[5]		71			NC	No connection. Pin must be left floating
22	I/O		P5[3]		72	I/O		P2[6]	External Voltage Reference (VREF)
23	I/O		P5[1]		73			NC	No connection. Pin must be left floating
24	I/O		P1[7]	I^2C SCL	74	I/O	I	P0[0]	Analog column mux input
25			NC	No connection. Pin must be left floating	75			NC	No connection. Pin must be left floating
26			NC	No connection. Pin must be left floating	76			NC	No connection. Pin must be left floating
27			NC	No connection. Pin must be left floating	77	I/O	I/O	P0[2]	Analog column mux input and column output
28	I/O		P1[5]	I^2C SDA	78			NC	No connection. Pin must be left floating
29	I/O		P1[3]		79	I/O	I/O	P0[4]	Analog column mux input and column output
30	I/O		P1[1]	Crystal (XTALin), I^2C Serial Clock (SCL), ISSP-SCLK[11]	80			NC	No connection. Pin must be left floating
31			NC	No connection. Pin must be left floating	81	I/O	I	P0[6]	Analog column mux input
32	Power		V_{DD}	Supply voltage	82	Power		V_{DD}	Supply voltage
33			NC	No connection. Pin must be left floating	83	Power		V_{DD}	Supply voltage
34	Power		V_{SS}	Ground connection [10]	84	Power		V_{SS}	Ground connection [10]
35			NC	No connection. Pin must be left floating	85	Power		V_{SS}	Ground connection [10]
36	I/O		P7[7]		86	I/O		P6[0]	
37	I/O		P7[6]		87	I/O		P6[1]	
38	I/O		P7[5]		88	I/O		P6[2]	
39	I/O		P7[4]		89	I/O		P6[3]	
40	I/O		P7[3]		90	I/O		P6[4]	
41	I/O		P7[2]		91	I/O		P6[5]	
42	I/O		P7[1]		92	I/O		P6[6]	
43	I/O		P7[0]		93	I/O		P6[7]	
44	I/O		P1[0]	Crystal (XTALout), I^2C Serial Data (SDA), ISSP-SDATA[11]	94			NC	No connection. Pin must be left floating
45	I/O		P1[2]		95	I/O	I	P0[7]	Analog column mux input
46	I/O		P1[4]	Optional EXTCLK	96			NC	No connection. Pin must be left floating
47	I/O		P1[6]		97	I/O	I/O	P0[5]	Analog column mux input and column output
48			NC	No connection. Pin must be left floating	98			NC	No connection. Pin must be left floating
49			NC	No connection. Pin must be left floating	99	I/O	I/O	P0[3]	Analog column mux input and column output
50			NC	No connection. Pin must be left floating	100			NC	No connection. Pin must be left floating

LEGEND: A = Analog, I = Input, and O = Output.

Notes
10. All V_{SS} pins should be brought out to one common GND plane.
11. These are the ISSP pins, which are not High Z at POR. See the *PSoC Programmable System-on-Chip Technical Reference Manual* for details.

Figure 8. CY8C29866 100-Pin PSoC Device



100-Pin Part Pinout (On-Chip Debug)

The 100-pin TQFP part is for the CY8C29000 On-Chip Debug (OCD) PSoC device.

Note OCD parts are only used for in-circuit debugging. OCD parts are NOT available for production.

Table 7. 100-Pin OCD Part Pinout (TQFP)

Pin No.	Digital	Analog	Name	Description	Pin No.	Digital	Analog	Name	Description
1			NC	No internal connection	51			NC	No internal connection
2			NC	No internal connection	52	I/O		P5[0]	
3	I/O	I	P0[1]	Analog column mux input	53	I/O		P5[2]	
4	I/O		P2[7]		54	I/O		P5[4]	
5	I/O		P2[5]		55	I/O		P5[6]	
6	I/O	I	P2[3]	Direct switched capacitor block input	56	I/O		P3[0]	
7	I/O	I	P2[1]	Direct switched capacitor block input	57	I/O		P3[2]	
8	I/O		P4[7]		58	I/O		P3[4]	
9	I/O		P4[5]		59	I/O		P3[6]	
10	I/O		P4[3]		60			HCLK	OCD high speed clock output
11	I/O		P4[1]		61			CCLK	OCD CPU clock output
12			OCDE	OCD even data I/O	62	Input		XRES	Active high pin reset with internal pull-down
13			OCDO	OCD odd data output	63	I/O		P4[0]	
14	Power		SMP	Switch Mode Pump (SMP) connection to required external components	64	I/O		P4[2]	
15	Power		V_{SS}	Ground connection [12]	65	Power		V_{SS}	Ground connection [12]
16	I/O		P3[7]		66	I/O		P4[4]	
17	I/O		P3[5]		67	I/O		P4[6]	
18	I/O		P3[3]		68	I/O	I	P2[0]	Direct switched capacitor block input
19	I/O		P3[1]		69	I/O	I	P2[2]	Direct switched capacitor block input
20	I/O		P5[7]		70	I/O		P2[4]	External Analog Ground (AGND) input
21	I/O		P5[5]		71			NC	No internal connection
22	I/O		P5[3]		72	I/O		P2[6]	External Voltage Reference (VREF) input
23	I/O		P5[1]		73			NC	No internal connection
24	I/O		P1[7]	I^2C SCL	74	I/O	I	P0[0]	Analog column mux input
25			NC	No internal connection	75			NC	No internal connection
26			NC	No internal connection	76			NC	No internal connection
27			NC	No internal connection	77	I/O	I/O	P0[2]	Analog column mux input and column output
28	I/O		P1[5]	I^2C SDA	78			NC	No internal connection
29	I/O		P1[3]	I_{FMTEST}	79	I/O	I/O	P0[4]	Analog column mux input and column output, V_{REF}
30	I/O		P1[1][13]	Crystal (XTALin), I^2C SCL, TC SCLK.	80			NC	No internal connection
31			NC	No internal connection	81	I/O	I	P0[6]	Analog column mux input
32	Power		V_{DD}	Supply voltage	82	Power		V_{DD}	Supply voltage
33			NC	No internal connection	83	Power		V_{DD}	Supply voltage
34	Power		V_{SS}	Ground connection [12]	84	Power		V_{SS}	Ground connection [12]
35			NC	No internal connection	85	Power		V_{SS}	Ground connection [12]
36	I/O		P7[7]		86	I/O		P6[0]	
37	I/O		P7[6]		87	I/O		P6[1]	
38	I/O		P7[5]		88	I/O		P6[2]	
39	I/O		P7[4]		89	I/O		P6[3]	
40	I/O		P7[3]		90	I/O		P6[4]	
41	I/O		P7[2]		91	I/O		P6[5]	
42	I/O		P7[1]		92	I/O		P6[6]	
43	I/O		P7[0]		93	I/O		P6[7]	
44	I/O		P1[0]*	Crystal (XTALout), I^2C SDA, TC SDATA	94			NC	No internal connection
45	I/O		P1[2]	V_{FMTEST}	95	I/O	I	P0[7]	Analog column mux input
46	I/O		P1[4]	Optional External Clock Input (EXTCLK)	96			NC	No internal connection
47	I/O		P1[6]		97	I/O	I/O	P0[5]	Analog column mux input and column output
48			NC	No internal connection	98			NC	No internal connection
49			NC	No internal connection	99	I/O	I/O	P0[3]	Analog column mux input and column output
50			NC	No internal connection	100			NC	No internal connection

LEGEND A = Analog, I = Input, O = Output, NC = No connection. Pin must be left floating, TC/TM: Test.

Notes
12. All V_{SS} pins should be brought out to one common GND plane.
13. ISSP pin which is not High-Z at POR.

Table 9. Register Map Bank 0 Table: User Space

Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access
PRT0DR	00	RW	DBB20DR0	40	#	ASC10CR0	80	RW	RDI2RI	C0	RW
PRT0IE	01	RW	DBB20DR1	41	W	ASC10CR1	81	RW	RDI2SYN	C1	RW
PRT0GS	02	RW	DBB20DR2	42	RW	ASC10CR2	82	RW	RDI2IS	C2	RW
PRT0DM2	03	RW	DBB20CR0	43	#	ASC10CR3	83	RW	RDI2LT0	C3	RW
PRT1DR	04	RW	DBB21DR0	44	#	ASD11CR0	84	RW	RDI2LT1	C4	RW
PRT1IE	05	RW	DBB21DR1	45	W	ASD11CR1	85	RW	RDI2RO0	C5	RW
PRT1GS	06	RW	DBB21DR2	46	RW	ASD11CR2	86	RW	RDI2RO1	C6	RW
PRT1DM2	07	RW	DBB21CR0	47	#	ASD11CR3	87	RW		C7	
PRT2DR	08	RW	DCB22DR0	48	#	ASC12CR0	88	RW	RDI3RI	C8	RW
PRT2IE	09	RW	DCB22DR1	49	W	ASC12CR1	89	RW	RDI3SYN	C9	RW
PRT2GS	0A	RW	DCB22DR2	4A	RW	ASC12CR2	8A	RW	RDI3IS	CA	RW
PRT2DM2	0B	RW	DCB22CR0	4B	#	ASC12CR3	8B	RW	RDI3LT0	CB	RW
PRT3DR	0C	RW	DCB23DR0	4C	#	ASD13CR0	8C	RW	RDI3LT1	CC	RW
PRT3IE	0D	RW	DCB23DR1	4D	W	ASD13CR1	8D	RW	RDI3RO0	CD	RW
PRT3GS	0E	RW	DCB23DR2	4E	RW	ASD13CR2	8E	RW	RDI3RO1	CE	RW
PRT3DM2	0F	RW	DCB23CR0	4F	#	ASD13CR3	8F	RW		CF	
PRT4DR	10	RW	DBB30DR0	50	#	ASD20CR0	90	RW	CUR_PP	D0	RW
PRT4IE	11	RW	DBB30DR1	51	W	ASD20CR1	91	RW	STK_PP	D1	RW
PRT4GS	12	RW	DBB30DR2	52	RW	ASD20CR2	92	RW		D2	
PRT4DM2	13	RW	DBB30CR0	53	#	ASD20CR3	93	RW	IDX_PP	D3	RW
PRT5DR	14	RW	DBB31DR0	54	#	ASC21CR0	94	RW	MVR_PP	D4	RW
PRT5IE	15	RW	DBB31DR1	55	W	ASC21CR1	95	RW	MVW_PP	D5	RW
PRT5GS	16	RW	DBB31DR2	56	RW	ASC21CR2	96	RW	I2C_CFG	D6	RW
PRT5DM2	17	RW	DBB31CR0	57	#	ASC21CR3	97	RW	I2C_SCR	D7	#
PRT6DR	18	RW	DCB32DR0	58	#	ASD22CR0	98	RW	I2C_DR	D8	RW
PRT6IE	19	RW	DCB32DR1	59	W	ASD22CR1	99	RW	I2C_MSCR	D9	#
PRT6GS	1A	RW	DCB32DR2	5A	RW	ASD22CR2	9A	RW	INT_CLR0	DA	RW
PRT6DM2	1B	RW	DCB32CR0	5B	#	ASD22CR3	9B	RW	INT_CLR1	DB	RW
PRT7DR	1C	RW	DCB33DR0	5C	#	ASC23CR0	9C	RW	INT_CLR2	DC	RW
PRT7IE	1D	RW	DCB33DR1	5D	W	ASC23CR1	9D	RW	INT_CLR3	DD	RW
PRT7GS	1E	RW	DCB33DR2	5E	RW	ASC23CR2	9E	RW	INT_MSK3	DE	RW
PRT7DM2	1F	RW	DCB33CR0	5F	#	ASC23CR3	9F	RW	INT_MSK2	DF	RW
DBB00DR0	20	#	AMX_IN	60	RW		A0		INT_MSK0	E0	RW
DBB00DR1	21	W		61			A1		INT_MSK1	E1	RW
DBB00DR2	22	RW		62			A2		INT_VC	E2	RC
DBB00CR0	23	#	ARF_CR	63	RW		A3		RES_WDT	E3	W
DBB01DR0	24	#	CMP_CR0	64	#		A4		DEC_DH	E4	RC
DBB01DR1	25	W	ASY_CR	65	#		A5		DEC_DL	E5	RC
DBB01DR2	26	RW	CMP_CR1	66	RW		A6		DEC_CR0	E6	RW
DBB01CR0	27	#		67			A7		DEC_CR1	E7	RW
DCB02DR0	28	#		68		MUL1_X	A8	W	MUL0_X	E8	W
DCB02DR1	29	W		69		MUL1_Y	A9	W	MUL0_Y	E9	W
DCB02DR2	2A	RW		6A		MUL1_DH	AA	R	MUL0_DH	EA	R
DCB02CR0	2B	#		6B		MUL1_DL	AB	R	MUL0_DL	EB	R
DCB03DR0	2C	#	TMP_DR0	6C	RW	ACC1_DR1	AC	RW	ACC0_DR1	EC	RW
DCB03DR1	2D	W	TMP_DR1	6D	RW	ACC1_DR0	AD	RW	ACC0_DR0	ED	RW
DCB03DR2	2E	RW	TMP_DR2	6E	RW	ACC1_DR3	AE	RW	ACC0_DR3	EE	RW
DCB03CR0	2F	#	TMP_DR3	6F	RW	ACC1_DR2	AF	RW	ACC0_DR2	EF	RW
DBB10DR0	30	#	ACB00CR3	70	RW	RDI0RI	B0	RW		F0	
DBB10DR1	31	W	ACB00CR0	71	RW	RDI0SYN	B1	RW		F1	
DBB10DR2	32	RW	ACB00CR1	72	RW	RDI0IS	B2	RW		F2	
DBB10CR0	33	#	ACB00CR2	73	RW	RDI0LT0	B3	RW		F3	
DBB11DR0	34	#	ACB01CR3	74	RW	RDI0LT1	B4	RW		F4	
DBB11DR1	35	W	ACB01CR0	75	RW	RDI0RO0	B5	RW		F5	
DBB11DR2	36	RW	ACB01CR1	76	RW	RDI0RO1	B6	RW		F6	
DBB11CR0	37	#	ACB01CR2	77	RW		B7		CPU_F	F7	RL
DCB12DR0	38	#	ACB02CR3	78	RW	RDI1RI	B8	RW		F8	
DCB12DR1	39	W	ACB02CR0	79	RW	RDI1SYN	B9	RW		F9	
DCB12DR2	3A	RW	ACB02CR1	7A	RW	RDI1IS	BA	RW		FA	
DCB12CR0	3B	#	ACB02CR2	7B	RW	RDI1LT0	BB	RW		FB	
DCB13DR0	3C	#	ACB03CR3	7C	RW	RDI1LT1	BC	RW		FC	
DCB13DR1	3D	W	ACB03CR0	7D	RW	RDI1RO0	BD	RW		FD	
DCB13DR2	3E	RW	ACB03CR1	7E	RW	RDI1RO1	BE	RW	CPU_SCR1	FE	#
DCB13CR0	3F	#	ACB03CR2	7F	RW		BF		CPU_SCR0	FF	#

Blank fields are Reserved and should not be accessed. # Access is bit specific.

Electrical Specifications

This section presents the DC and AC electrical specifications of the CY8C29x66 PSoC device. For the most up-to-date electrical specifications, confirm that you have the most recent datasheet by going to the web at http://www.cypress.com.

Specifications are valid for –40 °C ≤ T_A ≤ 85 °C and T_J ≤ 100 °C, except where noted. Refer to Table 29 for the electrical specifications on the internal main oscillator (IMO) using SLIMO mode.

Figure 10. Voltage versus CPU Frequency

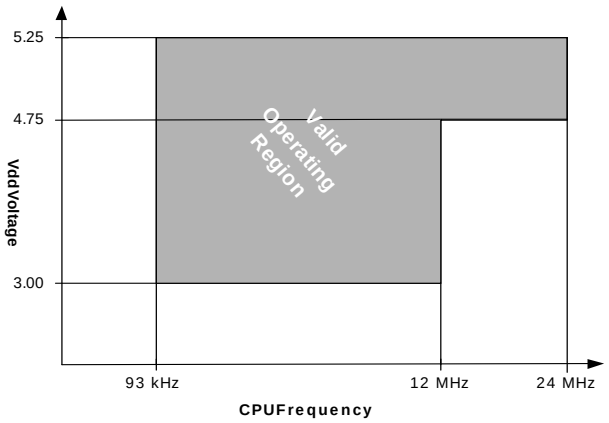
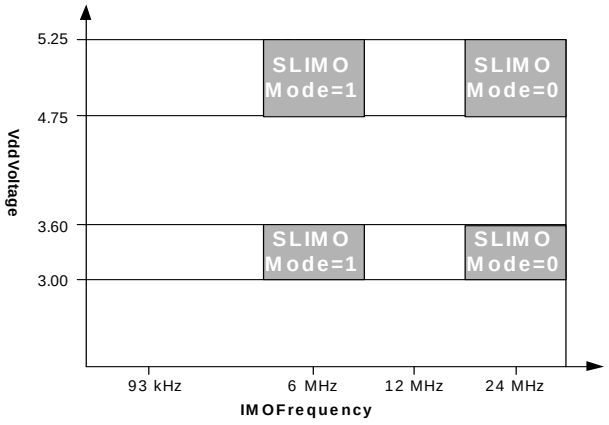


Figure 11. IMO Frequency Options



Absolute Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Table 11. Absolute Maximum Ratings

Symbol	Description	Min	Typ	Max	Unit	Notes
T_{STG}	Storage temperature	–55	25	+100	°C	Higher storage temperatures reduce data retention time. Recommended storage temperature is +25 °C ± 25 °C. Extended duration storage temperatures higher than 65 °C degrade reliability.
$T_{BAKETEMP}$	Bake temperature	–	125	See package label	°C	
$T_{BAKETIME}$	Bake time	See package label	–	72	Hours	
T_A	Ambient temperature with power applied	–40	–	+85	°C	
V_{DD}	Supply voltage on V_{DD} relative to V_{SS}	–0.5	–	+6.0	V	
V_{IO}	DC input voltage	V_{SS} – 0.5	–	V_{DD} + 0.5	V	
V_{IOZ}	DC voltage applied to tristate	V_{SS} – 0.5	–	V_{DD} + 0.5	V	
I_{MIO}	Maximum current into any port pin	–25	–	+50	mA	
I_{MAIO}	Maximum current into any port pin configured as analog driver	–50	–	+50	mA	
ESD	Electrostatic discharge voltage	2000	–	–	V	Human body model ESD.
LU	Latch-up current	–	–	200	mA	

Table 16. 3.3-V DC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Unit	Notes
V_{OSOA}	Input offset voltage (absolute value) Power = Low, Opamp bias = Low Power = Low, Opamp bias = High Power = Medium, Opamp bias = Low Power = Medium, Opamp bias = High Power = High, Opamp bias = Low Power = High, Opamp bias = High	 – – – – – –	 1.4 1.4 1.4 1.4 1.4 –	 10 10 10 10 10 –	 mV mV mV mV mV mV	Power = High, Opamp bias = High setting is not allowed for 3.3 V V_{DD} operation.
TCV_{OSOA}	Average input offset voltage drift	–	7	40	µV/°C	
I_{EBOA}	Input leakage current (port 0 analog pins)	–	200	–	pA	Gross tested to 1 µA.
C_{INOA}	Input capacitance (port 0 analog pins)	–	4.5	9.5	pF	Package and pin dependent. Temp = 25 °C
V_{CMOA}	Common mode voltage range	0	–	V_{DD}	V	The common-mode input voltage range is measured through an analog output buffer. The specification includes the limitations imposed by the characteristics of the analog output buffer.
$CMRR_{OA}$	Common mode rejection ratio	60	–	–	dB	
G_{OLOA}	Open loop gain	80	–	–	dB	
$V_{OHIGHOA}$	High output voltage swing (internal signals)	V_{DD} – 0.01	–	–	V	
V_{OLOWOA}	Low output voltage swing (internal signals)	–	–	0.01	V	
I_{SOA}	Supply current (including associated AGND buffer) Power = Low, Opamp bias = Low Power = Low, Opamp bias = High Power = Medium, Opamp bias = Low Power = Medium, Opamp bias = High Power = High, Opamp bias = Low Power = High, Opamp bias = High	 – – – – – –	 150 300 600 1200 2400 –	 200 400 800 1600 3200 –	 µA µA µA µA µA µA	Power = High, Opamp bias = High setting is not allowed for 3.3 V V_{DD} operation.
$PSRR_{OA}$	Supply voltage rejection ratio	54	80	–	dB	$V_{SS} \le V_{IN} \le (V_{DD} – 2.25)$ or $(V_{DD} – 1.25\ V) \le V_{IN} \le V_{DD}$

DC Low-Power Comparator Specifications

Table 17 lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V at 25 °C and are for design guidance only.

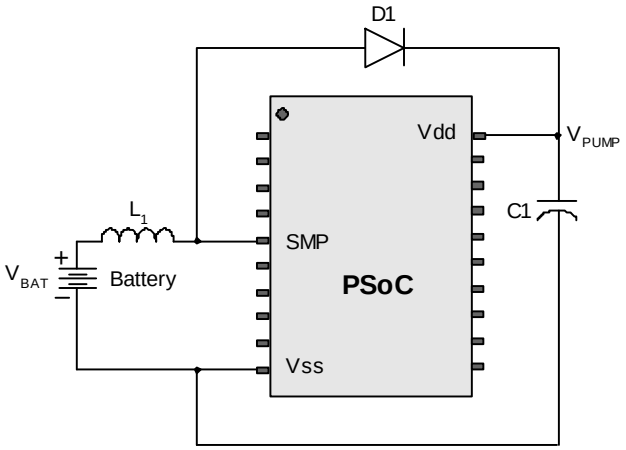
Table 17. DC Low-Power Comparator Specifications

Symbol	Description	Min	Typ	Max	Unit
V_{REFLPC}	Low-power comparator (LPC) reference voltage range	0.2	–	V_{DD} – 1	V
I_{SLPC}	LPC supply current	–	10	40	µA
V_{OSLPC}	LPC voltage offset	–	2.5	30	mV

Table 19. 3.3-V DC Analog Output Buffer Specifications

Symbol	Description	Min	Typ	Max	Unit	Notes
V_{OSOB}	Input offset voltage (absolute value) Power = Low, Opamp bias = Low Power = Low, Opamp bias = High Power = High, Opamp bias = Low Power = High, Opamp bias = High	 – – – –	 3.2 3.2 6 6	 20 20 25 25	 mV mV mV mV	High power setting is not recommended.
TCV_{OSOB}	Average input offset voltage drift Power = Low, Opamp bias = Low Power = Low, Opamp bias = High Power = High, Opamp bias = Low Power = High, Opamp bias = High	 – – – –	 8 8 12 12	 32 32 41 41	 µV/°C µV/°C µV/°C µV/°C	High power setting is not recommended.
V_{CMOB}	Common-mode input voltage range	0.5	–	$V_{DD} – 1.0$	V	
R_{OUTOB}	Output resistance Power = Low Power = High	 – –	 – –	 10 10	 W W	
$V_{OHIGHOB}$	High output voltage swing (Load = 32 ohms to $V_{DD}/2$) Power = Low Power = High	 $0.5 \times V_{DD} + 1.0$ $0.5 \times V_{DD} + 1.0$	 – –	 – –	 V V	
V_{OLOWOB}	Low output voltage swing (Load = 32 ohms to $V_{DD}/2$) Power = Low Power = High	 – –	 – –	 $0.5 \times V_{DD} – 1.0$ $0.5 \times V_{DD} – 1.0$	 V V	
I_{SOB}	Supply current including bias cell (no load) Power = Low Power = High	 – –	 0.8 2.0	 1 5	 mA mA	
$PSRR_{OB}$	Supply voltage rejection ratio	60	64	–	dB	
C_L	Load capacitance	–	–	200	pF	This specification applies to the external circuit driven by the analog output buffer.

Figure 12. Basic Switch Mode Pump Circuit



DC Analog Reference Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ TA ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ TA ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

The guaranteed specifications for RefHI and RefLO are measured through the analog continuous time PSoC blocks. The power levels for RefHI and RefLO refer to the analog reference control register. AGND is measured at P2[4] in AGND bypass mode. Each analog continuous time PSoC block adds a maximum of 10 mV additional offset error to guaranteed AGND specifications from the local AGND buffer. Reference control power can be set to medium or high unless otherwise noted.

Note Avoid using P2[4] for digital signaling when using an analog resource that depends on the analog reference. Some coupling of the digital signal may appear on the AGND.

Table 21. 5-V DC Analog Reference Specifications

Reference ARF_CR[5:3]	Reference Power Settings	Symbol	Reference	Description	Min	Typ	Max	Unit
0b000	RefPower = High Opamp bias = High	V_{REFHI}	Ref High	$V_{DD}/2$ + Bandgap	$V_{DD}/2$ + 1.228	$V_{DD}/2$ + 1.290	$V_{DD}/2$ + 1.352	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.078	$V_{DD}/2$ – 0.007	$V_{DD}/2$ + 0.063	V
		V_{REFLO}	Ref Low	$V_{DD}/2$ – Bandgap	$V_{DD}/2$ – 1.336	$V_{DD}/2$ – 1.295	$V_{DD}/2$ – 1.250	V
	RefPower = High Opamp bias = Low	V_{REFHI}	Ref High	$V_{DD}/2$ + Bandgap	$V_{DD}/2$ + 1.224	$V_{DD}/2$ + 1.293	$V_{DD}/2$ + 1.356	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.056	$V_{DD}/2$ – 0.005	$V_{DD}/2$ + 0.043	V
		V_{REFLO}	Ref Low	$V_{DD}/2$ – Bandgap	$V_{DD}/2$ – 1.338	$V_{DD}/2$ – 1.298	$V_{DD}/2$ – 1.255	V
	RefPower = Med Opamp bias = High	V_{REFHI}	Ref High	$V_{DD}/2$ + Bandgap	$V_{DD}/2$ + 1.226	$V_{DD}/2$ + 1.293	$V_{DD}/2$ + 1.356	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.057	$V_{DD}/2$ – 0.006	$V_{DD}/2$ + 0.044	V
		V_{REFLO}	Ref Low	$V_{DD}/2$ – Bandgap	$V_{DD}/2$ – 1.337	$V_{DD}/2$ – 1.298	$V_{DD}/2$ – 1.256	V
	RefPower = Med Opamp bias = Low	V_{REFHI}	Ref High	$V_{DD}/2$ + Bandgap	$V_{DD}/2$ + 1.226	$V_{DD}/2$ + 1.294	$V_{DD}/2$ + 1.359	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.047	$V_{DD}/2$ – 0.004	$V_{DD}/2$ + 0.035	V
		V_{REFLO}	Ref Low	$V_{DD}/2$ – Bandgap	$V_{DD}/2$ – 1.338	$V_{DD}/2$ – 1.299	$V_{DD}/2$ – 1.258	V

Table 21. 5-V DC Analog Reference Specifications (continued)

Reference ARF_CR[5:3]	Reference Power Settings	Symbol	Reference	Description	Min	Typ	Max	Unit
0b001	RefPower = High Opamp bias = High	V_{REFHI}	Ref High	P2[4] + P2[6] ($P2[4] = V_{DD}/2$, P2[6] = 1.3 V)	P2[4] + P2[6] – 0.085	P2[4] + P2[6] – 0.016	P2[4] + P2[6] + 0.044	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4] – P2[6] ($P2[4] = V_{DD}/2$, P2[6] = 1.3 V)	P2[4] – P2[6] – 0.022	P2[4] – P2[6] + 0.010	P2[4] – P2[6] + 0.055	V
	RefPower = High Opamp bias = Low	V_{REFHI}	Ref High	P2[4] + P2[6] ($P2[4] = V_{DD}/2$, P2[6] = 1.3 V)	P2[4] + P2[6] – 0.077	P2[4] + P2[6] – 0.010	P2[4] + P2[6] + 0.051	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4] – P2[6] ($P2[4] = V_{DD}/2$, P2[6] = 1.3 V)	P2[4] – P2[6] – 0.022	P2[4] – P2[6] + 0.005	P2[4] – P2[6] + 0.039	V
	RefPower = Med Opamp bias = High	V_{REFHI}	Ref High	P2[4] + P2[6] ($P2[4] = V_{DD}/2$, P2[6] = 1.3 V)	P2[4] + P2[6] – 0.070	P2[4] + P2[6] – 0.010	P2[4] + P2[6] + 0.050	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4] – P2[6] ($P2[4] = V_{DD}/2$, P2[6] = 1.3 V)	P2[4] – P2[6] – 0.022	P2[4] – P2[6] + 0.005	P2[4] – P2[6] + 0.039	V
	RefPower = Med Opamp bias = Low	V_{REFHI}	Ref High	P2[4] + P2[6] ($P2[4] = V_{DD}/2$, P2[6] = 1.3 V)	P2[4] + P2[6] – 0.070	P2[4] + P2[6] – 0.007	P2[4] + P2[6] + 0.054	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4] – P2[6] ($P2[4] = V_{DD}/2$, P2[6] = 1.3 V)	P2[4] – P2[6] – 0.022	P2[4] – P2[6] + 0.002	P2[4] – P2[6] + 0.032	V
0b010	RefPower = High Opamp bias = High	V_{REFHI}	Ref High	V_{DD}	V_{DD} – 0.037	V_{DD} – 0.009	V_{DD}	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.061	$V_{DD}/2$ – 0.006	$V_{DD}/2$ + 0.047	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.007	V_{SS} + 0.028	V
	RefPower = High Opamp bias = Low	V_{REFHI}	Ref High	V_{DD}	V_{DD} – 0.039	V_{DD} – 0.006	V_{DD}	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.049	$V_{DD}/2$ – 0.005	$V_{DD}/2$ + 0.036	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.005	V_{SS} + 0.019	V
	RefPower = Med Opamp bias = High	V_{REFHI}	Ref High	V_{DD}	V_{DD} – 0.037	V_{DD} – 0.007	V_{DD}	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.054	$V_{DD}/2$ – 0.005	$V_{DD}/2$ + 0.041	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.006	V_{SS} + 0.024	V
	RefPower = Med Opamp bias = Low	V_{REFHI}	Ref High	V_{DD}	V_{DD} – 0.042	V_{DD} – 0.005	V_{DD}	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.046	$V_{DD}/2$ – 0.004	$V_{DD}/2$ + 0.034	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.004	V_{SS} + 0.017	V

Table 22. 3.3-V DC Analog Reference Specifications (continued)

Reference ARF_CR[5:3]	Reference Power Settings	Symbol	Reference	Description	Min	Typ	Max	Unit
0b010	RefPower = High Opamp bias = High	V_{REFHI}	Ref High	V_{DD}	V_{DD} – 0.06	V_{DD} – 0.010	V_{DD}	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.05	$V_{DD}/2$ – 0.002	$V_{DD}/2$ + 0.040	V
		V_{REFLO}	Ref Low	Vss	Vss	Vss + 0.009	Vss + 0.056	V
	RefPower = High Opamp bias = Low	V_{REFHI}	Ref High	V_{DD}	V_{DD} – 0.060	V_{DD} – 0.006	V_{DD}	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.028	$V_{DD}/2$ – 0.001	$V_{DD}/2$ + 0.025	V
		V_{REFLO}	Ref Low	Vss	Vss	Vss + 0.005	Vss + 0.034	V
	RefPower = Med Opamp bias = High	V_{REFHI}	Ref High	V_{DD}	V_{DD} – 0.058	V_{DD} – 0.008	V_{DD}	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.037	$V_{DD}/2$ – 0.002	$V_{DD}/2$ + 0.033	V
		V_{REFLO}	Ref Low	Vss	Vss	Vss + 0.007	Vss + 0.046	V
	RefPower = Med Opamp bias = Low	V_{REFHI}	Ref High	V_{DD}	V_{DD} – 0.057	V_{DD} – 0.006	V_{DD}	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.025	$V_{DD}/2$ – 0.001	$V_{DD}/2$ + 0.022	V
		V_{REFLO}	Ref Low	Vss	Vss	Vss + 0.004	Vss + 0.030	V
0b011	All power settings. Not allowed for 3.3 V	–	–	–	–	–	–	–
0b100	All power settings. Not allowed for 3.3 V	–	–	–	–	–	–	–

Table 22. 3.3-V DC Analog Reference Specifications (continued)

Reference ARF_CR[5:3]	Reference Power Settings	Symbol	Reference	Description	Min	Typ	Max	Unit
0b101	RefPower = High Opamp bias = High	V_{REFHI}	Ref High	P2[4] + Band-Gap (P2[4] = $V_{DD}/2$)	P2[4] + 1.213	P2[4] + 1.291	P2[4] + 1.367	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	V
		V_{REFLO}	Ref Low	P2[4] – Band-Gap (P2[4] = $V_{DD}/2$)	P2[4] – 1.333	P2[4] – 1.294	P2[4] – 1.208	V
	RefPower = High Opamp bias = Low	V_{REFHI}	Ref High	P2[4] + Band-Gap (P2[4] = $V_{DD}/2$)	P2[4] + 1.217	P2[4] + 1.294	P2[4] + 1.368	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	V
		V_{REFLO}	Ref Low	P2[4] – Band-Gap (P2[4] = $V_{DD}/2$)	P2[4] – 1.320	P2[4] – 1.296	P2[4] – 1.261	V
	RefPower = Med Opamp bias = High	V_{REFHI}	Ref High	P2[4] + Band-Gap (P2[4] = $V_{DD}/2$)	P2[4] + 1.217	P2[4] + 1.294	P2[4] + 1.369	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	V
		V_{REFLO}	Ref Low	P2[4] – Band-Gap (P2[4] = $V_{DD}/2$)	P2[4] – 1.322	P2[4] – 1.297	P2[4] – 1.262	V
	RefPower = Med Opamp bias = Low	V_{REFHI}	Ref High	P2[4] + Band-Gap (P2[4] = $V_{DD}/2$)	P2[4] + 1.219	P2[4] + 1.295	P2[4] + 1.37	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	V
		V_{REFLO}	Ref Low	P2[4] – Band-Gap (P2[4] = $V_{DD}/2$)	P2[4] – 1.324	P2[4] – 1.297	P2[4] – 1.262	V
0b110	RefPower = High Opamp bias = High	V_{REFHI}	Ref High	2 × BandGap	2.507	2.598	2.698	V
		V_{AGND}	AGND	BandGap	1.203	1.307	1.424	V
		V_{REFLO}	Ref Low	Vss	Vss	Vss + 0.012	Vss + 0.067	V
	RefPower = High Opamp bias = Low	V_{REFHI}	Ref High	2 × BandGap	2.516	2.598	2.683	V
		V_{AGND}	AGND	BandGap	1.241	1.303	1.376	V
		V_{REFLO}	Ref Low	Vss	Vss	Vss + 0.007	Vss + 0.040	V
	RefPower = Med Opamp bias = High	V_{REFHI}	Ref High	2 × BandGap	2.510	2.599	2.693	V
		V_{AGND}	AGND	BandGap	1.240	1.305	1.374	V
		V_{REFLO}	Ref Low	Vss	Vss	Vss + 0.008	Vss + 0.048	V
	RefPower = Med Opamp bias = Low	V_{REFHI}	Ref High	2 × BandGap	2.515	2.598	2.683	V
		V_{AGND}	AGND	BandGap	1.258	1.302	1.355	V
		V_{REFLO}	Ref Low	Vss	Vss	Vss + 0.005	Vss + 0.03	V
0b111	All power settings. Not allowed for 3.3 V.	–	–	–	–	–	–	–

AC Electrical Characteristics

AC Chip-Level Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Note See the individual user module datasheets for information on maximum frequencies for user modules.

Table 29. AC Chip-Level Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{IMO24} [21]	Internal main oscillator (IMO) frequency for 24 MHz	22.8	24	25.2[22,23]	MHz	Trimmed for 5 V or 3.3 V operation using factory trim values. See Figure 11 on page 21. SLIMO Mode = 0.
F_{IMO6}	IMO frequency for 6 MHz	5.5	6	6.5[22,23]	MHz	Trimmed for 5 V or 3.3 V operation using factory trim values. See Figure 11 on page 21. SLIMO Mode = 1.
F_{CPU1}	CPU frequency (5 V Nominal)	0.0914	24	25.2[22]	MHz	SLIMO Mode = 0.
F_{CPU2}	CPU frequency (3.3 V Nominal)	0.0914	12	12.6[23]	MHz	SLIMO Mode = 0.
F_{48M}	Digital PSoC block frequency	0	48	50.4[22,24]	MHz	Refer to AC Digital Block Specifications on page 45.
F_{24M}	Digital PSoC block frequency	0	24	25.2 [24]	MHz	
F_{32K1}	Internal low speed oscillator frequency	15	32	64	kHz	
F_{32K2}	External crystal oscillator	–	32.768	–	kHz	Accuracy is capacitor and crystal dependent. 50% duty cycle
F_{32K_U}	Internal low speed oscillator (ILO) untrimmed frequency	5	–	100	kHz	After a reset and before the M8C starts to run, the ILO is not trimmed. See the System Resets section of the PSoC Technical Reference Manual for details on this timing
F_{PLL}	PLL frequency	–	23.986	–	MHz	A multiple (x732) of crystal frequency
$T_{PLLSLEW}$	PLL lock time	0.5	–	10	ms	
$T_{PLLSLEWLOW}$	PLL lock time for low gain setting	0.5	–	50	ms	
T_{OS}	External crystal oscillator startup to 1%	–	250	500	ms	
T_{OSACC}	External crystal oscillator startup to 100 ppm	–	300	600	ms	The crystal oscillator frequency is within 100 ppm of its final value by the end of the T_{OSACC} period. Correct operation assumes a properly loaded 1 µW maximum drive level 32.768 kHz crystal. 3.0 V ≤ V_{DD} ≤ 5.5 V, –40 °C ≤ T_A ≤ 85 °C.
T_{XRST}	External reset pulse width	10	–	–	µs	
DC24M	24 MHz duty cycle	40	50	60	%	
DC_{ILO}	Internal low speed oscillator duty cycle	20	50	80	%	
Step24M	24 MHz trim step size	–	50	–	kHz	
Fout48M	48 MHz output frequency	45.6	48.0	50.4[22, 23]	MHz	Trimmed. Using factory trim values
F_{MAX}	Maximum frequency of signal on row input or row output.	–	–	12.3	MHz	

Notes
21. Errata: When the device is operated within 0 °C to 70 °C, the frequency tolerance is reduced to ±2.5%, but if operated at extreme temperature (below 0 °C or above 70 °C), frequency tolerance deviates from ±2.5% to ±5%. For more information, see Errata on page 63.
22. 4.75 V < V_{DD} < 5.25 V.
23. 3.0 V < V_{DD} < 3.6 V. See application note Adjusting PSoC® Trims for 3.3 V and 2.7 V Operation – AN2012 for information on trimming for operation at 3.3 V.
24. See the individual user module datasheets for information on maximum frequencies for user modules

Table 38. 3.3-V AC External Clock Specifications

Symbol	Description	Min	Typ	Max	Unit
F_{OSCEXT}	Frequency with CPU clock divide by 1	0.093	–	12.3	MHz
F_{OSCEXT}	Frequency with CPU clock divide by 2 or greater	0.186	–	24.6	MHz
–	High period with CPU clock divide by 1	41.7	–	5300	ns
–	Low period with CPU clock divide by 1	41.7	–	–	ns
–	Power-up IMO to switch	150	–	–	µs

AC Programming Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 39. AC Programming Specifications

Symbol	Description	Min	Typ	Max	Unit	Notes
t_{RSCLK}	Rise time of SCLK	1	–	20	ns	–
t_{FSCLK}	Fall time of SCLK	1	–	20	ns	–
t_{SSCLK}	Data setup time to falling edge of SCLK	40	–	–	ns	–
t_{HSCLK}	Data hold time from falling edge of SCLK	40	–	–	ns	–
F_{SCLK}	Frequency of SCLK	0	–	8	MHz	–
t_{ERASEB}	Flash erase time (block)	–	10	–	ms	–
t_{WRITE}	Flash block write time	–	40	–	ms	–
t_{DSCLK}	Data out delay from falling edge of SCLK	–	–	45	ns	$V_{DD} > 3.6$
t_{DSCLK3}	Data out delay from falling edge of SCLK	–	–	50	ns	$3.0 \le V_{DD} \le 3.6$
$t_{ERASEALL}$	Flash erase time (Bulk)	–	80	–	ms	Erase all blocks and protection fields at once
$t_{PROGRAM\_HOT}$	Flash block erase + Flash block write time	–	–	100[28]	ms	0 °C ≤ Tj ≤ 100 °C
$t_{PROGRAM\_COLD}$	Flash block erase + Flash block write time	–	–	200[28]	ms	–40 °C ≤ Tj ≤ 0 °C

Note
28. For the full industrial range, you must employ a temperature sensor user module (FlashTemp) and feed the result to the temperature argument before writing. Refer to the Flash APIs application note Design Aids – Reading and Writing PSoC® Flash – AN2015 for more information.

Packaging Information

This section illustrates the packaging specifications for the CY8C29x66 PSoC device, along with the thermal impedances for each package and the typical package capacitance on crystal pins.

Important Note Emulation tools may require a larger area on the target PCB than the chip's footprint. For a detailed description of the emulation tools' dimensions, refer to the emulator pod drawings at http://www.cypress.com.

Packaging Dimensions

Figure 20. 28-pin PDIP (300 Mils) Package Outline, 51-85014

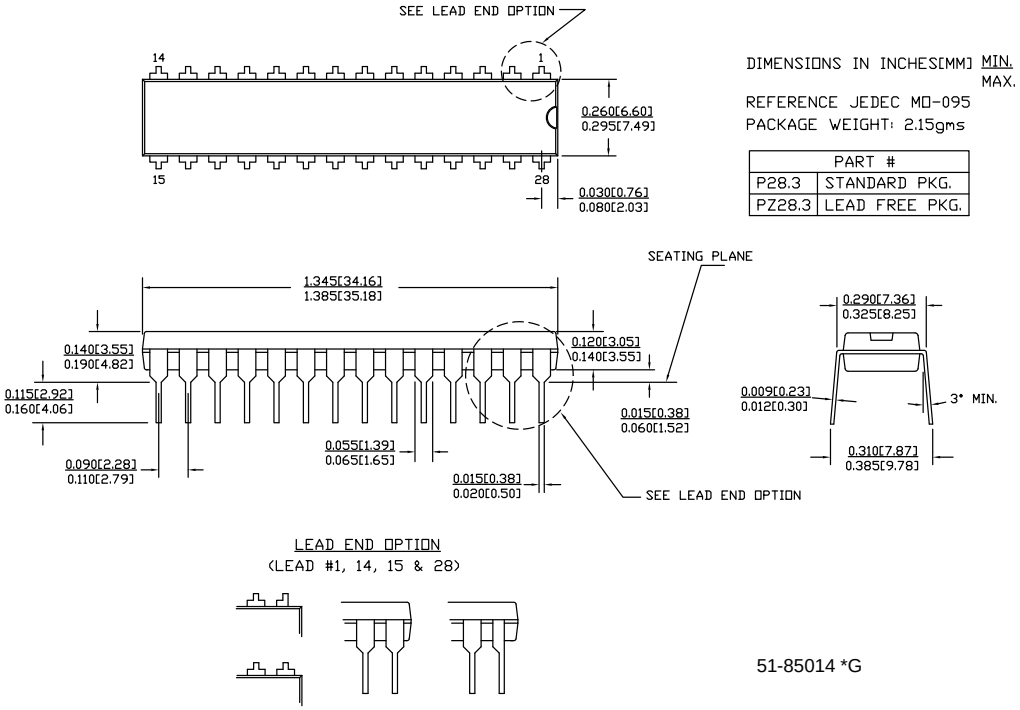


Figure 21. 28-pin SSOP (210 Mils) Package Outline, 51-85079

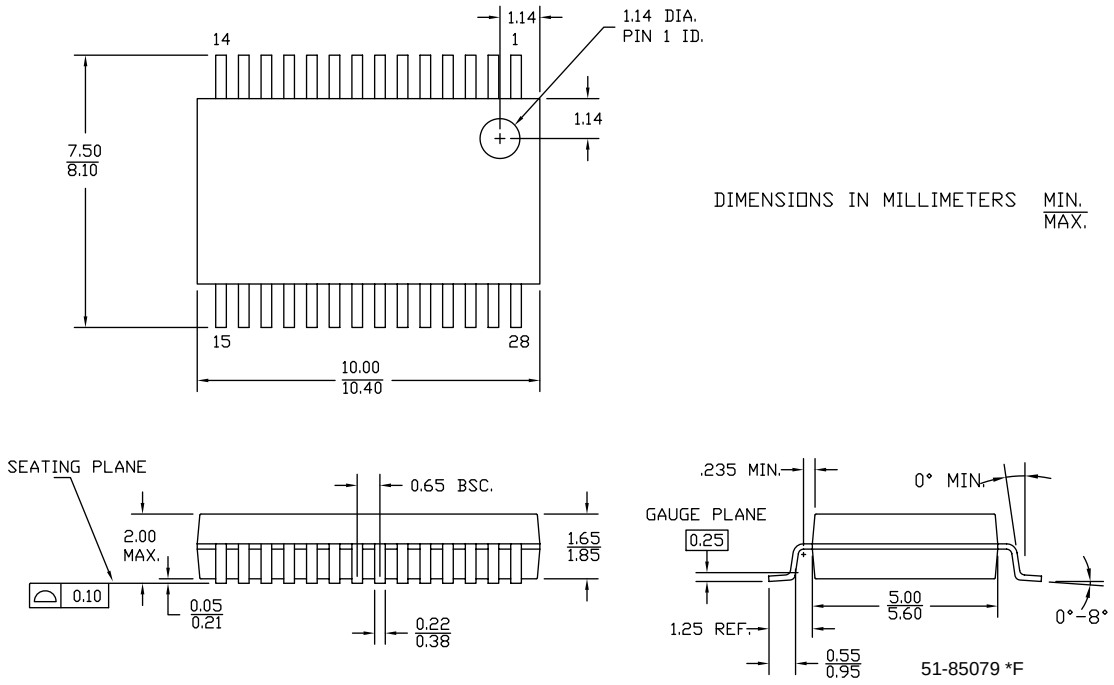


Figure 22. 28-pin SOIC (0.713 × 0.300 × 0.0932 Inches) Package Outline, 51-85026

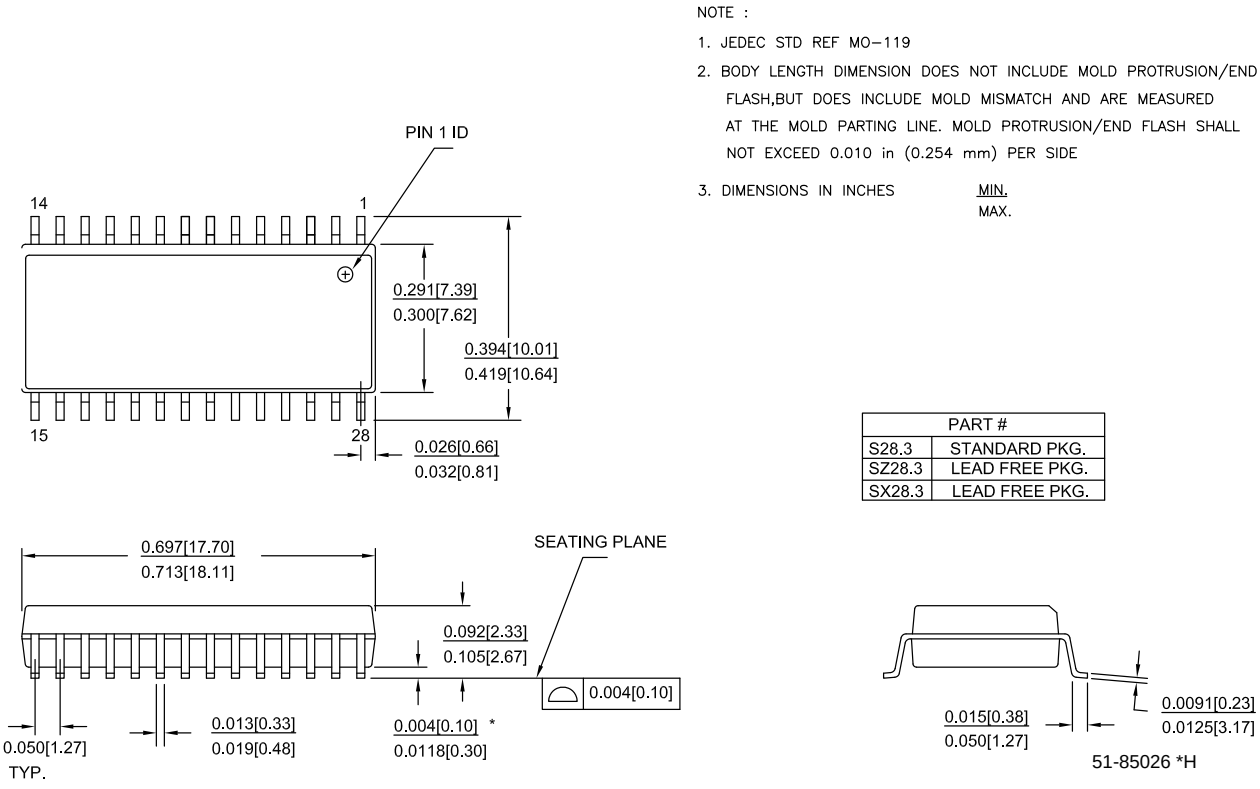


Figure 23. 44-pin TQFP (10 × 10 × 1.4 mm) Package Outline, 51-85064

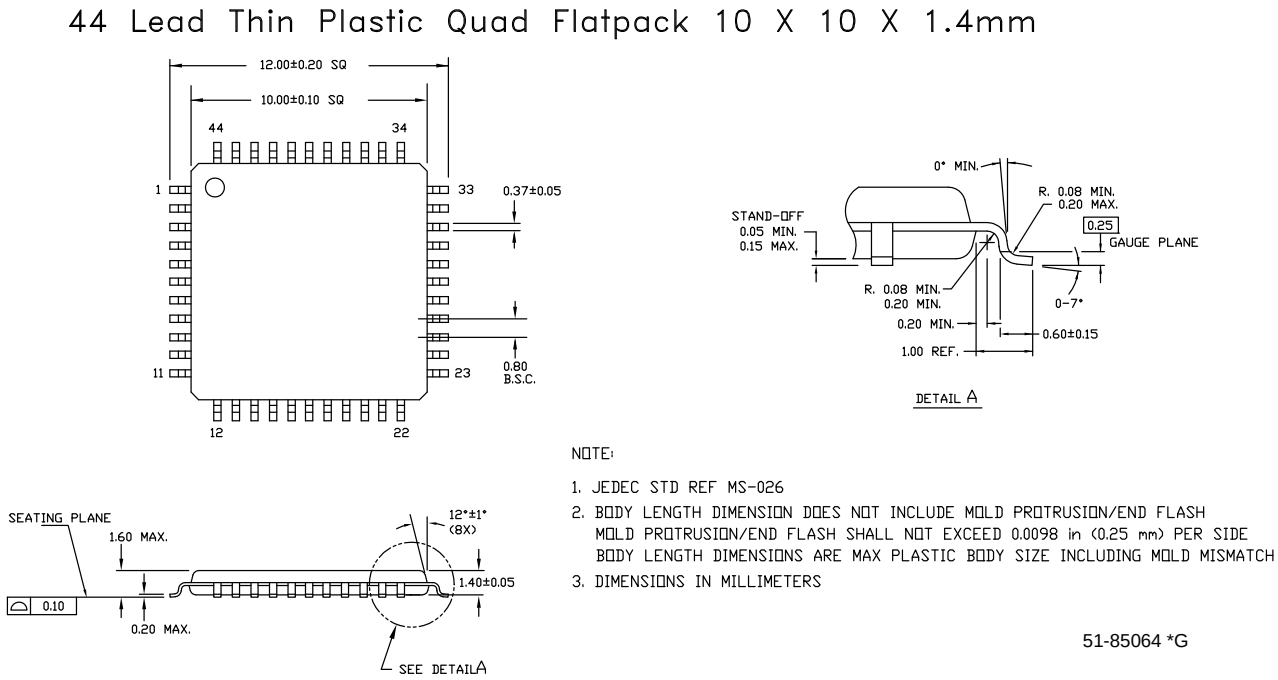
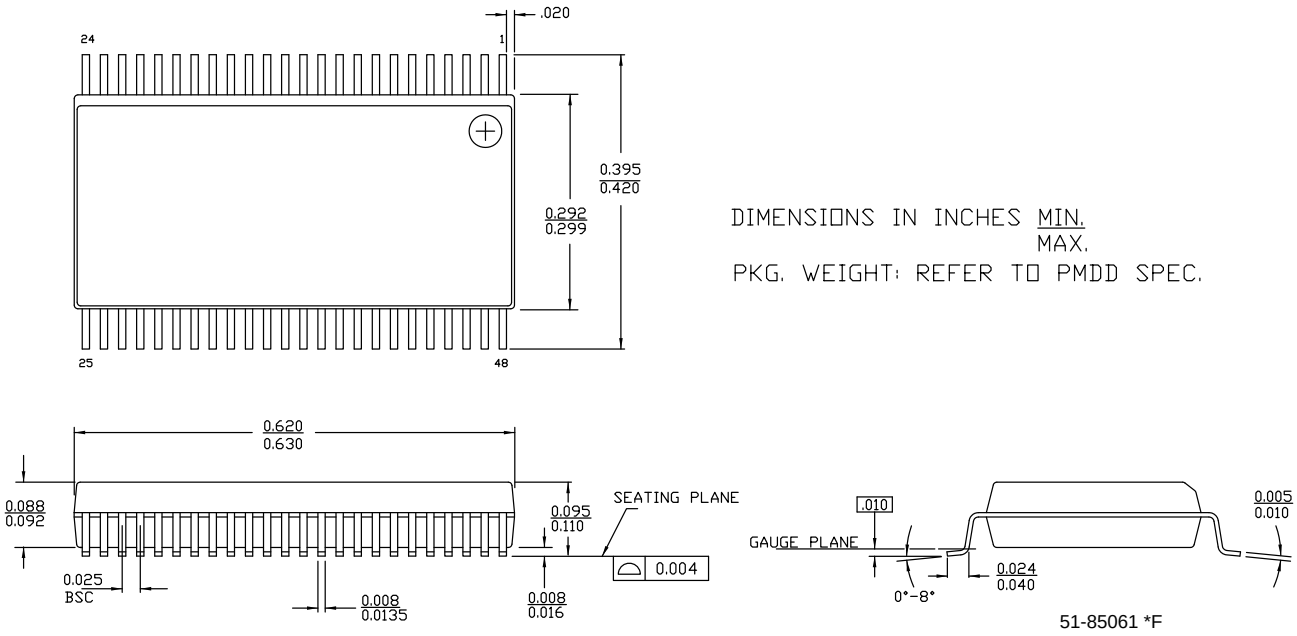


Figure 24. 48-pin SSOP (300 Mils) Package Outline, 51-85061



Document History Page (continued)

Document Title: CY8C29466/CY8C29566/CY8C29666/CY8C29866, PSoC® Programmable System-on-Chip™ Document Number: 38-12013				
Revision	**ECN**	**Origin of Change**	**Submission Date**	**Description of Change**
*V	3991993	PMAD	05/08/2013	Updated Packaging Information: spec 51-85014 – Changed revision from *F to *G. spec 51-85061 – Changed revision from *E to *F. spec 001-13191 – Changed revision from *F to *G. Updated Reference Documents (Removed 001-17397 spec, 001-14503 spec related information). Added Errata.
*W	4081641	PMAD	07/31/2013	Added Errata footnotes (Note 1, 2, 14, 21, 25). Updated Features: Replaced "±2.5%" with "±5%". Added Note 1 and referred the same note in ±5% under "Precision, programmable clocking". Updated PSoC Functional Overview: Updated PSoC Core: Replaced "2.5%" with "5%" in 4th paragraph. Added Note 2 and referred the same note in 5%. Updated Electrical Specifications: Updated DC Electrical Characteristics: Updated DC Chip-Level Specifications: Added Note 14 and referred the same note in V_{DD} parameter. Updated AC Electrical Characteristics: Updated AC Chip-Level Specifications: Added Note 21 and referred the same note in F_{IMO24} parameter in Table 29. Replaced all instances of "24.6" with "25.2" in Table 29. Replaced all instances of "23.4" with "22.8" in Table 29. Replaced all instances of "49.2" with "50.4" in Table 29. Replaced "12.3" with "12.6" for maximum value of F_{CPU2} parameter in Table 29. Replaced "46.8" with "45.6" for minimum value of Fout48M parameter in Table 29. Added Note 25 and referred the same note in $T_{POWERUP}$ parameter in Table 29. Updated AC Digital Block Specifications: Replaced all instances of "49.2" with "50.4" in Table 34. Replaced all instances of "24.6" with "25.2" in Table 34. Updated Packaging Information: spec 51-85026 – Changed revision from *F to *G. spec 51-85048 – Changed revision from *G to *H. Updated Errata. Updated in new template.
*X	4378144	PMAD	05/13/2014	Updated Electrical Specifications: Updated AC Electrical Characteristics: Updated AC External Clock Specifications: Updated Table 37: Changed unit from "ms" to "µs" corresponding to "Power-up IMO to switch". Updated Packaging Information: spec 51-85026 – Changed revision from *G to *H. spec 51-85064 – Changed revision from *E to *F. spec 51-85048 – Changed revision from *H to *I. Completing Sunset Review.

Document History Page (continued)

Document Title: CY8C29466/CY8C29566/CY8C29666/CY8C29866, PSoC® Programmable System-on-Chip™ Document Number: 38-12013				
Revision	**ECN**	**Origin of Change**	**Submission Date**	**Description of Change**
*Y	4461247	ASRI	07/30/2014	Replaced references of “Application Notes for Surface Mount Assembly of Amkor’s MicroLeadFrame (MLF) Packages” with “Design Guidelines for Cypress Quad Flat No Extended Lead (QFN) Packaged Devices – AN72845” in all instances across the document. Added More Information. Added PSoC Designer. Removed “Getting Started”. Updated Electrical Specifications: Updated DC Electrical Characteristics: Updated DC I2C Specifications: Updated Table 28: Replaced V_{OHI2C} with V_{OLI2C}.
*Z	4479512	ASRI / RJVB	09/03/2014	Updated Electrical Specifications: Updated DC Electrical Characteristics: Added DC Analog External Reference Specifications. Updated AC Electrical Characteristics: Updated AC Operational Amplifier Specifications: Updated description. Updated Figure 18. Updated Errata: Updated Errata Summary: Updated details in “Fix Status” column in the table. Updated details in “Fix Status” bulleted point below the table.
AA	4622517	DIMA	01/13/2015	Updated Pinouts: Updated 100-Pin Part Pinout: Updated Table 6: Added Note 10 and referred the same note in description of pin 15, pin 34, pin 65, pin 84 and pin 85. Updated 100-Pin Part Pinout (On-Chip Debug): Updated Table 7: Added Note 12 and referred the same note in description of pin 15, pin 34, pin 65, pin 84 and pin 85. Updated Packaging Information: spec 51-85079 – Changed revision from *E to *F.
AB	4882080	ASRI	08/12/2015	Replaced “Flash pages” with “Flash banks” in all instances across the document. Updated Packaging Information: spec 001-13191 – Changed revision from *G to *H.
AC	5702069	ASRI	04/19/2017	Updated Cypress logo. Updated Copyright. Updated the following Packaging Information: Figure 23 (spec 51-85064 *F to *G) Figure 26 (spec 51-85048 *I to *J)