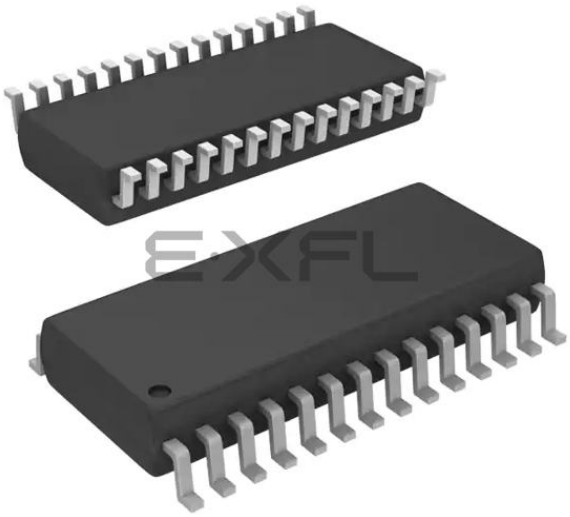


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	M8C
Core Size	8-Bit
Speed	24MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	24
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.25V
Data Converters	A/D 12x14b; D/A 4x9b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c29466-24sxit

More Information

Cypress provides a wealth of data at www.cypress.com to help you to select the right PSoC device for your design, and to help you to quickly and effectively integrate the device into your design. For a comprehensive list of resources, see the knowledge base article "How to Design with PSoC® 1, PowerPSoC®, and PLC – KBA88292". Following is an abbreviated list for PSoC 1:

- Overview: PSoC Portfolio, PSoC Roadmap
- Product Selectors: PSoC 1, PSoC 3, PSoC 4, PSoC 5LP
- In addition, PSoC Designer includes a device selection tool.
- Application notes: Cypress offers a large number of PSoC application notes covering a broad range of topics, from basic to advanced level. Recommended application notes for getting started with PSoC 1 are:
  - Getting Started with PSoC® 1 – AN75320
  - PSoC® 1 - Getting Started with GPIO – AN2094
  - PSoC® 1 Analog Structure and Configuration – AN74170
  - PSoC® 1 Switched Capacitor Analog Blocks – AN2041
  - Selecting Analog Ground and Reference – AN2219

Note: For CY8C29X66 devices related Application note please click here.

- Development Kits:
  - CY3210-PSoCEval1 supports all PSoC 1 Mixed-Signal Array families, including automotive, except CY8C25/26xxx devices. The kit includes an LCD module, potentiometer, LEDs, and breadboarding space.
  - CY3214-PSoCEvalUSB features a development board for the CY8C24x94 PSoC device. Special features of the board include USB and CapSense development and debugging support.

Note: For CY8C29X66 devices related Development Kits please click here.

The MiniProg1 and MiniProg3 devices provide interfaces for flash programming and debug.

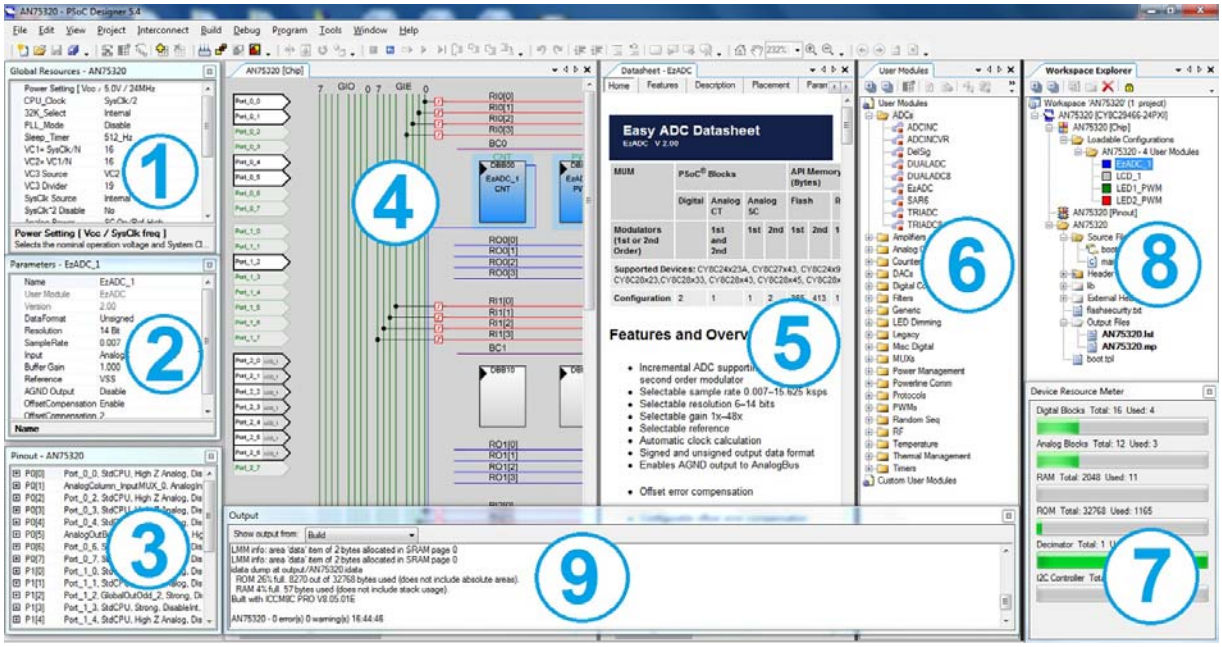
PSoC Designer

PSoC Designer is a free Windows-based Integrated Design Environment (IDE). Develop your applications using a library of pre-characterized analog and digital peripherals in a drag-and-drop design environment. Then, customize your design leveraging the dynamically generated API libraries of code. Figure 1 shows PSoC Designer windows. **Note:** This is not the default view.

1. **Global Resources –** all device hardware settings.
2. **Parameters –** the parameters of the currently selected User Modules.
3. **Pinout –** information related to device pins.
4. **Chip-Level Editor –** a diagram of the resources available on the selected chip.
5. **Datasheet –** the datasheet for the currently selected UM
6. **User Modules –** all available User Modules for the selected device.
7. **Device Resource Meter –** device resource usage for the current project configuration.
8. **Workspace –** a tree level diagram of files associated with the project.
9. **Output –** output from project build and debug operations.

Note: For detailed information on PSoC Designer, go to PSoC® Designer > Help > Documentation > Designer Specific Documents > IDE User Guide.

Figure 1. PSoC Designer Layout



Digital peripheral configurations include:

- PWMs (8- and 16-bit)
- PWMs with dead band (8- and 16-bit)
- Counters (8- to 32-bit)
- Timers (8- to 32-bit)
- UART 8-bit with selectable parity (up to 2)
- SPI slave and master (up to 2)
- I^2C slave and multi-master (one available as a system resource)
- CRC generator (8- to 32-bit)
- IrDA (up to 2)
- PRS generators (8- to 32-bit)

The digital blocks can be connected to any GPIO through a series of global buses that can route any signal to any pin. The buses also allow for signal multiplexing and for performing logic operations. This configurability frees your designs from the constraints of a fixed peripheral controller.

Digital blocks are provided in rows of four, where the number of blocks varies by PSoC device family. This allows you the optimum choice of system resources for your application. Family resources are shown in the table titled “PSoC Device Characteristics” on page 6.

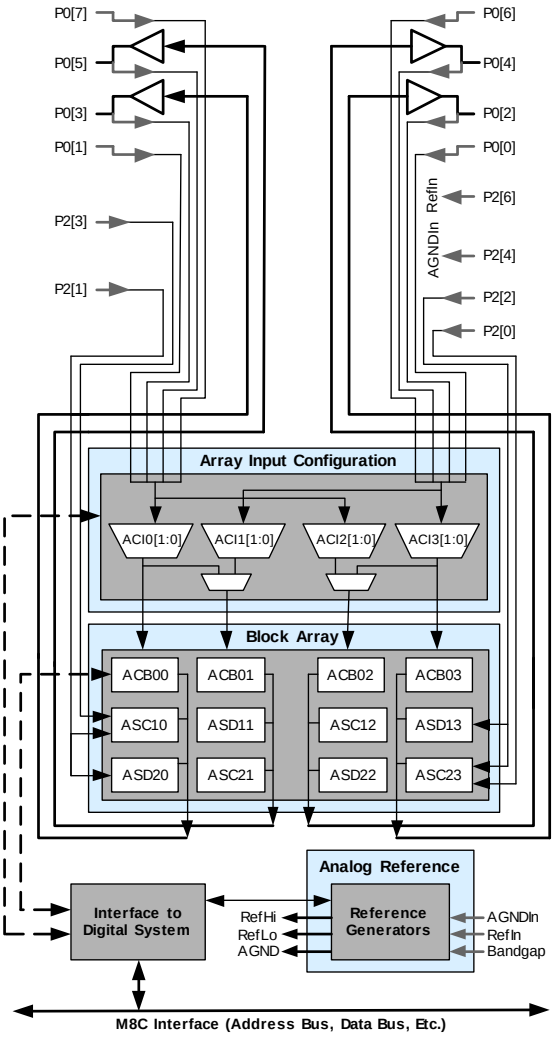
Analog System

The analog system is composed of 12 configurable blocks, each containing an opamp circuit that allows the creation of complex analog signal flows. Analog peripherals are very flexible and can be customized to support specific application requirements. Some of the more common PSoC analog functions (most available as user modules) are:

- ADCs (up to 4, with 6- to 14-bit resolution; selectable as incremental, delta sigma, and SAR)
- Filters (2-, 4-, 6-, and 8-pole band pass, low pass, and notch)
- Amplifiers (up to 4, with selectable gain to 48x)
- Instrumentation amplifiers (up to 2, with selectable gain to 93x)
- Comparators (up to 4, with 16 selectable thresholds)
- DACs (up to 4, with 6-bit to 9-bit resolution)
- Multiplying DACs (up to 4, with 6-bit to 9-bit resolution)
- High current output drivers (four with 30-mA drive as a core resource)
- 1.3-V reference (as a system resource)
- DTMF Dialer
- Modulators
- Correlators
- Peak detectors
- Many other topologies possible

Analog blocks are provided in columns of three, which includes one continuous time (CT) and two switched capacitor (SC) blocks, as shown in Figure 3.

Figure 3. Analog System Block Diagram



Organize and Connect

You build signal chains at the chip level by interconnecting user modules to each other and the I/O pins. You perform the selection, configuration, and routing so that you have complete control over all on-chip resources.

Generate, Verify, and Debug

When you are ready to test the hardware configuration or move on to developing code for the project, you perform the “Generate Configuration Files” step. This causes PSoC Designer to generate source code that automatically configures the device to your specification and provides the software for the system. The generated code provides application programming interfaces (APIs) with high-level functions to control and respond to hardware events at run time and interrupt service routines that you can adapt as needed.

A complete code development environment allows you to develop and customize your applications in either C, assembly language, or both.

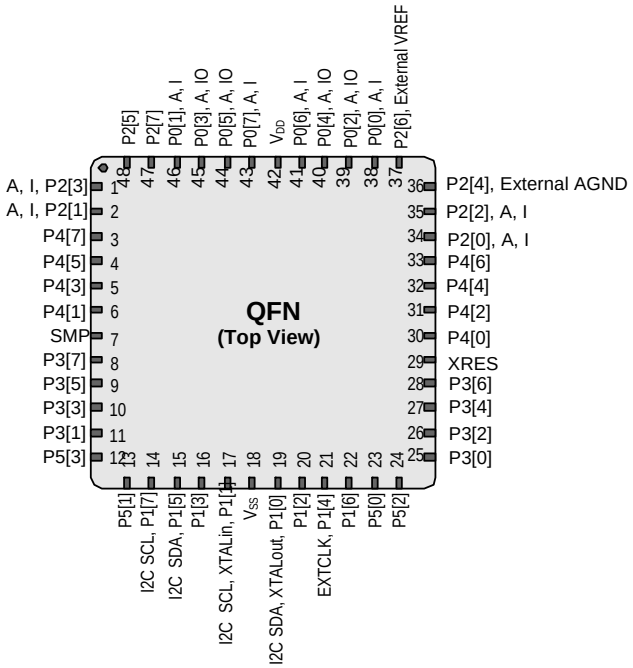
The last step in the development process takes place inside PSoC Designer’s debugger (access by clicking the Connect icon). PSoC Designer downloads the HEX image to the ICE where it runs at full speed. PSoC Designer debugging capabilities rival those of systems costing many times more. In addition to traditional single-step, run-to-breakpoint and watch-variable features, the debug interface provides a large trace buffer and allows you to define complex breakpoint events that include monitoring address and data bus values, memory locations and external signals.

Table 5. 48-Pin Part Pinout (QFN) [9]

Pin No.	Type		Pin Name	Description
	Digital	Analog		
1	I/O	I	P2[3]	Direct switched capacitor block input
2	I/O	I	P2[1]	Direct switched capacitor block input
3	I/O		P4[7]	
4	I/O		P4[5]	
5	I/O		P4[3]	
6	I/O		P4[1]	
7	Power		SMP	Switch mode pump (SMP) connection to external components required
8	I/O		P3[7]	
9	I/O		P3[5]	
10	I/O		P3[3]	
11	I/O		P3[1]	
12	I/O		P5[3]	
13	I/O		P5[1]	
14	I/O		P1[7]	I^2C SCL
15	I/O		P1[5]	I^2C SDA
16	I/O		P1[3]	
17	I/O		P1[1]	Crystal (XTALin), I^2C SCL, ISSP-SCLK[8]
18	Power		V_{SS}	Ground connection
19	I/O		P1[0]	Crystal (XTALout), I^2C SDA, ISSP-SDATA[8]
20	I/O		P1[2]	
21	I/O		P1[4]	Optional EXTCLK
22	I/O		P1[6]	
23	I/O		P5[0]	
24	I/O		P5[2]	
25	I/O		P3[0]	
26	I/O		P3[2]	
27	I/O		P3[4]	
28	I/O		P3[6]	
29	Input		XRES	Active high external reset with internal pull-down
30	I/O		P4[0]	
31	I/O		P4[2]	
32	I/O		P4[4]	
33	I/O		P4[6]	
34	I/O	I	P2[0]	Direct switched capacitor block input
35	I/O	I	P2[2]	Direct switched capacitor block input
36	I/O		P2[4]	External analog ground (AGND)
37	I/O		P2[6]	External voltage reference (VREF)
38	I/O	I	P0[0]	Analog column mux input
39	I/O	I/O	P0[2]	Analog column mux input and column output
40	I/O	I/O	P0[4]	Analog column mux input and column output
41	I/O	I	P0[6]	Analog column mux input
42	Power		V_{DD}	Supply voltage
43	I/O	I	P0[7]	Analog column mux input
44	I/O	I/O	P0[5]	Analog column mux input and column output
45	I/O	I/O	P0[3]	Analog column mux input and column output
46	I/O	I	P0[1]	Analog column mux input
47	I/O		P2[7]	
48	I/O		P2[5]	

LEGEND: A = Analog, I = Input, and O = Output.

Figure 7. CY8C29666 48-Pin PSoC Device



Notes
8. These are the ISSP pins, which are not High Z at POR. See the *PSoC Programmable System-on-Chip Technical Reference Manual* for details.
9. The QFN package has a center pad that must be connected to ground (V_{SS}).

100-Pin Part Pinout

Table 6. 100-Pin Part Pinout (TQFP)

Pin No.	Type		Name	Description	Pin No.	Type		Name	Description
	Digital	Analog				Digital	Analog		
1			NC	No connection. Pin must be left floating	51			NC	No connection. Pin must be left floating
2			NC	No connection. Pin must be left floating	52	I/O		P5[0]	
3	I/O	I	P0[1]	Analog column mux input	53	I/O		P5[2]	
4	I/O		P2[7]		54	I/O		P5[4]	
5	I/O		P2[5]		55	I/O		P5[6]	
6	I/O	I	P2[3]	Direct switched capacitor block input	56	I/O		P3[0]	
7	I/O	I	P2[1]	Direct switched capacitor block input	57	I/O		P3[2]	
8	I/O		P4[7]		58	I/O		P3[4]	
9	I/O		P4[5]		59	I/O		P3[6]	
10	I/O		P4[3]		60			NC	No connection. Pin must be left floating
11	I/O		P4[1]		61			NC	No connection. Pin must be left floating
12			NC	No connection. Pin must be left floating	62	Input		XRES	Active high external reset with internal pull-down
13			NC	No connection. Pin must be left floating	63	I/O		P4[0]	
14	Power		SMP	Switch mode pump (SMP) connection to external components required	64	I/O		P4[2]	
15	Power		V_{SS}	Ground connection [10]	65	Power		V_{SS}	Ground connection [10]
16	I/O		P3[7]		66	I/O		P4[4]	
17	I/O		P3[5]		67	I/O		P4[6]	
18	I/O		P3[3]		68	I/O	I	P2[0]	Direct switched capacitor block input
19	I/O		P3[1]		69	I/O	I	P2[2]	Direct switched capacitor block input
20	I/O		P5[7]		70	I/O		P2[4]	External Analog Ground (AGND)
21	I/O		P5[5]		71			NC	No connection. Pin must be left floating
22	I/O		P5[3]		72	I/O		P2[6]	External Voltage Reference (VREF)
23	I/O		P5[1]		73			NC	No connection. Pin must be left floating
24	I/O		P1[7]	I^2C SCL	74	I/O	I	P0[0]	Analog column mux input
25			NC	No connection. Pin must be left floating	75			NC	No connection. Pin must be left floating
26			NC	No connection. Pin must be left floating	76			NC	No connection. Pin must be left floating
27			NC	No connection. Pin must be left floating	77	I/O	I/O	P0[2]	Analog column mux input and column output
28	I/O		P1[5]	I^2C SDA	78			NC	No connection. Pin must be left floating
29	I/O		P1[3]		79	I/O	I/O	P0[4]	Analog column mux input and column output
30	I/O		P1[1]	Crystal (XTALin), I^2C Serial Clock (SCL), ISSP-SCLK[11]	80			NC	No connection. Pin must be left floating
31			NC	No connection. Pin must be left floating	81	I/O	I	P0[6]	Analog column mux input
32	Power		V_{DD}	Supply voltage	82	Power		V_{DD}	Supply voltage
33			NC	No connection. Pin must be left floating	83	Power		V_{DD}	Supply voltage
34	Power		V_{SS}	Ground connection [10]	84	Power		V_{SS}	Ground connection [10]
35			NC	No connection. Pin must be left floating	85	Power		V_{SS}	Ground connection [10]
36	I/O		P7[7]		86	I/O		P6[0]	
37	I/O		P7[6]		87	I/O		P6[1]	
38	I/O		P7[5]		88	I/O		P6[2]	
39	I/O		P7[4]		89	I/O		P6[3]	
40	I/O		P7[3]		90	I/O		P6[4]	
41	I/O		P7[2]		91	I/O		P6[5]	
42	I/O		P7[1]		92	I/O		P6[6]	
43	I/O		P7[0]		93	I/O		P6[7]	
44	I/O		P1[0]	Crystal (XTALout), I^2C Serial Data (SDA), ISSP-SDATA[11]	94			NC	No connection. Pin must be left floating
45	I/O		P1[2]		95	I/O	I	P0[7]	Analog column mux input
46	I/O		P1[4]	Optional EXTCLK	96			NC	No connection. Pin must be left floating
47	I/O		P1[6]		97	I/O	I/O	P0[5]	Analog column mux input and column output
48			NC	No connection. Pin must be left floating	98			NC	No connection. Pin must be left floating
49			NC	No connection. Pin must be left floating	99	I/O	I/O	P0[3]	Analog column mux input and column output
50			NC	No connection. Pin must be left floating	100			NC	No connection. Pin must be left floating

LEGEND: A = Analog, I = Input, and O = Output.

Notes
10. All V_{SS} pins should be brought out to one common GND plane.
11. These are the ISSP pins, which are not High Z at POR. See the *PSoC Programmable System-on-Chip Technical Reference Manual* for details.

100-Pin Part Pinout (On-Chip Debug)

The 100-pin TQFP part is for the CY8C29000 On-Chip Debug (OCD) PSoC device.

Note OCD parts are only used for in-circuit debugging. OCD parts are NOT available for production.

Table 7. 100-Pin OCD Part Pinout (TQFP)

Pin No.	Digital	Analog	Name	Description	Pin No.	Digital	Analog	Name	Description
1			NC	No internal connection	51			NC	No internal connection
2			NC	No internal connection	52	I/O		P5[0]	
3	I/O	I	P0[1]	Analog column mux input	53	I/O		P5[2]	
4	I/O		P2[7]		54	I/O		P5[4]	
5	I/O		P2[5]		55	I/O		P5[6]	
6	I/O	I	P2[3]	Direct switched capacitor block input	56	I/O		P3[0]	
7	I/O	I	P2[1]	Direct switched capacitor block input	57	I/O		P3[2]	
8	I/O		P4[7]		58	I/O		P3[4]	
9	I/O		P4[5]		59	I/O		P3[6]	
10	I/O		P4[3]		60			HCLK	OCD high speed clock output
11	I/O		P4[1]		61			CCLK	OCD CPU clock output
12			OCDE	OCD even data I/O	62	Input		XRES	Active high pin reset with internal pull-down
13			OCDO	OCD odd data output	63	I/O		P4[0]	
14	Power		SMP	Switch Mode Pump (SMP) connection to required external components	64	I/O		P4[2]	
15	Power		V_{SS}	Ground connection [12]	65	Power		V_{SS}	Ground connection [12]
16	I/O		P3[7]		66	I/O		P4[4]	
17	I/O		P3[5]		67	I/O		P4[6]	
18	I/O		P3[3]		68	I/O	I	P2[0]	Direct switched capacitor block input
19	I/O		P3[1]		69	I/O	I	P2[2]	Direct switched capacitor block input
20	I/O		P5[7]		70	I/O		P2[4]	External Analog Ground (AGND) input
21	I/O		P5[5]		71			NC	No internal connection
22	I/O		P5[3]		72	I/O		P2[6]	External Voltage Reference (VREF) input
23	I/O		P5[1]		73			NC	No internal connection
24	I/O		P1[7]	I^2C SCL	74	I/O	I	P0[0]	Analog column mux input
25			NC	No internal connection	75			NC	No internal connection
26			NC	No internal connection	76			NC	No internal connection
27			NC	No internal connection	77	I/O	I/O	P0[2]	Analog column mux input and column output
28	I/O		P1[5]	I^2C SDA	78			NC	No internal connection
29	I/O		P1[3]	I_{FMTEST}	79	I/O	I/O	P0[4]	Analog column mux input and column output, V_{REF}
30	I/O		P1[1][13]	Crystal (XTALin), I^2C SCL, TC SCLK.	80			NC	No internal connection
31			NC	No internal connection	81	I/O	I	P0[6]	Analog column mux input
32	Power		V_{DD}	Supply voltage	82	Power		V_{DD}	Supply voltage
33			NC	No internal connection	83	Power		V_{DD}	Supply voltage
34	Power		V_{SS}	Ground connection [12]	84	Power		V_{SS}	Ground connection [12]
35			NC	No internal connection	85	Power		V_{SS}	Ground connection [12]
36	I/O		P7[7]		86	I/O		P6[0]	
37	I/O		P7[6]		87	I/O		P6[1]	
38	I/O		P7[5]		88	I/O		P6[2]	
39	I/O		P7[4]		89	I/O		P6[3]	
40	I/O		P7[3]		90	I/O		P6[4]	
41	I/O		P7[2]		91	I/O		P6[5]	
42	I/O		P7[1]		92	I/O		P6[6]	
43	I/O		P7[0]		93	I/O		P6[7]	
44	I/O		P1[0]*	Crystal (XTALout), I^2C SDA, TC SDATA	94			NC	No internal connection
45	I/O		P1[2]	V_{FMTEST}	95	I/O	I	P0[7]	Analog column mux input
46	I/O		P1[4]	Optional External Clock Input (EXTCLK)	96			NC	No internal connection
47	I/O		P1[6]		97	I/O	I/O	P0[5]	Analog column mux input and column output
48			NC	No internal connection	98			NC	No internal connection
49			NC	No internal connection	99	I/O	I/O	P0[3]	Analog column mux input and column output
50			NC	No internal connection	100			NC	No internal connection

LEGEND A = Analog, I = Input, O = Output, NC = No connection. Pin must be left floating, TC/TM: Test.

Notes
12. All V_{SS} pins should be brought out to one common GND plane.
13. ISSP pin which is not High-Z at POR.

Figure 9. CY8C29000 OCD (Not for Production)

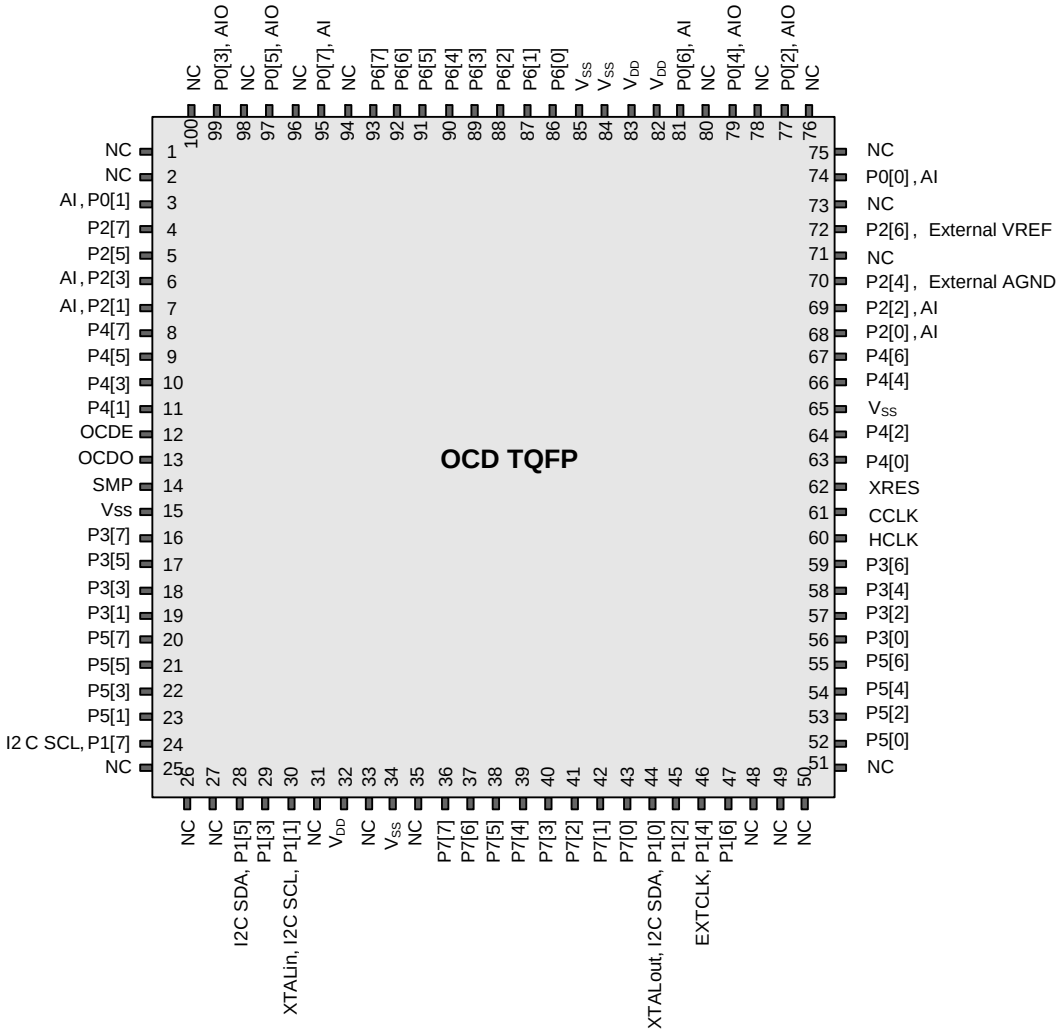


Table 19. 3.3-V DC Analog Output Buffer Specifications

Symbol	Description	Min	Typ	Max	Unit	Notes
V_{OSOB}	Input offset voltage (absolute value) Power = Low, Opamp bias = Low Power = Low, Opamp bias = High Power = High, Opamp bias = Low Power = High, Opamp bias = High	 – – – –	 3.2 3.2 6 6	 20 20 25 25	 mV mV mV mV	High power setting is not recommended.
TCV_{OSOB}	Average input offset voltage drift Power = Low, Opamp bias = Low Power = Low, Opamp bias = High Power = High, Opamp bias = Low Power = High, Opamp bias = High	 – – – –	 8 8 12 12	 32 32 41 41	 µV/°C µV/°C µV/°C µV/°C	High power setting is not recommended.
V_{CMOB}	Common-mode input voltage range	0.5	–	$V_{DD} – 1.0$	V	
R_{OUTOB}	Output resistance Power = Low Power = High	 – –	 – –	 10 10	 W W	
$V_{OHIGHOB}$	High output voltage swing (Load = 32 ohms to $V_{DD}/2$) Power = Low Power = High	 $0.5 \times V_{DD} + 1.0$ $0.5 \times V_{DD} + 1.0$	 – –	 – –	 V V	
V_{OLOWOB}	Low output voltage swing (Load = 32 ohms to $V_{DD}/2$) Power = Low Power = High	 – –	 – –	 $0.5 \times V_{DD} – 1.0$ $0.5 \times V_{DD} – 1.0$	 V V	
I_{SOB}	Supply current including bias cell (no load) Power = Low Power = High	 – –	 0.8 2.0	 1 5	 mA mA	
$PSRR_{OB}$	Supply voltage rejection ratio	60	64	–	dB	
C_L	Load capacitance	–	–	200	pF	This specification applies to the external circuit driven by the analog output buffer.

Table 21. 5-V DC Analog Reference Specifications (continued)

Reference ARF_CR[5:3]	Reference Power Settings	Symbol	Reference	Description	Min	Typ	Max	Unit
0b011	RefPower = High Opamp bias = High	V_{REFHI}	Ref High	3 × Bandgap	3.788	3.891	3.986	V
		V_{AGND}	AGND	2 × Bandgap	2.500	2.604	2.699	V
		V_{REFLO}	Ref Low	Bandgap	1.257	1.306	1.359	V
	RefPower = High Opamp bias = Low	V_{REFHI}	Ref High	3 × Bandgap	3.792	3.893	3.982	V
		V_{AGND}	AGND	2 × Bandgap	2.518	2.602	2.692	V
		V_{REFLO}	Ref Low	Bandgap	1.256	1.302	1.354	V
	RefPower = Med Opamp bias = High	V_{REFHI}	Ref High	3 × Bandgap	3.795	3.894	3.993	V
		V_{AGND}	AGND	2 × Bandgap	2.516	2.603	2.698	V
		V_{REFLO}	Ref Low	Bandgap	1.256	1.303	1.353	V
	RefPower = Med Opamp bias = Low	V_{REFHI}	Ref High	3 × Bandgap	3.792	3.895	3.986	V
		V_{AGND}	AGND	2 × Bandgap	2.522	2.602	2.685	V
		V_{REFLO}	Ref Low	Bandgap	1.255	1.301	1.350	V
0b100	RefPower = High Opamp bias = High	V_{REFHI}	Ref High	2 × Bandgap + P2[6] (P2[6] = 1.3 V)	2.495 + P2[6]	2.586 + P2[6]	2.657 + P2[6]	V
		V_{AGND}	AGND	2 × Bandgap	2.502	2.604	2.719	V
		V_{REFLO}	Ref Low	2 × Bandgap – P2[6] (P2[6] = 1.3 V)	2.531 – P2[6]	2.611 – P2[6]	2.681 – P2[6]	V
	RefPower = High Opamp bias = Low	V_{REFHI}	Ref High	2 × Bandgap + P2[6] (P2[6] = 1.3 V)	2.500 + P2[6]	2.591 + P2[6]	2.662 + P2[6]	V
		V_{AGND}	AGND	2 × Bandgap	2.519	2.602	2.693	V
		V_{REFLO}	Ref Low	2 × Bandgap – P2[6] (P2[6] = 1.3 V)	2.530 – P2[6]	2.605 – P2[6]	2.666 – P2[6]	V
	RefPower = Med Opamp bias = High	V_{REFHI}	Ref High	2 × Bandgap + P2[6] (P2[6] = 1.3 V)	2.503 + P2[6]	2.592 + P2[6]	2.662 + P2[6]	V
		V_{AGND}	AGND	2 × Bandgap	2.517	2.603	2.698	V
		V_{REFLO}	Ref Low	2 × Bandgap – P2[6] (P2[6] = 1.3 V)	2.529 – P2[6]	2.606 – P2[6]	2.665 – P2[6]	V
	RefPower = Med Opamp bias = Low	V_{REFHI}	Ref High	2 × Bandgap + P2[6] (P2[6] = 1.3 V)	2.505 + P2[6]	2.594 + P2[6]	2.665 + P2[6]	V
		V_{AGND}	AGND	2 × Bandgap	2.525	2.602	2.685	V
		V_{REFLO}	Ref Low	2 × Bandgap – P2[6] (P2[6] = 1.3 V)	2.528 – P2[6]	2.603 – P2[6]	2.661 – P2[6]	V

Table 21. 5-V DC Analog Reference Specifications (continued)

Reference ARF_CR[5:3]	Reference Power Settings	Symbol	Reference	Description	Min	Typ	Max	Unit
0b101	RefPower = High Opamp bias = High	V_{REFHI}	Ref High	P2[4] + Bandgap ($P2[4] = V_{DD}/2$)	P2[4] + 1.222	P2[4] + 1.290	P2[4] + 1.343	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4] – Bandgap ($P2[4] = V_{DD}/2$)	P2[4] – 1.331	P2[4] – 1.295	P2[4] – 1.254	V
	RefPower = High Opamp bias = Low	V_{REFHI}	Ref High	P2[4] + Bandgap ($P2[4] = V_{DD}/2$)	P2[4] + 1.226	P2[4] + 1.293	P2[4] + 1.347	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4] – Bandgap ($P2[4] = V_{DD}/2$)	P2[4] – 1.331	P2[4] – 1.298	P2[4] – 1.259	V
	RefPower = Med Opamp bias = High	V_{REFHI}	Ref High	P2[4] + Bandgap ($P2[4] = V_{DD}/2$)	P2[4] + 1.227	P2[4] + 1.294	P2[4] + 1.347	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4] – Bandgap ($P2[4] = V_{DD}/2$)	P2[4] – 1.331	P2[4] – 1.298	P2[4] – 1.259	V
	RefPower = Med Opamp bias = Low	V_{REFHI}	Ref High	P2[4] + Bandgap ($P2[4] = V_{DD}/2$)	P2[4] + 1.228	P2[4] + 1.295	P2[4] + 1.349	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4] – Bandgap ($P2[4] = V_{DD}/2$)	P2[4] – 1.332	P2[4] – 1.299	P2[4] – 1.260	V
0b110	RefPower = High Opamp bias = High	V_{REFHI}	Ref High	2 × Bandgap	2.535	2.598	2.644	V
		V_{AGND}	AGND	Bandgap	1.227	1.305	1.398	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.009	V_{SS} + 0.038	V
	RefPower = High Opamp bias = Low	V_{REFHI}	Ref High	2 × Bandgap	2.530	2.598	2.643	V
		V_{AGND}	AGND	Bandgap	1.244	1.303	1.370	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.005	V_{SS} + 0.024	V
	RefPower = Med Opamp bias = High	V_{REFHI}	Ref High	2 × Bandgap	2.532	2.598	2.644	V
		V_{AGND}	AGND	Bandgap	1.239	1.304	1.380	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.006	V_{SS} + 0.026	V
	RefPower = Med Opamp bias = Low	V_{REFHI}	Ref High	2 × Bandgap	2.528	2.598	2.645	V
		V_{AGND}	AGND	Bandgap	1.249	1.302	1.362	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.004	V_{SS} + 0.018	V
0b111	RefPower = High Opamp bias = High	V_{REFHI}	Ref High	3.2 × Bandgap	4.041	4.155	4.234	V
		V_{AGND}	AGND	1.6 × Bandgap	1.998	2.083	2.183	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.010	V_{SS} + 0.038	V
	RefPower = High Opamp bias = Low	V_{REFHI}	Ref High	3.2 × Bandgap	4.047	4.153	4.236	V
		V_{AGND}	AGND	1.6 × Bandgap	2.012	2.082	2.157	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.006	V_{SS} + 0.024	V
	RefPower = Med Opamp bias = High	V_{REFHI}	Ref High	3.2 × Bandgap	4.049	4.154	4.238	V
		V_{AGND}	AGND	1.6 × Bandgap	2.008	2.083	2.165	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.006	V_{SS} + 0.026	V
	RefPower = Med Opamp bias = Low	V_{REFHI}	Ref High	3.2 × Bandgap	4.047	4.154	4.238	V
		V_{AGND}	AGND	1.6 × Bandgap	2.016	2.081	2.150	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.004	V_{SS} + 0.018	V

DC Analog External Reference Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 23. 5-V DC Analog External Reference Specifications

Reference	Description	Min	Typ	Max	Unit
Ref Low	Ref Low = P2[4] – P2[6] (P2[4] = V_{CC}/2, P2[6] = 1.3 V)	1.12	1.221	1.28	V
AGND	AGND = P2[4] (P2[4] = V_{CC}/2)	2.487	2.499	2.513	V
Ref High	Ref Low = P2[4] + P2[6] (P2[4] = V_{CC}/2, P2[6] = 1.3 V)	3.67	3.759	3.93	V

Table 24. 3.3-V DC Analog External Reference Specifications

Reference	Description	Min	Typ	Max	Unit
Ref Low	Ref Low = P2[4] – P2[6] (P2[4] = V_{CC}/2, P2[6] = 1.3 V)	0.29	0.371	0.41	V
AGND	AGND = P2[4] (P2[4] = V_{CC}/2)	1.642	1.649	1.658	V
Ref High	Ref Low = P2[4] + P2[6] (P2[4] = V_{CC}/2, P2[6] = 1.3 V)	–	2.916	–	V

DC Analog PSoC Block Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 25. DC Analog PSoC Block Specifications

Symbol	Description	Min	Typ	Max	Unit	Notes
R_{CT}	Resistor unit value (continuous time)	–	12.2	–	kΩ	
C_{SC}	Capacitor unit value (switch cap)	–	80	–	fF	

Table 32. 3.3-V AC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units
t_{ROA}	Rising settling time to 0.1% of a 1 V Step (10 pF load, unity gain) Power = Low, Opamp bias = Low Power = Medium, Opamp bias = High	 – –	 – –	 3.92 0.72	 µs µs
t_{SOA}	Falling settling time to 0.1% of a 1 V Step (10 pF load, unity gain) Power = Low, Opamp bias = Low Power = Medium, Opamp bias = High	 – –	 – –	 5.41 0.72	 µs µs
SR_{ROA}	Rising slew rate (20% to 80%) of a 1 V Step (10 pF load, unity gain) Power = Low, Opamp bias = Low Power = Medium, Opamp bias = High	 0.31 2.7	 – –	 – –	 V/µs V/µs
SR_{FOA}	Falling slew rate (20% to 80%) of a 1 V Step (10 pF load, unity gain) Power = Low, Opamp bias = Low Power = Medium, Opamp bias = High	 0.24 1.8	 – –	 – –	 V/µs V/µs
BW_{OA}	Gain bandwidth product Power = Low, Opamp bias = Low Power = Medium, Opamp bias = High	0.67 2.8	– –	– –	MHz MHz
E_{NOA}	Noise at 1 kHz (Power = Medium, Opamp bias = High)	–	100	–	nV/rt-Hz

Figure 17. Typical Opamp Noise

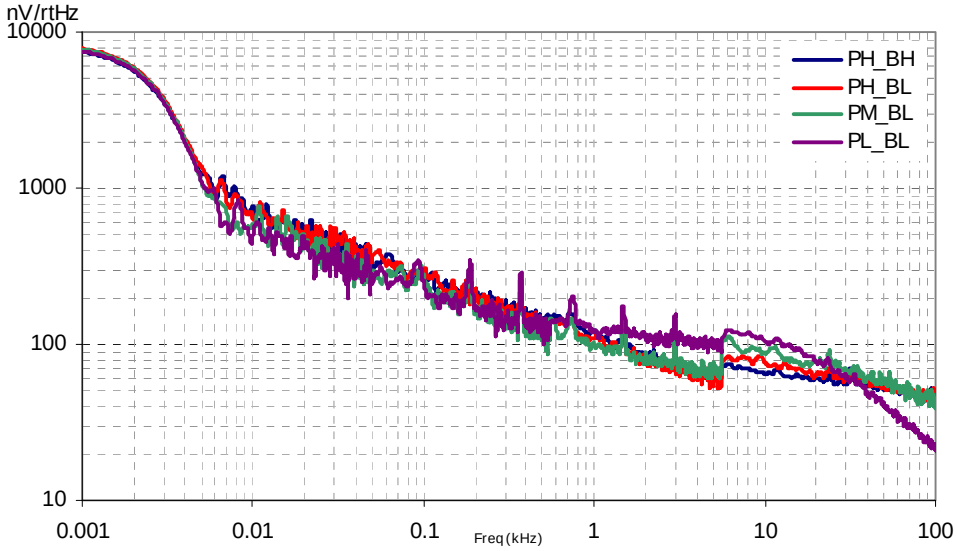


Table 38. 3.3-V AC External Clock Specifications

Symbol	Description	Min	Typ	Max	Unit
F_{OSCEXT}	Frequency with CPU clock divide by 1	0.093	–	12.3	MHz
F_{OSCEXT}	Frequency with CPU clock divide by 2 or greater	0.186	–	24.6	MHz
–	High period with CPU clock divide by 1	41.7	–	5300	ns
–	Low period with CPU clock divide by 1	41.7	–	–	ns
–	Power-up IMO to switch	150	–	–	µs

AC Programming Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 39. AC Programming Specifications

Symbol	Description	Min	Typ	Max	Unit	Notes
t_{RSCLK}	Rise time of SCLK	1	–	20	ns	–
t_{FSCLK}	Fall time of SCLK	1	–	20	ns	–
t_{SSCLK}	Data setup time to falling edge of SCLK	40	–	–	ns	–
t_{HSCLK}	Data hold time from falling edge of SCLK	40	–	–	ns	–
F_{SCLK}	Frequency of SCLK	0	–	8	MHz	–
t_{ERASEB}	Flash erase time (block)	–	10	–	ms	–
t_{WRITE}	Flash block write time	–	40	–	ms	–
t_{DSCLK}	Data out delay from falling edge of SCLK	–	–	45	ns	$V_{DD} > 3.6$
t_{DSCLK3}	Data out delay from falling edge of SCLK	–	–	50	ns	$3.0 \le V_{DD} \le 3.6$
$t_{ERASEALL}$	Flash erase time (Bulk)	–	80	–	ms	Erase all blocks and protection fields at once
$t_{PROGRAM\_HOT}$	Flash block erase + Flash block write time	–	–	100[28]	ms	0 °C ≤ Tj ≤ 100 °C
$t_{PROGRAM\_COLD}$	Flash block erase + Flash block write time	–	–	200[28]	ms	–40 °C ≤ Tj ≤ 0 °C

Note
28. For the full industrial range, you must employ a temperature sensor user module (FlashTemp) and feed the result to the temperature argument before writing. Refer to the Flash APIs application note Design Aids – Reading and Writing PSoC® Flash – AN2015 for more information.

Figure 25. 48-pin QFN (7 × 7 × 1.0 mm) 5.1 × 5.1 E-Pad (Sawn) Package Outline, 001-13191

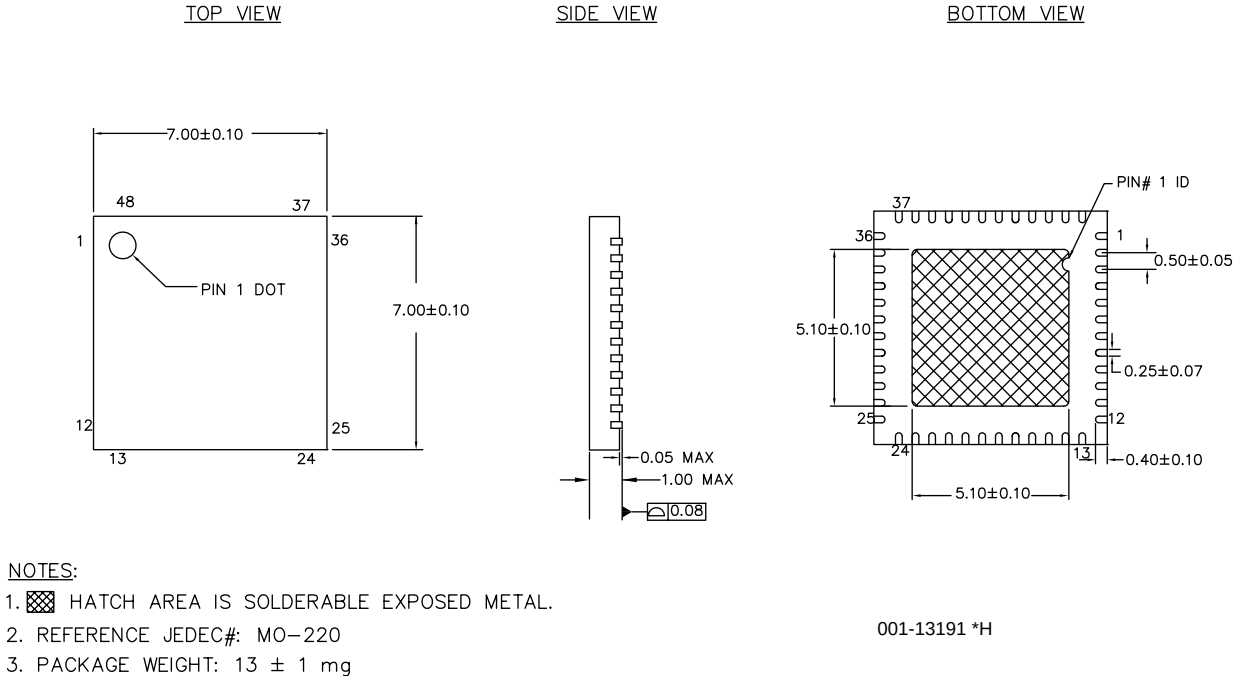
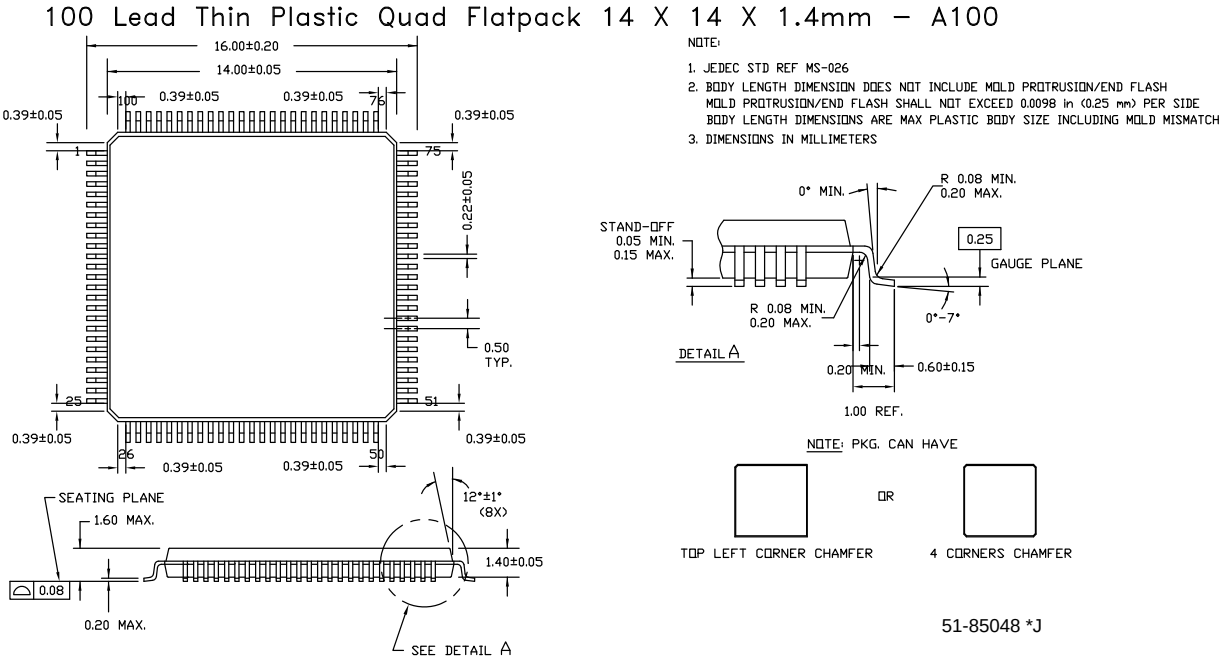


Figure 26. 100-pin TQFP (14 × 14 × 1.4 mm) Package Outline, 51-85048



Important Note For information on the preferred dimensions for mounting the QFN packages, see the application note *Design Guidelines for Cypress Quad Flat No Extended Lead (QFN) Packaged Devices – AN72845* available at http://www.cypress.com.

Important Note Pinned vias for thermal conduction are not required for the low-power PSoC device.

Thermal Impedances

Table 41. Thermal Impedances per Package

Package	Typical θ_{JA}[30]
28-pin PDIP	69 °C/W
28-pin SSOP	94 °C/W
28-pin SOIC	67 °C/W
44-pin TQFP	60 °C/W
48-pin SSOP	69 °C/W
48-pin QFN[31]	28 °C/W
100-pin TQFP	50 °C/W

Capacitance on Crystal Pins

Table 42. Typical Package Capacitance on Crystal Pins

Package	Package Capacitance
28-pin PDIP	3.5 pF
28-pin SSOP	2.8 pF
28-pin SOIC	2.7 pF
44-pin TQFP	2.6 pF
48-pin SSOP	3.3 pF
48-pin QFN	1.8 pF
100-pin TQFP	3.1 pF

Solder Reflow Specifications

Table 43 shows the solder reflow temperature limits that must not be exceeded.

Table 43. Solder Reflow Specifications

Package	Maximum Peak Temperature (T_C)	Maximum Time above T_C – 5 °C
28-pin PDIP	260 °C	30 seconds
28-pin SSOP	260 °C	30 seconds
28-pin SOIC	260 °C	30 seconds
44-pin TQFP	260 °C	30 seconds
48-pin SSOP	260 °C	30 seconds
48-pin QFN	260 °C	30 seconds
100-pin TQFP	260 °C	30 seconds

Notes
30. $T_J = T_A + POWER \times \theta_{JA}$.
31. To achieve the thermal impedance specified for the QFN package, refer to the application note *Design Guidelines for Cypress Quad Flat No Extended Lead (QFN) Packaged Devices – AN72845* available at http://www.cypress.com.

Development Tool Selection

This section presents the development tools available for all current PSoC device families including the CY8C29x66 family.

Software

PSoC Designer™

At the core of the PSoC development software suite is PSoC Designer, used to generate PSoC firmware applications. PSoC Designer is available free of charge at http://www.cypress.com and includes a free C compiler.

PSoC Programmer

Flexible enough to be used on the bench in development, yet suitable for factory programming, PSoC Programmer works either as a standalone programming application or it can operate directly from PSoC Designer or PSoC Express. PSoC Programmer software is compatible with both PSoC ICE-Cube In-Circuit Emulator and PSoC MiniProg. PSoC programmer is available free of charge at http://www.cypress.com.

Development Kits

All development kits can be purchased from the Cypress Online Store.

CY3215-DK Basic Development Kit

The CY3215-DK is for prototyping and development with PSoC Designer. This kit supports in-circuit emulation and the software interface allows users to run, halt, and single step the processor and view the content of specific memory locations. Advance emulation features also supported through PSoC Designer. The kit includes:

- PSoC Designer software CD
- ICE-Cube In-Circuit Emulator
- ICE Flex-Pod for CY8C29x66 family
- Cat-5 adapter
- Mini-Eval programming board
- 110 ~ 240 V power supply, Euro-Plug adapter
- iMAGEcraft C compiler
- ISSP cable
- USB 2.0 cable and Blue Cat-5 cable
- Two CY8C29466-24PXI 28-PDIP chip samples

Evaluation Tools

All evaluation tools can be purchased from the Cypress online store.

CY3210-MiniProg1

The CY3210-MiniProg1 kit allows a user to program PSoC devices via the MiniProg1 programming unit. The MiniProg is a small, compact prototyping programmer that connects to the PC via a provided USB 2.0 cable. The kit includes:

- MiniProg programming unit
- MiniEval socket programming and evaluation board
- 28-pin CY8C29466-24PXI PDIP PSoC device sample
- 28-pin CY8C27443-24PXI PDIP PSoC device sample
- PSoC Designer software CD
- Getting Started guide
- USB 2.0 cable

CY3210-PSoCEval1

The CY3210-PSoCEval1 kit features an evaluation board and the MiniProg1 programming unit. The evaluation board includes an LCD module, potentiometer, LEDs, and plenty of bread-boarding space to meet all of your evaluation needs. The kit includes:

- Evaluation board with LCD module
- MiniProg programming unit
- 28-Pin CY8C29466-24PXI PDIP PSoC Device Sample (2)
- PSoC Designer software CD
- Getting Started guide
- USB 2.0 cable

CY3214-PSoCEvalUSB

The CY3214-PSoCEvalUSB evaluation kit features a development board for the CY8C24794-24LFXI PSoC device. Special features of the board include both USB and capacitive sensing development and debugging support. This evaluation board also includes an LCD module, potentiometer, LEDs, an enunciator and plenty of bread boarding space to meet all of your evaluation needs. The kit includes:

- PSoCEvalUSB board
- LCD module
- MIniProg programming unit
- Mini USB cable
- PSoC Designer and example projects CD
- Getting Started guide
- Wire pack

Glossary (continued)

bias	1. A systematic deviation of a value from a reference value. 2. The amount by which the average of a set of values departs from a reference value. 3. The electrical, mechanical, magnetic, or other force (field) applied to a device to establish a reference level to operate the device.
block	1. A functional unit that performs a single function, such as an oscillator. 2. A functional unit that may be configured to perform one of several functions, such as a digital PSoC block or an analog PSoC block.
buffer	1. A storage area for data that is used to compensate for a speed difference, when transferring data from one device to another. Usually refers to an area reserved for IO operations, into which data is read, or from which data is written. 2. A portion of memory set aside to store data, often before it is sent to an external device or as it is received from an external device. 3. An amplifier used to lower the output impedance of a system.
bus	1. A named connection of nets. Bundling nets together in a bus makes it easier to route nets with similar routing patterns. 2. A set of signals performing a common function and carrying similar data. Typically represented using vector notation; for example, address[7:0]. 3. One or more conductors that serve as a common connection for a group of related devices.
clock	The device that generates a periodic signal with a fixed frequency and duty cycle. A clock is sometimes used to synchronize different logic blocks.
comparator	An electronic circuit that produces an output voltage or current whenever two input levels simultaneously satisfy predetermined amplitude requirements.
compiler	A program that translates a high level language, such as C, into machine language.
configuration space	In PSoC devices, the register space accessed when the XIO bit, in the CPU_F register, is set to ‘1’.
crystal oscillator	An oscillator in which the frequency is controlled by a piezoelectric crystal. Typically a piezoelectric crystal is less sensitive to ambient temperature than other circuit components.
cyclic redundancy check (CRC)	A calculation used to detect errors in data communications, typically performed using a linear feedback shift register. Similar calculations may be used for a variety of other purposes such as data compression.
data bus	A bi-directional set of signals used by a computer to convey information from a memory location to the central processing unit and vice versa. More generally, a set of signals used to convey data between digital functions.
debugger	A hardware and software system that allows you to analyze the operation of the system under development. A debugger usually allows the developer to step through the firmware one step at a time, set break points, and analyze memory.
dead band	A period of time when neither of two or more signals are in their active state or in transition.
digital blocks	The 8-bit logic blocks that can act as a counter, timer, serial receiver, serial transmitter, CRC generator, pseudo-random number generator, or SPI.
digital-to-analog (DAC)	A device that changes a digital signal to an analog signal of corresponding magnitude. The analog-to-digital (ADC) converter performs the reverse operation.

Document History Page

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Revision	**ECN**	**Origin of Change**	**Submission Date**	**Description of Change**
**	131151	New Silicon	11/13/2003	New document (Revision **).
*A	132848	NWJ	01/21/2004	New information. First edition of preliminary datasheet.
*B	133205	NWJ	01/27/2004	Changed part numbers, increased SRAM data storage to 2 K bytes.
*C	133656	SFV	02/09/2004	Changed part numbers and removed a 28-pin SOIC.
*D	227240	SFV		Changes to Overview section, 48-pin MLF pinout, and significant changes to the Electrical Specs.
*E	240108	SFV	See ECN	Added a 28-lead (300 mil) SOIC part.
*F	247492	SFV	See ECN	New information added to the Electrical Specifications chapter.
*G	288849	HMT	See ECN	Add DS standards, update device table, fine-tune pinouts, add Reflow Peak Temp. table. Finalize.
*H	722736	HMT	See ECN	Add QFN package clarifications. Add new QFN diagram. Add Low Power Comparator (LPC) AC/DC electrical spec. tables. Add CY8C20x34 to PSoC Device Characteristics table. Update emulation pod/feet kit part numbers. Add OCD non-production pinouts and package diagrams. Add ISSP note to pinout tables. Update package diagram revisions. Update typical and recommended Storage Temperature per industrial specs. Update CY branding and QFN convention. Add new Dev. Tool section. Update copyright and trademarks.
*I	2503350	DFK / PYRS	See ECN	Pinout for CY8C29000 OCD wrongly included details of CY8C24X94. The correct pinout for CY8C29000 is included in this version. Added note on digital signaling in “DC Analog Reference Specifications” section.
*J	2545030	YARA	07/29/08	Added note to Ordering Information
*K	2708295	JVY	04/22/2009	Changed title from “CY8C29466, CY8C29566, CY8C29666, and CY8C29866 PSoC Mixed Signal Array Final datasheet” to “CY8C29466, CY8C29566, CY8C29666, and CY8C29866 PSoC® Programmable System-on-Chip™” Updated to datasheet template Added 48-Pin QFN (Sawn) package diagram and CY8C29666-24LTXI and CY8C29666-24LTXIT part details in the Ordering Information table Updated DC GPIO, AC Chip-Level, and AC Programming Specifications as follows: Modified F_{IMO6} (page 27), T_{WRITE} specifications (page 34) Added I_{OH} (page 21), I_{OL} (page 21), DC_{ILO} (page 28), F_{32K_U} (page 27), $T_{POWERUP}$ (page 28), $T_{ERASEALL}$ (page 34), $T_{PROGRAM\_HOT}$ (page 34), and $T_{PROGRAM\_COLD}$ (page 34) specifications
*L	2761941	DRSW / AESA	09/10/2009	Added SR_{POWER_UP} parameter in AC specs table.
*M	2842762	DRSW	01/08/2010	Corrected Notes for V_{DD} parameter in Table 13, “DC Chip-Level Specifications,” on page 22. Added “Contents” on page 3. Updated links in Sales, Solutions, and Legal Information.

Document History Page (continued)

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Revision	**ECN**	**Origin of Change**	**Submission Date**	**Description of Change**
*Y	4461247	ASRI	07/30/2014	Replaced references of “Application Notes for Surface Mount Assembly of Amkor’s MicroLeadFrame (MLF) Packages” with “Design Guidelines for Cypress Quad Flat No Extended Lead (QFN) Packaged Devices – AN72845” in all instances across the document. Added More Information. Added PSoC Designer. Removed “Getting Started”. Updated Electrical Specifications: Updated DC Electrical Characteristics: Updated DC I2C Specifications: Updated Table 28: Replaced V_{OHI2C} with V_{OLI2C}.
*Z	4479512	ASRI / RJVB	09/03/2014	Updated Electrical Specifications: Updated DC Electrical Characteristics: Added DC Analog External Reference Specifications. Updated AC Electrical Characteristics: Updated AC Operational Amplifier Specifications: Updated description. Updated Figure 18. Updated Errata: Updated Errata Summary: Updated details in “Fix Status” column in the table. Updated details in “Fix Status” bulleted point below the table.
AA	4622517	DIMA	01/13/2015	Updated Pinouts: Updated 100-Pin Part Pinout: Updated Table 6: Added Note 10 and referred the same note in description of pin 15, pin 34, pin 65, pin 84 and pin 85. Updated 100-Pin Part Pinout (On-Chip Debug): Updated Table 7: Added Note 12 and referred the same note in description of pin 15, pin 34, pin 65, pin 84 and pin 85. Updated Packaging Information: spec 51-85079 – Changed revision from *E to *F.
AB	4882080	ASRI	08/12/2015	Replaced “Flash pages” with “Flash banks” in all instances across the document. Updated Packaging Information: spec 001-13191 – Changed revision from *G to *H.
AC	5702069	ASRI	04/19/2017	Updated Cypress logo. Updated Copyright. Updated the following Packaging Information: Figure 23 (spec 51-85064 *F to *G) Figure 26 (spec 51-85048 *I to *J)

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