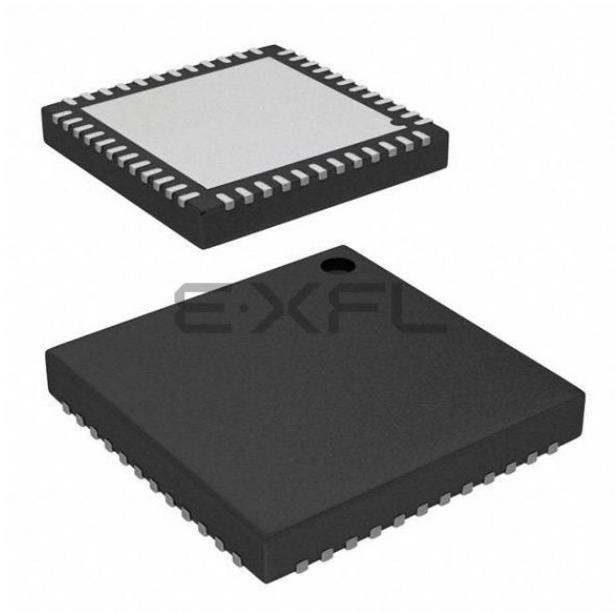

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Details	
Product Status	Active
Core Processor	M8C
Core Size	8-Bit
Speed	24MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	44
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.25V
Data Converters	A/D 12x14b; D/A 4x9b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-VFQFN Exposed Pad
Supplier Device Package	48-QFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c29666-24ltxit

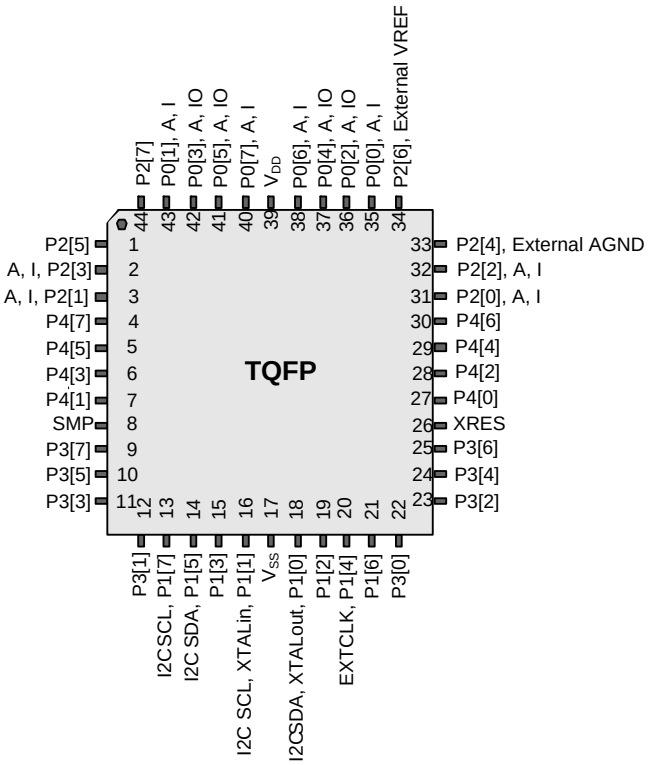
44-Pin Part Pinout

Table 3. 44-Pin Part Pinout (TQFP)

Pin No.	Type		Pin Name	Description
	Digital	Analog		
1	I/O		P2[5]	
2	I/O	I	P2[3]	Direct switched capacitor block input
3	I/O	I	P2[1]	Direct switched capacitor block input
4	I/O		P4[7]	
5	I/O		P4[5]	
6	I/O		P4[3]	
7	I/O		P4[1]	
8	Power		SMP	Switch mode pump (SMP) connection to external components required
9	I/O		P3[7]	
10	I/O		P3[5]	
11	I/O		P3[3]	
12	I/O		P3[1]	
13	I/O		P1[7]	I^2C SCL
14	I/O		P1[5]	I^2C SDA
15	I/O		P1[3]	
16	I/O		P1[1]	Crystal (XTALin), I^2C SCL, ISSP-SCLK[6]
17	Power		V_{SS}	Ground connection
18	I/O		P1[0]	Crystal (XTALout), I^2C SDA, ISSP-SDATA[6]
19	I/O		P1[2]	
20	I/O		P1[4]	Optional EXTCLK
21	I/O		P1[6]	
22	I/O		P3[0]	
23	I/O		P3[2]	
24	I/O		P3[4]	
25	I/O		P3[6]	
26	Input		XRES	Active high external reset with internal pull-down
27	I/O		P4[0]	
28	I/O		P4[2]	
29	I/O		P4[4]	
30	I/O		P4[6]	
31	I/O	I	P2[0]	Direct switched capacitor block input
32	I/O	I	P2[2]	Direct switched capacitor block input
33	I/O		P2[4]	External analog ground (AGND)
34	I/O		P2[6]	External voltage reference (VREF)
35	I/O	I	P0[0]	Analog column mux input
36	I/O	I/O	P0[2]	Analog column mux input and column output
37	I/O	I/O	P0[4]	Analog column mux input and column output
38	I/O	I	P0[6]	Analog column mux input
39	Power		V_{DD}	Supply voltage
40	I/O	I	P0[7]	Analog column mux input
41	I/O	I/O	P0[5]	Analog column mux input and column output
42	I/O	I/O	P0[3]	Analog column mux input and column output
43	I/O	I	P0[1]	Analog column mux input
44	I/O		P2[7]	

LEGEND: A = Analog, I = Input, and O = Output.

Figure 5. CY8C29566 44-Pin PSoC Device



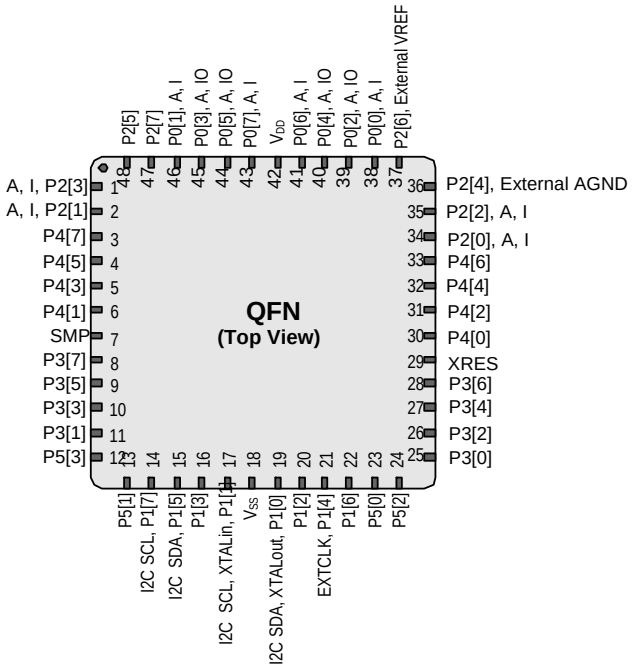
Note
6. These are the ISSP pins, which are not High Z at POR. See the *PSoC Programmable System-on-Chip Technical Reference Manual* for details.

Table 5. 48-Pin Part Pinout (QFN) [9]

Pin No.	Type		Pin Name	Description
	Digital	Analog		
1	I/O	I	P2[3]	Direct switched capacitor block input
2	I/O	I	P2[1]	Direct switched capacitor block input
3	I/O		P4[7]	
4	I/O		P4[5]	
5	I/O		P4[3]	
6	I/O		P4[1]	
7	Power		SMP	Switch mode pump (SMP) connection to external components required
8	I/O		P3[7]	
9	I/O		P3[5]	
10	I/O		P3[3]	
11	I/O		P3[1]	
12	I/O		P5[3]	
13	I/O		P5[1]	
14	I/O		P1[7]	I^2C SCL
15	I/O		P1[5]	I^2C SDA
16	I/O		P1[3]	
17	I/O		P1[1]	Crystal (XTALin), I^2C SCL, ISSP-SCLK[8]
18	Power		V_{SS}	Ground connection
19	I/O		P1[0]	Crystal (XTALout), I^2C SDA, ISSP-SDATA[8]
20	I/O		P1[2]	
21	I/O		P1[4]	Optional EXTCLK
22	I/O		P1[6]	
23	I/O		P5[0]	
24	I/O		P5[2]	
25	I/O		P3[0]	
26	I/O		P3[2]	
27	I/O		P3[4]	
28	I/O		P3[6]	
29	Input		XRES	Active high external reset with internal pull-down
30	I/O		P4[0]	
31	I/O		P4[2]	
32	I/O		P4[4]	
33	I/O		P4[6]	
34	I/O	I	P2[0]	Direct switched capacitor block input
35	I/O	I	P2[2]	Direct switched capacitor block input
36	I/O		P2[4]	External analog ground (AGND)
37	I/O		P2[6]	External voltage reference (VREF)
38	I/O	I	P0[0]	Analog column mux input
39	I/O	I/O	P0[2]	Analog column mux input and column output
40	I/O	I/O	P0[4]	Analog column mux input and column output
41	I/O	I	P0[6]	Analog column mux input
42	Power		V_{DD}	Supply voltage
43	I/O	I	P0[7]	Analog column mux input
44	I/O	I/O	P0[5]	Analog column mux input and column output
45	I/O	I/O	P0[3]	Analog column mux input and column output
46	I/O	I	P0[1]	Analog column mux input
47	I/O		P2[7]	
48	I/O		P2[5]	

LEGEND: A = Analog, I = Input, and O = Output.

Figure 7. CY8C29666 48-Pin PSoC Device



Notes
8. These are the ISSP pins, which are not High Z at POR. See the *PSoC Programmable System-on-Chip Technical Reference Manual* for details.
9. The QFN package has a center pad that must be connected to ground (V_{SS}).

100-Pin Part Pinout

Table 6. 100-Pin Part Pinout (TQFP)

Pin No.	Type		Name	Description	Pin No.	Type		Name	Description
	Digital	Analog				Digital	Analog		
1			NC	No connection. Pin must be left floating	51			NC	No connection. Pin must be left floating
2			NC	No connection. Pin must be left floating	52	I/O		P5[0]	
3	I/O	I	P0[1]	Analog column mux input	53	I/O		P5[2]	
4	I/O		P2[7]		54	I/O		P5[4]	
5	I/O		P2[5]		55	I/O		P5[6]	
6	I/O	I	P2[3]	Direct switched capacitor block input	56	I/O		P3[0]	
7	I/O	I	P2[1]	Direct switched capacitor block input	57	I/O		P3[2]	
8	I/O		P4[7]		58	I/O		P3[4]	
9	I/O		P4[5]		59	I/O		P3[6]	
10	I/O		P4[3]		60			NC	No connection. Pin must be left floating
11	I/O		P4[1]		61			NC	No connection. Pin must be left floating
12			NC	No connection. Pin must be left floating	62	Input		XRES	Active high external reset with internal pull-down
13			NC	No connection. Pin must be left floating	63	I/O		P4[0]	
14	Power		SMP	Switch mode pump (SMP) connection to external components required	64	I/O		P4[2]	
15	Power		V_{SS}	Ground connection [10]	65	Power		V_{SS}	Ground connection [10]
16	I/O		P3[7]		66	I/O		P4[4]	
17	I/O		P3[5]		67	I/O		P4[6]	
18	I/O		P3[3]		68	I/O	I	P2[0]	Direct switched capacitor block input
19	I/O		P3[1]		69	I/O	I	P2[2]	Direct switched capacitor block input
20	I/O		P5[7]		70	I/O		P2[4]	External Analog Ground (AGND)
21	I/O		P5[5]		71			NC	No connection. Pin must be left floating
22	I/O		P5[3]		72	I/O		P2[6]	External Voltage Reference (VREF)
23	I/O		P5[1]		73			NC	No connection. Pin must be left floating
24	I/O		P1[7]	I^2C SCL	74	I/O	I	P0[0]	Analog column mux input
25			NC	No connection. Pin must be left floating	75			NC	No connection. Pin must be left floating
26			NC	No connection. Pin must be left floating	76			NC	No connection. Pin must be left floating
27			NC	No connection. Pin must be left floating	77	I/O	I/O	P0[2]	Analog column mux input and column output
28	I/O		P1[5]	I^2C SDA	78			NC	No connection. Pin must be left floating
29	I/O		P1[3]		79	I/O	I/O	P0[4]	Analog column mux input and column output
30	I/O		P1[1]	Crystal (XTALin), I^2C Serial Clock (SCL), ISSP-SCLK[11]	80			NC	No connection. Pin must be left floating
31			NC	No connection. Pin must be left floating	81	I/O	I	P0[6]	Analog column mux input
32	Power		V_{DD}	Supply voltage	82	Power		V_{DD}	Supply voltage
33			NC	No connection. Pin must be left floating	83	Power		V_{DD}	Supply voltage
34	Power		V_{SS}	Ground connection [10]	84	Power		V_{SS}	Ground connection [10]
35			NC	No connection. Pin must be left floating	85	Power		V_{SS}	Ground connection [10]
36	I/O		P7[7]		86	I/O		P6[0]	
37	I/O		P7[6]		87	I/O		P6[1]	
38	I/O		P7[5]		88	I/O		P6[2]	
39	I/O		P7[4]		89	I/O		P6[3]	
40	I/O		P7[3]		90	I/O		P6[4]	
41	I/O		P7[2]		91	I/O		P6[5]	
42	I/O		P7[1]		92	I/O		P6[6]	
43	I/O		P7[0]		93	I/O		P6[7]	
44	I/O		P1[0]	Crystal (XTALout), I^2C Serial Data (SDA), ISSP-SDATA[11]	94			NC	No connection. Pin must be left floating
45	I/O		P1[2]		95	I/O	I	P0[7]	Analog column mux input
46	I/O		P1[4]	Optional EXTCLK	96			NC	No connection. Pin must be left floating
47	I/O		P1[6]		97	I/O	I/O	P0[5]	Analog column mux input and column output
48			NC	No connection. Pin must be left floating	98			NC	No connection. Pin must be left floating
49			NC	No connection. Pin must be left floating	99	I/O	I/O	P0[3]	Analog column mux input and column output
50			NC	No connection. Pin must be left floating	100			NC	No connection. Pin must be left floating

LEGEND: A = Analog, I = Input, and O = Output.

Notes
10. All V_{SS} pins should be brought out to one common GND plane.
11. These are the ISSP pins, which are not High Z at POR. See the *PSoC Programmable System-on-Chip Technical Reference Manual* for details.

100-Pin Part Pinout (On-Chip Debug)

The 100-pin TQFP part is for the CY8C29000 On-Chip Debug (OCD) PSoC device.

Note OCD parts are only used for in-circuit debugging. OCD parts are NOT available for production.

Table 7. 100-Pin OCD Part Pinout (TQFP)

Pin No.	Digital	Analog	Name	Description	Pin No.	Digital	Analog	Name	Description
1			NC	No internal connection	51			NC	No internal connection
2			NC	No internal connection	52	I/O		P5[0]	
3	I/O	I	P0[1]	Analog column mux input	53	I/O		P5[2]	
4	I/O		P2[7]		54	I/O		P5[4]	
5	I/O		P2[5]		55	I/O		P5[6]	
6	I/O	I	P2[3]	Direct switched capacitor block input	56	I/O		P3[0]	
7	I/O	I	P2[1]	Direct switched capacitor block input	57	I/O		P3[2]	
8	I/O		P4[7]		58	I/O		P3[4]	
9	I/O		P4[5]		59	I/O		P3[6]	
10	I/O		P4[3]		60			HCLK	OCD high speed clock output
11	I/O		P4[1]		61			CCLK	OCD CPU clock output
12			OCDE	OCD even data I/O	62	Input		XRES	Active high pin reset with internal pull-down
13			OCDO	OCD odd data output	63	I/O		P4[0]	
14	Power		SMP	Switch Mode Pump (SMP) connection to required external components	64	I/O		P4[2]	
15	Power		V_{SS}	Ground connection [12]	65	Power		V_{SS}	Ground connection [12]
16	I/O		P3[7]		66	I/O		P4[4]	
17	I/O		P3[5]		67	I/O		P4[6]	
18	I/O		P3[3]		68	I/O	I	P2[0]	Direct switched capacitor block input
19	I/O		P3[1]		69	I/O	I	P2[2]	Direct switched capacitor block input
20	I/O		P5[7]		70	I/O		P2[4]	External Analog Ground (AGND) input
21	I/O		P5[5]		71			NC	No internal connection
22	I/O		P5[3]		72	I/O		P2[6]	External Voltage Reference (VREF) input
23	I/O		P5[1]		73			NC	No internal connection
24	I/O		P1[7]	I^2C SCL	74	I/O	I	P0[0]	Analog column mux input
25			NC	No internal connection	75			NC	No internal connection
26			NC	No internal connection	76			NC	No internal connection
27			NC	No internal connection	77	I/O	I/O	P0[2]	Analog column mux input and column output
28	I/O		P1[5]	I^2C SDA	78			NC	No internal connection
29	I/O		P1[3]	I_{FMTEST}	79	I/O	I/O	P0[4]	Analog column mux input and column output, V_{REF}
30	I/O		P1[1][13]	Crystal (XTALin), I^2C SCL, TC SCLK.	80			NC	No internal connection
31			NC	No internal connection	81	I/O	I	P0[6]	Analog column mux input
32	Power		V_{DD}	Supply voltage	82	Power		V_{DD}	Supply voltage
33			NC	No internal connection	83	Power		V_{DD}	Supply voltage
34	Power		V_{SS}	Ground connection [12]	84	Power		V_{SS}	Ground connection [12]
35			NC	No internal connection	85	Power		V_{SS}	Ground connection [12]
36	I/O		P7[7]		86	I/O		P6[0]	
37	I/O		P7[6]		87	I/O		P6[1]	
38	I/O		P7[5]		88	I/O		P6[2]	
39	I/O		P7[4]		89	I/O		P6[3]	
40	I/O		P7[3]		90	I/O		P6[4]	
41	I/O		P7[2]		91	I/O		P6[5]	
42	I/O		P7[1]		92	I/O		P6[6]	
43	I/O		P7[0]		93	I/O		P6[7]	
44	I/O		P1[0]*	Crystal (XTALout), I^2C SDA, TC SDATA	94			NC	No internal connection
45	I/O		P1[2]	V_{FMTEST}	95	I/O	I	P0[7]	Analog column mux input
46	I/O		P1[4]	Optional External Clock Input (EXTCLK)	96			NC	No internal connection
47	I/O		P1[6]		97	I/O	I/O	P0[5]	Analog column mux input and column output
48			NC	No internal connection	98			NC	No internal connection
49			NC	No internal connection	99	I/O	I/O	P0[3]	Analog column mux input and column output
50			NC	No internal connection	100			NC	No internal connection

LEGEND A = Analog, I = Input, O = Output, NC = No connection. Pin must be left floating, TC/TM: Test.

Notes
12. All V_{SS} pins should be brought out to one common GND plane.
13. ISSP pin which is not High-Z at POR.

Figure 9. CY8C29000 OCD (Not for Production)

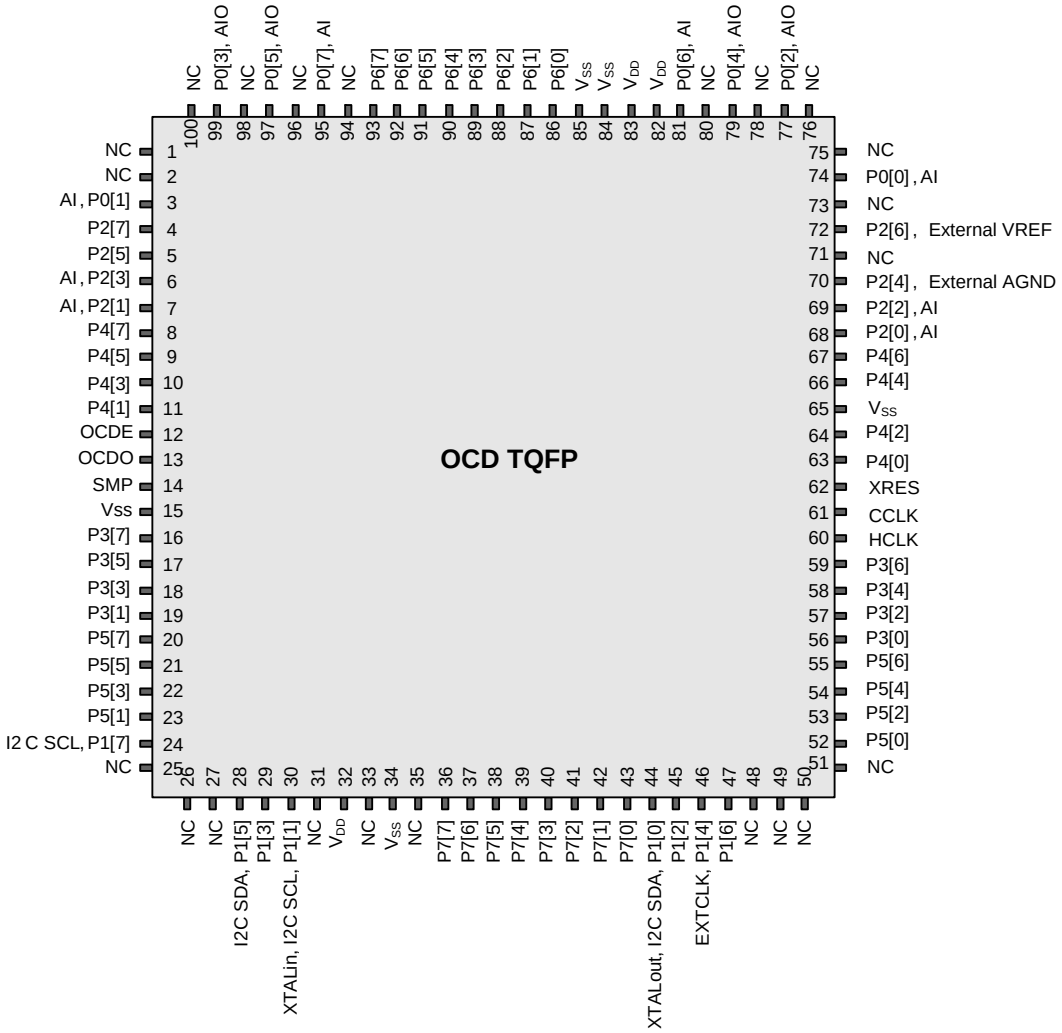
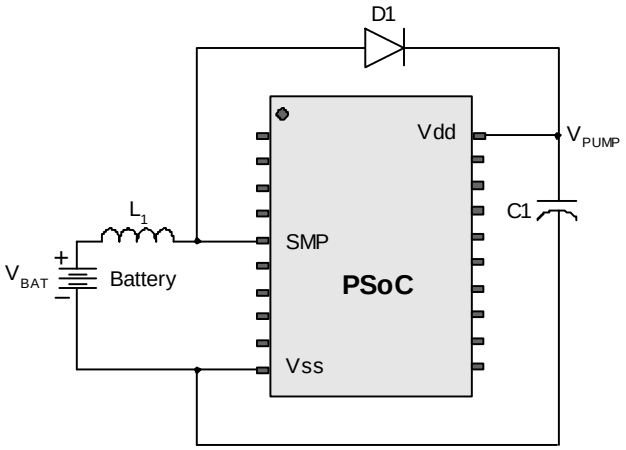


Figure 12. Basic Switch Mode Pump Circuit



DC Analog Reference Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ TA ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ TA ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

The guaranteed specifications for RefHI and RefLO are measured through the analog continuous time PSoC blocks. The power levels for RefHI and RefLO refer to the analog reference control register. AGND is measured at P2[4] in AGND bypass mode. Each analog continuous time PSoC block adds a maximum of 10 mV additional offset error to guaranteed AGND specifications from the local AGND buffer. Reference control power can be set to medium or high unless otherwise noted.

Note Avoid using P2[4] for digital signaling when using an analog resource that depends on the analog reference. Some coupling of the digital signal may appear on the AGND.

Table 21. 5-V DC Analog Reference Specifications

Reference ARF_CR[5:3]	Reference Power Settings	Symbol	Reference	Description	Min	Typ	Max	Unit
0b000	RefPower = High Opamp bias = High	V_{REFHI}	Ref High	$V_{DD}/2$ + Bandgap	$V_{DD}/2$ + 1.228	$V_{DD}/2$ + 1.290	$V_{DD}/2$ + 1.352	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.078	$V_{DD}/2$ – 0.007	$V_{DD}/2$ + 0.063	V
		V_{REFLO}	Ref Low	$V_{DD}/2$ – Bandgap	$V_{DD}/2$ – 1.336	$V_{DD}/2$ – 1.295	$V_{DD}/2$ – 1.250	V
	RefPower = High Opamp bias = Low	V_{REFHI}	Ref High	$V_{DD}/2$ + Bandgap	$V_{DD}/2$ + 1.224	$V_{DD}/2$ + 1.293	$V_{DD}/2$ + 1.356	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.056	$V_{DD}/2$ – 0.005	$V_{DD}/2$ + 0.043	V
		V_{REFLO}	Ref Low	$V_{DD}/2$ – Bandgap	$V_{DD}/2$ – 1.338	$V_{DD}/2$ – 1.298	$V_{DD}/2$ – 1.255	V
	RefPower = Med Opamp bias = High	V_{REFHI}	Ref High	$V_{DD}/2$ + Bandgap	$V_{DD}/2$ + 1.226	$V_{DD}/2$ + 1.293	$V_{DD}/2$ + 1.356	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.057	$V_{DD}/2$ – 0.006	$V_{DD}/2$ + 0.044	V
		V_{REFLO}	Ref Low	$V_{DD}/2$ – Bandgap	$V_{DD}/2$ – 1.337	$V_{DD}/2$ – 1.298	$V_{DD}/2$ – 1.256	V
	RefPower = Med Opamp bias = Low	V_{REFHI}	Ref High	$V_{DD}/2$ + Bandgap	$V_{DD}/2$ + 1.226	$V_{DD}/2$ + 1.294	$V_{DD}/2$ + 1.359	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.047	$V_{DD}/2$ – 0.004	$V_{DD}/2$ + 0.035	V
		V_{REFLO}	Ref Low	$V_{DD}/2$ – Bandgap	$V_{DD}/2$ – 1.338	$V_{DD}/2$ – 1.299	$V_{DD}/2$ – 1.258	V

Table 21. 5-V DC Analog Reference Specifications (continued)

Reference ARF_CR[5:3]	Reference Power Settings	Symbol	Reference	Description	Min	Typ	Max	Unit
0b101	RefPower = High Opamp bias = High	V_{REFHI}	Ref High	P2[4] + Bandgap ($P2[4] = V_{DD}/2$)	P2[4] + 1.222	P2[4] + 1.290	P2[4] + 1.343	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4] – Bandgap ($P2[4] = V_{DD}/2$)	P2[4] – 1.331	P2[4] – 1.295	P2[4] – 1.254	V
	RefPower = High Opamp bias = Low	V_{REFHI}	Ref High	P2[4] + Bandgap ($P2[4] = V_{DD}/2$)	P2[4] + 1.226	P2[4] + 1.293	P2[4] + 1.347	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4] – Bandgap ($P2[4] = V_{DD}/2$)	P2[4] – 1.331	P2[4] – 1.298	P2[4] – 1.259	V
	RefPower = Med Opamp bias = High	V_{REFHI}	Ref High	P2[4] + Bandgap ($P2[4] = V_{DD}/2$)	P2[4] + 1.227	P2[4] + 1.294	P2[4] + 1.347	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4] – Bandgap ($P2[4] = V_{DD}/2$)	P2[4] – 1.331	P2[4] – 1.298	P2[4] – 1.259	V
	RefPower = Med Opamp bias = Low	V_{REFHI}	Ref High	P2[4] + Bandgap ($P2[4] = V_{DD}/2$)	P2[4] + 1.228	P2[4] + 1.295	P2[4] + 1.349	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4] – Bandgap ($P2[4] = V_{DD}/2$)	P2[4] – 1.332	P2[4] – 1.299	P2[4] – 1.260	V
0b110	RefPower = High Opamp bias = High	V_{REFHI}	Ref High	2 × Bandgap	2.535	2.598	2.644	V
		V_{AGND}	AGND	Bandgap	1.227	1.305	1.398	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.009	V_{SS} + 0.038	V
	RefPower = High Opamp bias = Low	V_{REFHI}	Ref High	2 × Bandgap	2.530	2.598	2.643	V
		V_{AGND}	AGND	Bandgap	1.244	1.303	1.370	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.005	V_{SS} + 0.024	V
	RefPower = Med Opamp bias = High	V_{REFHI}	Ref High	2 × Bandgap	2.532	2.598	2.644	V
		V_{AGND}	AGND	Bandgap	1.239	1.304	1.380	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.006	V_{SS} + 0.026	V
	RefPower = Med Opamp bias = Low	V_{REFHI}	Ref High	2 × Bandgap	2.528	2.598	2.645	V
		V_{AGND}	AGND	Bandgap	1.249	1.302	1.362	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.004	V_{SS} + 0.018	V
0b111	RefPower = High Opamp bias = High	V_{REFHI}	Ref High	3.2 × Bandgap	4.041	4.155	4.234	V
		V_{AGND}	AGND	1.6 × Bandgap	1.998	2.083	2.183	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.010	V_{SS} + 0.038	V
	RefPower = High Opamp bias = Low	V_{REFHI}	Ref High	3.2 × Bandgap	4.047	4.153	4.236	V
		V_{AGND}	AGND	1.6 × Bandgap	2.012	2.082	2.157	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.006	V_{SS} + 0.024	V
	RefPower = Med Opamp bias = High	V_{REFHI}	Ref High	3.2 × Bandgap	4.049	4.154	4.238	V
		V_{AGND}	AGND	1.6 × Bandgap	2.008	2.083	2.165	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.006	V_{SS} + 0.026	V
	RefPower = Med Opamp bias = Low	V_{REFHI}	Ref High	3.2 × Bandgap	4.047	4.154	4.238	V
		V_{AGND}	AGND	1.6 × Bandgap	2.016	2.081	2.150	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.004	V_{SS} + 0.018	V

Table 22. 3.3-V DC Analog Reference Specifications

Reference ARF_CR[5:3]	Reference Power Settings	Symbol	Reference	Description	Min	Typ	Max	Unit
0b000	RefPower = High Opamp bias = High	V_{REFHI}	Ref High	$V_{DD}/2$ + Band-Gap	$V_{DD}/2$ + 1.225	$V_{DD}/2$ + 1.292	$V_{DD}/2$ + 1.361	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.067	$V_{DD}/2$ – 0.002	$V_{DD}/2$ + 0.063	V
		V_{REFLO}	Ref Low	$V_{DD}/2$ – Band-Gap	$V_{DD}/2$ – 1.35	$V_{DD}/2$ – 1.293	$V_{DD}/2$ – 1.210	V
	RefPower = High Opamp bias = Low	V_{REFHI}	Ref High	$V_{DD}/2$ + Band-Gap	$V_{DD}/2$ + 1.218	$V_{DD}/2$ + 1.294	$V_{DD}/2$ + 1.370	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.038	$V_{DD}/2$ – 0.001	$V_{DD}/2$ + 0.035	V
		V_{REFLO}	Ref Low	$V_{DD}/2$ – Band-Gap	$V_{DD}/2$ – 1.329	$V_{DD}/2$ – 1.296	$V_{DD}/2$ – 1.259	V
	RefPower = Med Opamp bias = High	V_{REFHI}	Ref High	$V_{DD}/2$ + Band-Gap	$V_{DD}/2$ + 1.221	$V_{DD}/2$ + 1.294	$V_{DD}/2$ + 1.366	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.050	$V_{DD}/2$ – 0.002	$V_{DD}/2$ + 0.046	V
		V_{REFLO}	Ref Low	$V_{DD}/2$ – Band-Gap	$V_{DD}/2$ – 1.331	$V_{DD}/2$ – 1.296	$V_{DD}/2$ – 1.260	V
	RefPower = Med Opamp bias = Low	V_{REFHI}	Ref High	$V_{DD}/2$ + Band-Gap	$V_{DD}/2$ + 1.226	$V_{DD}/2$ + 1.295	$V_{DD}/2$ + 1.365	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.028	$V_{DD}/2$ – 0.001	$V_{DD}/2$ + 0.025	V
		V_{REFLO}	Ref Low	$V_{DD}/2$ – Band-Gap	$V_{DD}/2$ – 1.329	$V_{DD}/2$ – 1.297	$V_{DD}/2$ – 1.262	V

Table 22. 3.3-V DC Analog Reference Specifications (continued)

Reference ARF_CR[5:3]	Reference Power Settings	Symbol	Reference	Description	Min	Typ	Max	Unit
0b101	RefPower = High Opamp bias = High	V_{REFHI}	Ref High	P2[4] + Band-Gap (P2[4] = $V_{DD}/2$)	P2[4] + 1.213	P2[4] + 1.291	P2[4] + 1.367	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	V
		V_{REFLO}	Ref Low	P2[4] – Band-Gap (P2[4] = $V_{DD}/2$)	P2[4] – 1.333	P2[4] – 1.294	P2[4] – 1.208	V
	RefPower = High Opamp bias = Low	V_{REFHI}	Ref High	P2[4] + Band-Gap (P2[4] = $V_{DD}/2$)	P2[4] + 1.217	P2[4] + 1.294	P2[4] + 1.368	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	V
		V_{REFLO}	Ref Low	P2[4] – Band-Gap (P2[4] = $V_{DD}/2$)	P2[4] – 1.320	P2[4] – 1.296	P2[4] – 1.261	V
	RefPower = Med Opamp bias = High	V_{REFHI}	Ref High	P2[4] + Band-Gap (P2[4] = $V_{DD}/2$)	P2[4] + 1.217	P2[4] + 1.294	P2[4] + 1.369	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	V
		V_{REFLO}	Ref Low	P2[4] – Band-Gap (P2[4] = $V_{DD}/2$)	P2[4] – 1.322	P2[4] – 1.297	P2[4] – 1.262	V
	RefPower = Med Opamp bias = Low	V_{REFHI}	Ref High	P2[4] + Band-Gap (P2[4] = $V_{DD}/2$)	P2[4] + 1.219	P2[4] + 1.295	P2[4] + 1.37	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	V
		V_{REFLO}	Ref Low	P2[4] – Band-Gap (P2[4] = $V_{DD}/2$)	P2[4] – 1.324	P2[4] – 1.297	P2[4] – 1.262	V
0b110	RefPower = High Opamp bias = High	V_{REFHI}	Ref High	2 × BandGap	2.507	2.598	2.698	V
		V_{AGND}	AGND	BandGap	1.203	1.307	1.424	V
		V_{REFLO}	Ref Low	Vss	Vss	Vss + 0.012	Vss + 0.067	V
	RefPower = High Opamp bias = Low	V_{REFHI}	Ref High	2 × BandGap	2.516	2.598	2.683	V
		V_{AGND}	AGND	BandGap	1.241	1.303	1.376	V
		V_{REFLO}	Ref Low	Vss	Vss	Vss + 0.007	Vss + 0.040	V
	RefPower = Med Opamp bias = High	V_{REFHI}	Ref High	2 × BandGap	2.510	2.599	2.693	V
		V_{AGND}	AGND	BandGap	1.240	1.305	1.374	V
		V_{REFLO}	Ref Low	Vss	Vss	Vss + 0.008	Vss + 0.048	V
	RefPower = Med Opamp bias = Low	V_{REFHI}	Ref High	2 × BandGap	2.515	2.598	2.683	V
		V_{AGND}	AGND	BandGap	1.258	1.302	1.355	V
		V_{REFLO}	Ref Low	Vss	Vss	Vss + 0.005	Vss + 0.03	V
0b111	All power settings. Not allowed for 3.3 V.	–	–	–	–	–	–	–

DC Analog External Reference Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 23. 5-V DC Analog External Reference Specifications

Reference	Description	Min	Typ	Max	Unit
Ref Low	Ref Low = P2[4] – P2[6] (P2[4] = V_{CC}/2, P2[6] = 1.3 V)	1.12	1.221	1.28	V
AGND	AGND = P2[4] (P2[4] = V_{CC}/2)	2.487	2.499	2.513	V
Ref High	Ref Low = P2[4] + P2[6] (P2[4] = V_{CC}/2, P2[6] = 1.3 V)	3.67	3.759	3.93	V

Table 24. 3.3-V DC Analog External Reference Specifications

Reference	Description	Min	Typ	Max	Unit
Ref Low	Ref Low = P2[4] – P2[6] (P2[4] = V_{CC}/2, P2[6] = 1.3 V)	0.29	0.371	0.41	V
AGND	AGND = P2[4] (P2[4] = V_{CC}/2)	1.642	1.649	1.658	V
Ref High	Ref Low = P2[4] + P2[6] (P2[4] = V_{CC}/2, P2[6] = 1.3 V)	–	2.916	–	V

DC Analog PSoC Block Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 25. DC Analog PSoC Block Specifications

Symbol	Description	Min	Typ	Max	Unit	Notes
R_{CT}	Resistor unit value (continuous time)	–	12.2	–	kΩ	
C_{SC}	Capacitor unit value (switch cap)	–	80	–	fF	

AC Electrical Characteristics

AC Chip-Level Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Note See the individual user module datasheets for information on maximum frequencies for user modules.

Table 29. AC Chip-Level Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{IMO24} [21]	Internal main oscillator (IMO) frequency for 24 MHz	22.8	24	25.2[22,23]	MHz	Trimmed for 5 V or 3.3 V operation using factory trim values. See Figure 11 on page 21. SLIMO Mode = 0.
F_{IMO6}	IMO frequency for 6 MHz	5.5	6	6.5[22,23]	MHz	Trimmed for 5 V or 3.3 V operation using factory trim values. See Figure 11 on page 21. SLIMO Mode = 1.
F_{CPU1}	CPU frequency (5 V Nominal)	0.0914	24	25.2[22]	MHz	SLIMO Mode = 0.
F_{CPU2}	CPU frequency (3.3 V Nominal)	0.0914	12	12.6[23]	MHz	SLIMO Mode = 0.
F_{48M}	Digital PSoC block frequency	0	48	50.4[22,24]	MHz	Refer to AC Digital Block Specifications on page 45.
F_{24M}	Digital PSoC block frequency	0	24	25.2 [24]	MHz	
F_{32K1}	Internal low speed oscillator frequency	15	32	64	kHz	
F_{32K2}	External crystal oscillator	–	32.768	–	kHz	Accuracy is capacitor and crystal dependent. 50% duty cycle
F_{32K_U}	Internal low speed oscillator (ILO) untrimmed frequency	5	–	100	kHz	After a reset and before the M8C starts to run, the ILO is not trimmed. See the System Resets section of the PSoC Technical Reference Manual for details on this timing
F_{PLL}	PLL frequency	–	23.986	–	MHz	A multiple (x732) of crystal frequency
$T_{PLLSLEW}$	PLL lock time	0.5	–	10	ms	
$T_{PLLSLEWLOW}$	PLL lock time for low gain setting	0.5	–	50	ms	
T_{OS}	External crystal oscillator startup to 1%	–	250	500	ms	
T_{OSACC}	External crystal oscillator startup to 100 ppm	–	300	600	ms	The crystal oscillator frequency is within 100 ppm of its final value by the end of the T_{OSACC} period. Correct operation assumes a properly loaded 1 µW maximum drive level 32.768 kHz crystal. 3.0 V ≤ V_{DD} ≤ 5.5 V, –40 °C ≤ T_A ≤ 85 °C.
T_{XRST}	External reset pulse width	10	–	–	µs	
DC24M	24 MHz duty cycle	40	50	60	%	
DC_{ILO}	Internal low speed oscillator duty cycle	20	50	80	%	
Step24M	24 MHz trim step size	–	50	–	kHz	
Fout48M	48 MHz output frequency	45.6	48.0	50.4[22, 23]	MHz	Trimmed. Using factory trim values
F_{MAX}	Maximum frequency of signal on row input or row output.	–	–	12.3	MHz	

Notes
21. Errata: When the device is operated within 0 °C to 70 °C, the frequency tolerance is reduced to ±2.5%, but if operated at extreme temperature (below 0 °C or above 70 °C), frequency tolerance deviates from ±2.5% to ±5%. For more information, see Errata on page 63.
22. 4.75 V < V_{DD} < 5.25 V.
23. 3.0 V < V_{DD} < 3.6 V. See application note Adjusting PSoC® Trims for 3.3 V and 2.7 V Operation – AN2012 for information on trimming for operation at 3.3 V.
24. See the individual user module datasheets for information on maximum frequencies for user modules

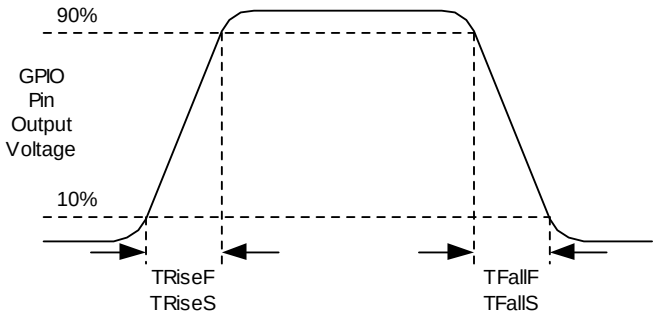
AC General Purpose I/O Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 30. AC GPIO Specifications

Symbol	Description	Min	Typ	Max	Unit	Notes
F_{GPIO}	GPIO operating frequency	0	–	12.3	MHz	Normal strong mode
tRiseF	Rise time, normal strong mode, Cload = 50 pF	3	–	18	ns	V_{DD} = 4.75 to 5.25 V, 10% to 90%
tFallF	Fall time, normal strong mode, Cload = 50 pF	2	–	18	ns	V_{DD} = 4.75 to 5.25 V, 10% to 90%
tRiseS	Rise time, slow strong mode, Cload = 50 pF	10	27	–	ns	V_{DD} = 3 to 5.25 V, 10% to 90%
tFallS	Fall time, slow strong mode, Cload = 50 pF	10	22	–	ns	V_{DD} = 3 to 5.25 V, 10% to 90%

Figure 16. GPIO Timing Diagram



AC Operational Amplifier Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Settling times, slew rates, and gain bandwidth are based on the analog continuous time PSoC block.

Power = High and Opamp bias = High is not supported at 3.3 V.

Table 31. 5-V AC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Unit
t_{ROA}	Rising settling time to 0.1% for a 1 V step (10 pF load, unity gain) Power = Low, Opamp bias = Low Power = Medium, Opamp bias = High Power = High, Opamp bias = High	 – – –	 – – –	 3.9 0.72 0.62	 µs µs µs
t_{SOA}	Falling settling time to 0.1% for a 1 V step (10 pF load, unity gain) Power = Low, Opamp bias = Low Power = Medium, Opamp bias = High Power = High, Opamp bias = High	 – – –	 – – –	 5.9 0.92 0.72	 µs µs µs
SR_{ROA}	Rising slew rate (20% to 80%) of a 1 V step (10 pF load, unity gain) Power = Low, Opamp bias = Low Power = Medium, Opamp bias = High Power = High, Opamp bias = High	 0.15 1.7 6.5	 – – –	 – – –	 V/µs V/µs V/µs
SR_{FOA}	Falling slew rate (20% to 80%) of a 1 V step (10 pF load, unity gain) Power = Low, Opamp bias = Low Power = Medium, Opamp bias = High Power = High, Opamp bias = High	 0.01 0.5 4.0	 – – –	 – – –	 V/µs V/µs V/µs
BW_{OA}	Gain bandwidth product Power = Low, Opamp bias = Low Power = Medium, Opamp bias = High Power = High, Opamp bias = High	 0.75 3.1 5.4	 – – –	 – – –	 MHz MHz MHz
E_{NOA}	Noise at 1 kHz (Power = Medium, Opamp bias = High)	–	100	–	nV/rt-Hz

AC Analog Output Buffer Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 35. 5-V AC Analog Output Buffer Specifications

Symbol	Description	Min	Typ	Max	Unit
t_{ROB}	Rising settling time to 0.1%, 1 V Step, 100 pF load Power = Low Power = High	 – –	 – –	 4 4	 µs µs
t_{SOB}	Falling settling time to 0.1%, 1 V step, 100 pF load Power = Low Power = High	 – –	 – –	 3.4 3.4	 µs µs
SR_{ROB}	Rising slew rate (20% to 80%), 1 V step, 100 pF load Power = Low Power = High	 0.5 0.5	 – –	 – –	 V/µs V/µs
SR_{FOB}	Falling slew rate (80% to 20%), 1 V step, 100 pF load Power = Low Power = High	 0.55 0.55	 – –	 – –	 V/µs V/µs
BW_{OB}	Small signal bandwidth, 20 mV_{pp}, 3 dB BW, 100 pF load Power = Low Power = High	 0.8 0.8	 – –	 – –	 MHz MHz
BW_{OB}	Large signal bandwidth, 1 V_{pp}, 3 dB BW, 100 pF load Power = Low Power = High	 300 300	 – –	 – –	 kHz kHz

Table 36. 3.3-V AC Analog Output Buffer Specifications

Symbol	Description	Min	Typ	Max	Unit
t_{ROB}	Rising settling time to 0.1%, 1 V Step, 100 pF load Power = Low Power = High	 – –	 – –	 4.7 4.7	 µs µs
t_{SOB}	Falling settling time to 0.1%, 1 V Step, 100 pF load Power = Low Power = High	 – –	 – –	 4 4	 µs µs
SR_{ROB}	Rising slew rate (20% to 80%), 1 V Step, 100 pF load Power = Low Power = High	 0.36 0.36	 – –	 – –	 V/µs V/µs
SR_{FOB}	Falling slew rate (80% to 20%), 1 V Step, 100 pF load Power = Low Power = High	 0.40 0.40	 – –	 – –	 V/µs V/µs
BW_{OB}	Small signal bandwidth, 20 mV_{pp}, 3 dB BW, 100 pF load Power = Low Power = High	 0.7 0.7	 – –	 – –	 MHz MHz
BW_{OB}	Large signal bandwidth, 1 V_{pp}, 3 dB BW, 100 pF load Power = Low Power = High	 200 200	 – –	 – –	 kHz kHz

AC External Clock Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 37. 5-V AC External Clock Specifications

Symbol	Description	Min	Typ	Max	Unit
F_{OSCEXT}	Frequency	0.093	–	24.6	MHz
–	High period	20.6	–	5300	ns
–	Low period	20.6	–	–	ns
–	Power-up IMO to switch	150	–	–	µs

Table 38. 3.3-V AC External Clock Specifications

Symbol	Description	Min	Typ	Max	Unit
F_{OSCEXT}	Frequency with CPU clock divide by 1	0.093	–	12.3	MHz
F_{OSCEXT}	Frequency with CPU clock divide by 2 or greater	0.186	–	24.6	MHz
–	High period with CPU clock divide by 1	41.7	–	5300	ns
–	Low period with CPU clock divide by 1	41.7	–	–	ns
–	Power-up IMO to switch	150	–	–	µs

AC Programming Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 39. AC Programming Specifications

Symbol	Description	Min	Typ	Max	Unit	Notes
t_{RSCLK}	Rise time of SCLK	1	–	20	ns	–
t_{FSCLK}	Fall time of SCLK	1	–	20	ns	–
t_{SSCLK}	Data setup time to falling edge of SCLK	40	–	–	ns	–
t_{HSCLK}	Data hold time from falling edge of SCLK	40	–	–	ns	–
F_{SCLK}	Frequency of SCLK	0	–	8	MHz	–
t_{ERASEB}	Flash erase time (block)	–	10	–	ms	–
t_{WRITE}	Flash block write time	–	40	–	ms	–
t_{DSCLK}	Data out delay from falling edge of SCLK	–	–	45	ns	$V_{DD} > 3.6$
t_{DSCLK3}	Data out delay from falling edge of SCLK	–	–	50	ns	$3.0 \le V_{DD} \le 3.6$
$t_{ERASEALL}$	Flash erase time (Bulk)	–	80	–	ms	Erase all blocks and protection fields at once
$t_{PROGRAM\_HOT}$	Flash block erase + Flash block write time	–	–	100[28]	ms	0 °C ≤ Tj ≤ 100 °C
$t_{PROGRAM\_COLD}$	Flash block erase + Flash block write time	–	–	200[28]	ms	–40 °C ≤ Tj ≤ 0 °C

Note
28. For the full industrial range, you must employ a temperature sensor user module (FlashTemp) and feed the result to the temperature argument before writing. Refer to the Flash APIs application note Design Aids – Reading and Writing PSoC® Flash – AN2015 for more information.

Figure 25. 48-pin QFN (7 × 7 × 1.0 mm) 5.1 × 5.1 E-Pad (Sawn) Package Outline, 001-13191

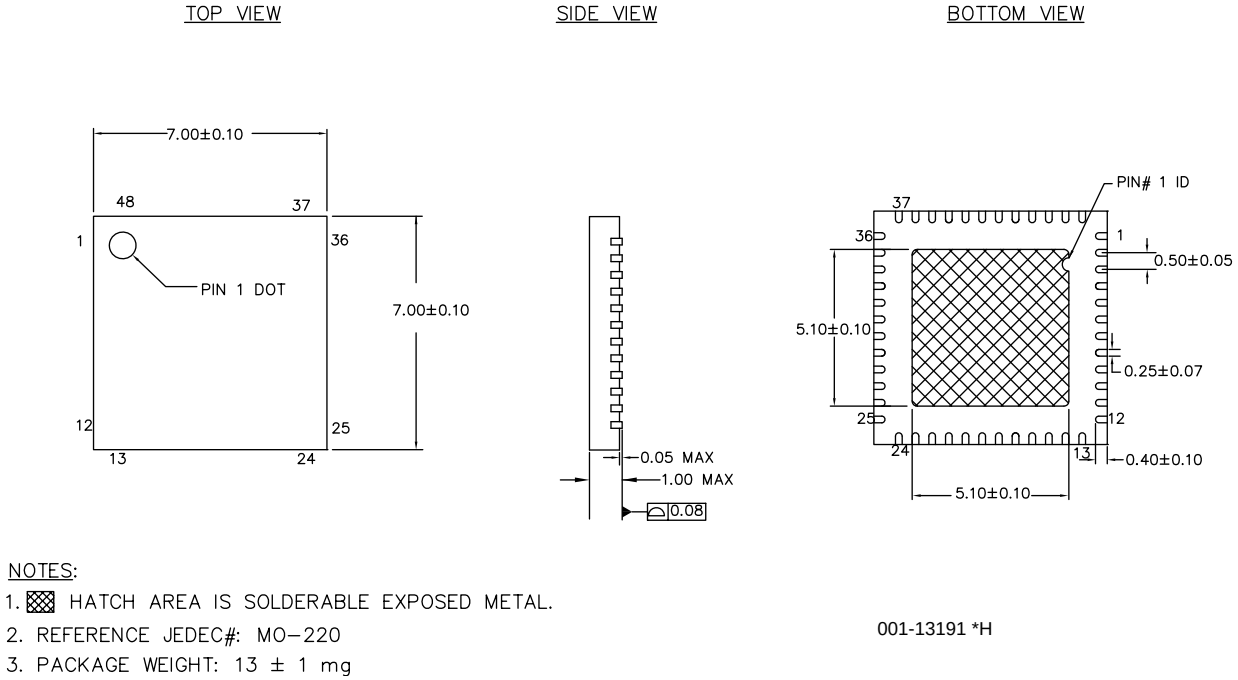
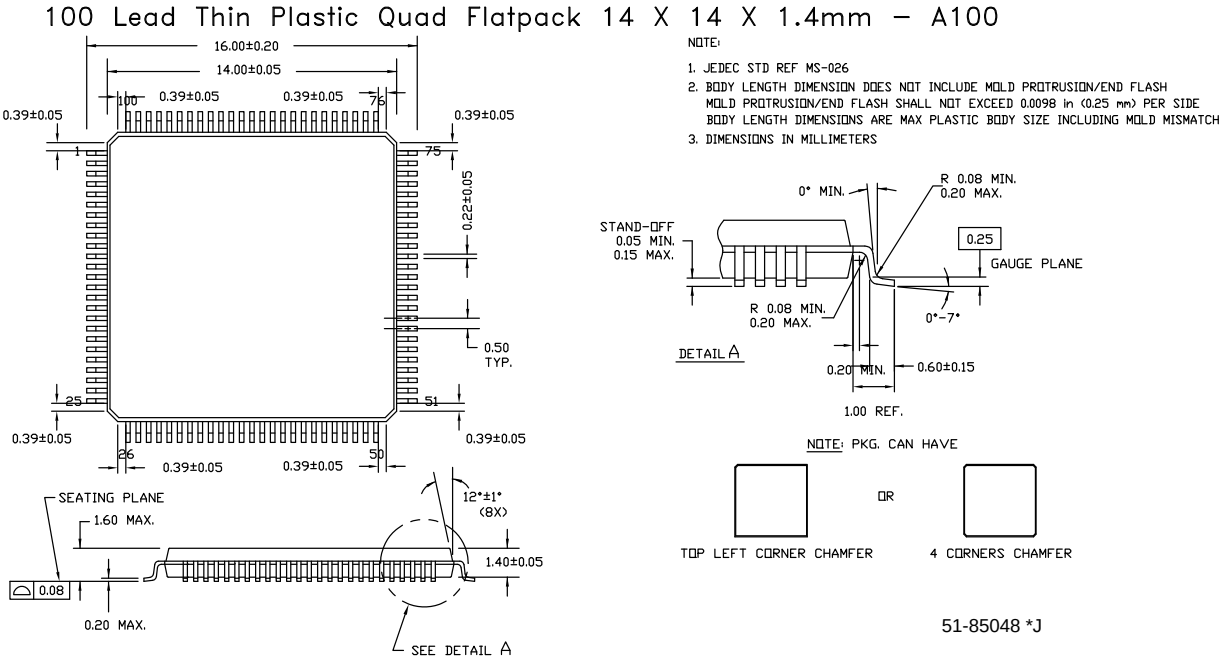


Figure 26. 100-pin TQFP (14 × 14 × 1.4 mm) Package Outline, 51-85048



Important Note For information on the preferred dimensions for mounting the QFN packages, see the application note *Design Guidelines for Cypress Quad Flat No Extended Lead (QFN) Packaged Devices – AN72845* available at http://www.cypress.com.

Important Note Pinned vias for thermal conduction are not required for the low-power PSoC device.

Device Programmers

All device programmers can be purchased from the Cypress Online Store.

CY3216 Modular Programmer

The CY3216 Modular Programmer kit features a modular programmer and the MiniProg1 programming unit. The modular programmer includes three programming module cards and supports multiple Cypress products. The kit includes:

- Modular programmer base
- Three programming module cards
- MiniProg programming unit
- PSoC Designer software CD
- Getting Started guide
- USB 2.0 cable

CY3207ISSP In-System Serial Programmer (ISSP)

The CY3207ISSP is a production programmer. It includes protection circuitry and an industrial case that is more robust than the MiniProg in a production-programming environment.

Note CY3207ISSP needs special software and is not compatible with PSoC Programmer. The kit includes:

- CY3207 programmer unit
- PSoC ISSP software CD
- 110 ~ 240 V power supply, Euro-Plug adapter
- USB 2.0 cable

Accessories (Emulation and Programming)

Table 44. Emulation and Programming Accessories

Part #	Pin Package	Flex-Pod Kit[32]	Foot Kit[33]	Adapter[34]
CY8C29466-24PXI	28-pin PDIP	CY3250-29XXX	CY3250-28PDIP-FK	Adapters can be found at http://www.emulation.com.
CY8C29466-24PVXI	28-pin SSOP	CY3250-29XXX	CY3250-28SSOP-FK	
CY8C29466-24SXI	28-pin SOIC	CY3250-29XXX	CY3250-28SOIC-FK	
CY8C29566-24AXI	44-pin TQFP	CY3250-29XXX	CY3250-44TQFP-FK	
CY8C29666-24PVXI	48-pin SSOP	CY3250-29XXX	CY3250-48SSOP-FK	
CY8C29666-24LTXI	48-pin QFN	CY3250-29XXXQFN	CY3250-48QFN-FK	
CY8C29866-24AXI	100-pin TQFP	CY3250-29XXX	CY3250-100TQFP-FK	

Notes
32. Flex-Pod kit includes a practice flex-pod and a practice PCB, in addition to two flex-pods.
33. Foot kit includes surface mount feet that can be soldered to the target PCB.
34. Programming adapter converts non-DIP package to DIP footprint. Specific details and ordering information for each of the adapters can be found at http://www.emulation.com

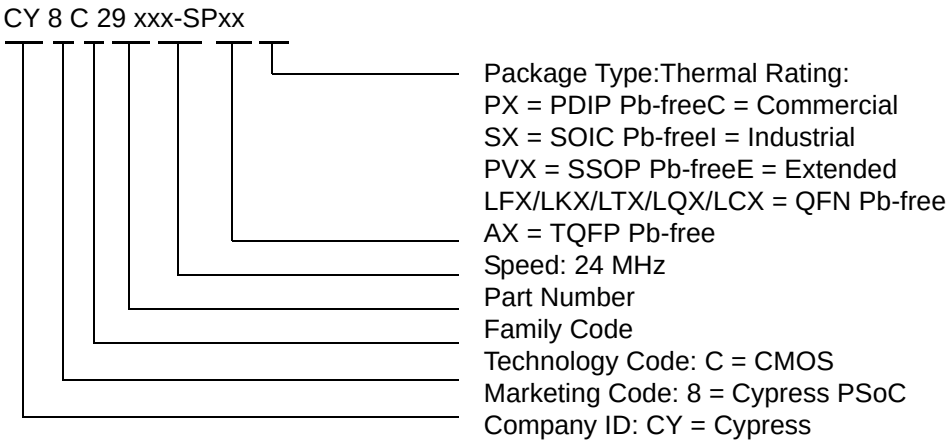
Ordering Information

The following table lists the CY8C29x66 PSoC device's key package features and ordering codes.

Package	Ordering Code	Flash (KB)	RAM (KB)	Switch Mode Pump	Temperature Range	Digital PSoC Blocks	Analog PSoC Blocks	Digital I/O Pins	Analog Inputs	Analog Outputs	XRES Pin
28-pin (300-mil) DIP	CY8C29466-24PXI	32	2	Yes	–40 °C to +85 °C	16	12	24	12	4	Yes
28-pin (210-mil) SSOP	CY8C29466-24PVXI	32	2	Yes	–40 °C to +85 °C	16	12	24	12	4	Yes
28-pin (210-mil) SSOP (Tape and Reel)	CY8C29466-24PVXIT	32	2	Yes	–40 °C to +85 °C	16	12	24	12	4	Yes
28-pin (300-mil) SOIC	CY8C29466-24SXI	32	2	Yes	–40 °C to +85 °C	16	12	24	12	4	Yes
28-pin (300-mil) SOIC (Tape and Reel)	CY8C29466-24SXIT	32	2	Yes	–40 °C to +85 °C	16	12	24	12	4	Yes
44-pin TQFP	CY8C29566-24AXI	32	2	Yes	–40 °C to +85 °C	16	12	40	12	4	Yes
44-pin TQFP (Tape and Reel)	CY8C29566-24AXIT	32	2	Yes	–40 °C to +85 °C	16	12	40	12	4	Yes
48-pin (300-mil) SSOP	CY8C29666-24PVXI	32	2	Yes	–40 °C to +85 °C	16	12	44	12	4	Yes
48-pin (300-mil) SSOP (Tape and Reel)	CY8C29666-24PVXIT	32	2	Yes	–40 °C to +85 °C	16	12	44	12	4	Yes
100-Pin TQFP	CY8C29866-24AXI	32	2	Yes	–40 °C to +85 °C	16	12	64	12	4	Yes
100-Pin OCD TQFP[35]	CY8C29000-24AXI	32	2	Yes	–40 °C to +85 °C	16	12	64	12	4	Yes
48-Pin (7 × 7 × 1.0 mm) QFN (Sawn)	CY8C29666-24LTXI	32	2	Yes	–40 °C to +85 °C	16	12	44	12	4	Yes
48-Pin (7 × 7 × 1.0 mm) QFN (Sawn)	CY8C29666-24LTXIT	32	2	Yes	–40 °C to +85 °C	16	12	44	12	4	Yes

Note For Die sales information, contact a local Cypress sales office or field applications engineer (FAE).

Ordering Code Definitions



Note
35. This part may be used for in-circuit debugging. It is NOT available for production.

Acronyms

Table 45 lists the acronyms that are used in this document.

Table 45. Acronyms Used in this Datasheet

Acronym	Description	Acronym	Description
AC	alternating current	MIPS	million instructions per second
ADC	analog-to-digital converter	OCD	on-chip debug
API	application programming interface	PCB	printed circuit board
CMOS	complementary metal oxide semiconductor	PDIP	plastic dual-in-line package
CPU	central processing unit	PGA	programmable gain amplifier
CRC	cyclic redundancy check	PLL	phase-locked loop
CT	continuous time	POR	power on reset
DAC	digital-to-analog converter	PPOR	precision power on reset
DC	direct current	PRS	pseudo-random sequence
DTMF	dual-tone multi-frequency	PSoC®	Programmable System-on-Chip
ECO	external crystal oscillator	PWM	pulse width modulator
EEPROM	electrically erasable programmable read-only memory	QFN	quad flat no leads
GPIO	general purpose I/O	RTC	real time clock
ICE	in-circuit emulator	SAR	successive approximation
IDE	integrated development environment	SC	switched capacitor
ILO	internal low speed oscillator	SMP	switch mode pump
IMO	internal main oscillator	SOIC	small-outline integrated circuit
I/O	input/output	SPI	serial peripheral interface
IrDA	infrared data association	SRAM	static random access memory
ISSP	in-system serial programming	SROM	supervisory read only memory
LCD	liquid crystal display	SSOP	shrink small-outline package
LED	light-emitting diode	TQFP	thin quad flat pack
LPC	low power comparator	UART	universal asynchronous reciever / transmitter
LVD	low voltage detect	USB	universal serial bus
MAC	multiply-accumulate	WDT	watchdog timer
MCU	microcontroller unit	XRES	external reset

Reference Documents

CY8CPLC20, CY8CLED16P01, CY8C29x66, CY8C27x43, CY8C24x94, CY8C24x23, CY8C24x23A, CY8C22x13, CY8C21x34, CY8C21x23, CY7C64215, CY7C603xx, CY8CNP1xx, and CYWUSB6953 PSoC® Programmable System-on-Chip Technical Reference Manual (TRM) (001-14463)

Design Aids – Reading and Writing PSoC® Flash - AN2015 (001-40459)

Design Guidelines for Cypress Quad Flat No Extended Lead (QFN) Packaged Devices – AN72845 available at http://www.cypress.com.

Glossary (continued)

microcontroller	An integrated circuit chip that is designed primarily for control systems and products. In addition to a CPU, a microcontroller typically includes memory, timing circuits, and IO circuitry. The reason for this is to permit the realization of a controller with a minimal quantity of chips, thus achieving maximal possible miniaturization. This in turn, reduces the volume and the cost of the controller. The microcontroller is normally not used for general-purpose computation as is a microprocessor.
mixed-signal	The reference to a circuit containing both analog and digital techniques and components.
modulator	A device that imposes a signal on a carrier.
noise	1. A disturbance that affects a signal and that may distort the information carried by the signal. 2. The random variations of one or more characteristics of any entity such as voltage, current, or data.
oscillator	A circuit that may be crystal controlled and is used to generate a clock frequency.
parity	A technique for testing transmitting data. Typically, a binary digit is added to the data to make the sum of all the digits of the binary data either always even (even parity) or always odd (odd parity).
Phase-locked loop (PLL)	An electronic circuit that controls an ***oscillator*** so that it maintains a constant phase angle relative to a reference signal.
pinouts	The pin number assignment: the relation between the logical inputs and outputs of the PSoC device and their physical counterparts in the printed circuit board (PCB) package. Pinouts involve pin numbers as a link between schematic and PCB design (both being computer generated files) and may also involve pin names.
port	A group of pins, usually eight.
Power on reset (POR)	A circuit that forces the PSoC device to reset when the voltage is lower than a pre-set level. This is a type of hardware reset.
PSoC®	Cypress Semiconductor's PSoC® is a registered trademark and Programmable System-on-Chip™ is a trademark of Cypress.
PSoC Designer™	The software for Cypress' Programmable System-on-Chip technology.
pulse width modulator (PWM)	An output in the form of duty cycle which varies as a function of the applied measurand
RAM	An acronym for random access memory. A data-storage device from which data can be read out and new data can be written in.
register	A storage device with a specific capacity, such as a bit or byte.
reset	A means of bringing a system back to a know state. See hardware reset and software reset.
ROM	An acronym for read only memory. A data-storage device from which data can be read out, but new data cannot be written in.
serial	1. Pertaining to a process in which all events occur one after the other. 2. Pertaining to the sequential or consecutive occurrence of two or more related activities in a single device or channel.
settling time	The time it takes for an output signal or value to stabilize after the input has changed from one value to another.

Document History Page (continued)

Document Title: CY8C29466/CY8C29566/CY8C29666/CY8C29866, PSoC® Programmable System-on-Chip™ Document Number: 38-12013				
Revision	**ECN**	**Origin of Change**	**Submission Date**	**Description of Change**
*N	2902396	NJF	03/30/2010	Updated and content in Digital System Updated Cypress website links. Removed reference to PSoC Designer 4.4 in PSoC Designer Software Subsystems Added $T_{BAKETEMP}$ and $T_{BAKETIME}$ parameters in Absolute Maximum Ratings Updated AC Chip-Level Specifications Changed unit for SPIS function to ns in AC Digital Block Specifications Updated notes in Packaging Information and package diagrams. Updated Solder Reflow Specifications Updated Emulation and Programming Accessories Removed Third Party Tools and Build a PSoC Emulator into Your Board. Updated Ordering Information and Ordering Code Definitions.
*O	2940410	YJI	05/31/2010	Updated content to match current style guide and datasheet template. No technical updates.
*P	3044869	NJF	10/01/2010	Added PSoC Device Characteristics table . Added DC I^2C Specifications table. Added F_{32K_U} max limit. Added Tjit_IMO specification, removed existing jitter specifications. Updated Analog reference tables. Updated Units of Measure, Acronyms, Glossary, and References sections. Updated solder reflow specifications. No specific changes were made to AC Digital Block Specifications table and I^2C Timing Diagram. They were updated for clearer understanding. Updated Figure 13 since the labelling for y-axis was incorrect. Template and styles update. Removed footnote reference for “Solder Reflow Peak Temperature” table.
*Q	3017427	GDK	11/08/10	Removed the pruned part “CY8C29666-24LFXI” from the Ordering Information and Accessories (Emulation and Programming).
*R	3263978	NJF	05/23/11	Updated Logic Block Diagram. Updated Solder Reflow Specifications.
*S	3301676	NJF	07/04/11	Fixed page numbering error on footer.
*T	3358177	NJF / GIR / BTK / NPD	09/26/11	Updated max value for ‘0b011’ under Table 22 on page 33. Updated V_{REFHI} values for ‘0b100’ under Table 21 on page 29. Incorrect flash/SRAM size mentioned under section PSoC Core on page 4. Changed paragraph “Memory uses 16 KB of flash for program storage, 256 bytes of SRAM for data storage, and up to 2 KB of EEPROM emulated using the flash. Program flash uses four protection levels on blocks of 64 bytes, allowing customized software information protection (IP)” to “Memory uses 16 KB of flash for program storage, 256 bytes of SRAM for data storage, and up to 2 KB of EEPROM emulated using the flash. Program flash uses four protection levels on blocks of 64 bytes, allowing customized software information protection (IP)”. Removed package diagram spec 001-12919 as there is no MPN mapped to this package. The text “Pin must be left floating” is included under Description of NC pin in Table 6 on page 14.
*U	3598291	LURE / XZNG	04/24/2012	Changed the PWM description string from “8- to 32-bit” to “8- and 16-bit”. Updated package diagrams 001-13191 and 51-85048.