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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	M8C
Core Size	8-Bit
Speed	24MHz
Connectivity	I ² C, SPI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	44
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.25V
Data Converters	A/D 12x14b; D/A 4x9b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-BSSOP (0.295", 7.50mm Width)
Supplier Device Package	48-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c29666-24pvxi

More Information

Cypress provides a wealth of data at www.cypress.com to help you to select the right PSoC device for your design, and to help you to quickly and effectively integrate the device into your design. For a comprehensive list of resources, see the knowledge base article “How to Design with PSoC® 1, PowerPSoC®, and PLC – KBA88292”. Following is an abbreviated list for PSoC 1:

- Overview: PSoC Portfolio, PSoC Roadmap
- Product Selectors: [PSoC 1](#), [PSoC 3](#), [PSoC 4](#), [PSoC 5LP](#)
- In addition, PSoC Designer includes a device selection tool.
- Application notes: Cypress offers a large number of PSoC application notes covering a broad range of topics, from basic to advanced level. Recommended application notes for getting started with PSoC 1 are:
 - [Getting Started with PSoC® 1 – AN75320](#)
 - [PSoC® 1 - Getting Started with GPIO – AN2094](#)
 - [PSoC® 1 Analog Structure and Configuration – AN74170](#)
 - [PSoC® 1 Switched Capacitor Analog Blocks – AN2041](#)
 - [Selecting Analog Ground and Reference – AN2219](#)

Note: For CY8C29X66 devices related Application note please click [here](#).

- Development Kits:
 - [CY3210-PSocEval1](#) supports all PSoC 1 Mixed-Signal Array families, including automotive, except CY8C25/26xxx devices. The kit includes an LCD module, potentiometer, LEDs, and breadboarding space.
 - [CY3214-PSocEvalUSB](#) features a development board for the CY8C24x94 PSoC device. Special features of the board include USB and CapSense development and debugging support.

Note: For CY8C29X66 devices related Development Kits please click [here](#).

The [MiniProg1](#) and [MiniProg3](#) devices provide interfaces for flash programming and debug.

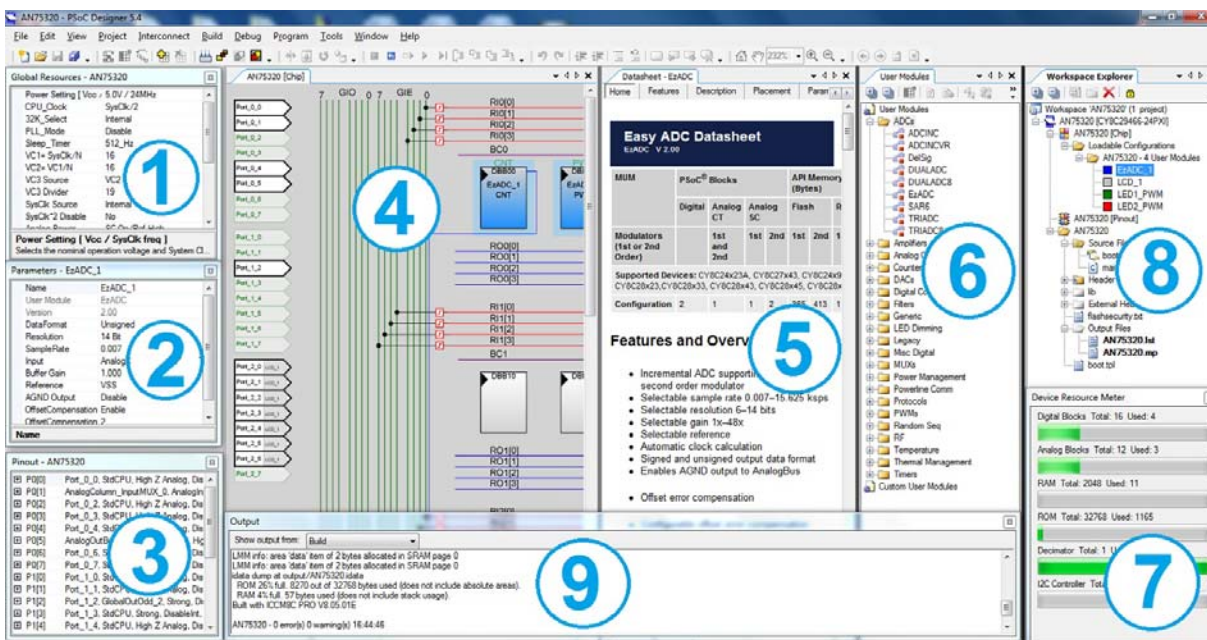
PSoC Designer

[PSoC Designer](#) is a free Windows-based Integrated Design Environment (IDE). Develop your applications using a library of pre-characterized analog and digital peripherals in a drag-and-drop design environment. Then, customize your design leveraging the dynamically generated API libraries of code. [Figure 1](#) shows PSoC Designer windows. **Note:** This is not the default view.

1. **Global Resources** – all device hardware settings.
2. **Parameters** – the parameters of the currently selected User Modules.
3. **Pinout** – information related to device pins.
4. **Chip-Level Editor** – a diagram of the resources available on the selected chip.
5. **Datasheet** – the datasheet for the currently selected UM
6. **User Modules** – all available User Modules for the selected device.
7. **Device Resource Meter** – device resource usage for the current project configuration.
8. **Workspace** – a tree level diagram of files associated with the project.
9. **Output** – output from project build and debug operations.

Note: For detailed information on PSoC Designer, go to PSoC® Designer > Help > Documentation > Designer Specific Documents > IDE User Guide.

Figure 1. PSoC Designer Layout



PSoC Functional Overview

The PSoC family consists of many Programmable System-on-Chip controller devices. These devices are designed to replace multiple traditional microcontroller unit (MCU)-based system components with one, low-cost single-chip programmable device. PSoC devices include configurable blocks of analog and digital logic, as well as programmable interconnects. This architecture allows you to create customized peripheral configurations that match the requirements of each individual application. Additionally, a fast central processing unit (CPU), flash program memory, SRAM data memory, and configurable I/O are included in a range of convenient pinouts and packages.

The PSoC architecture, as illustrated in the [Logic Block Diagram on page 1](#), consists of four main areas: PSoC core, digital system, analog system, and system resources. Configurable global busing allows all of the device resources to be combined into a complete custom system. The PSoC CY8C29x66 family can have up to five I/O ports that connect to the global digital and analog interconnects, providing access to 8 digital blocks and 12 analog blocks.

PSoC Core

The PSoC core is a powerful engine that supports a rich feature set. The core includes a CPU, memory, clocks, and configurable GPIOs.

The M8C CPU core is a powerful processor with speeds up to 24 MHz, providing a 4 million instructions per second (MIPS) 8-bit Harvard-architecture microprocessor. The CPU uses an interrupt controller with 17 vectors, to simplify programming of real-time embedded events. Program execution is timed and protected using the included sleep and watchdog timers (WDT).

Memory uses 32 KB of flash for program storage, 2 KB of SRAM for data storage, and up to 2 KB of EEPROM emulated using the flash. Program flash uses four protection levels on blocks of 64 bytes, allowing customized software information protection (IP).

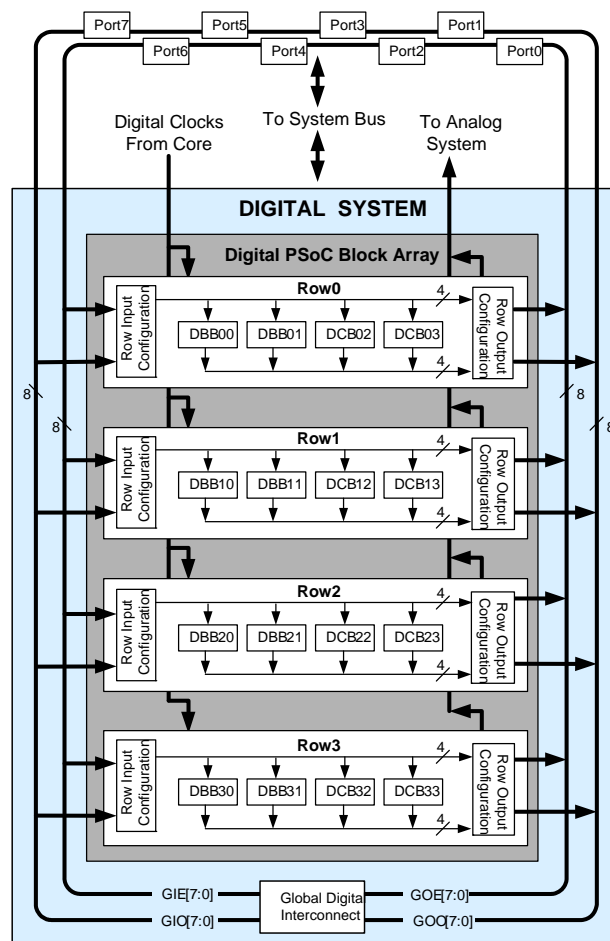
The PSoC device incorporates flexible internal clock generators, including a 24 MHz internal main oscillator (IMO) accurate to 5% [2] over temperature and voltage. The 24 MHz IMO can also be doubled to 48 MHz for use by the digital system. A low-power 32 kHz internal low speed oscillator (ILO) is provided for the sleep timer and WDT. If crystal accuracy is desired, the 32.768 kHz external crystal oscillator (ECO) is available for use as a real-time clock (RTC) and can optionally generate a crystal-accurate 24 MHz system clock using a PLL. The clocks, together with programmable clock dividers (as a system resource), provide the flexibility to integrate almost any timing requirement into the PSoC device.

PSoC GPIOs provide connection to the CPU, and digital and analog resources of the device. Each pin's drive mode may be selected from eight options, allowing great flexibility in external interfacing. Every pin also has the capability to generate a system interrupt on high level, low level, and change from last read.

Digital System

The digital system is composed of 16 digital PSoC blocks. Each block is an 8-bit resource that can be used alone or combined with other blocks to form 8-, 16-, 24-, and 32-bit peripherals, which are called user modules.

Figure 2. Digital System Block Diagram



Note

- Errata:** When the device is operated within 0 °C to 70 °C, the frequency tolerance is reduced to $\pm 2.5\%$, but if operated at extreme temperature (below 0 °C or above 70 °C), frequency tolerance deviates from $\pm 2.5\%$ to $\pm 5\%$. For more information, see [Errata on page 63](#).

Additional System Resources

System resources, some of which were previously listed, provide additional capability useful to complete systems. Additional resources include a multiplier, decimator, switch mode pump, low-voltage detection, and power-on-reset (POR).

- Digital clock dividers provide three customizable clock frequencies for use in applications. The clocks can be routed to both the digital and analog systems. Additional clocks can be generated using digital PSoC blocks as clock dividers.
- Multiply accumulate (MAC) provides a fast 8-bit multiplier with 32-bit accumulate, to assist in general math and digital filters.
- The decimator provides a custom hardware filter for digital signal processing applications including the creation of delta sigma ADCs.
- The I²C module provides 100 and 400 kHz communication over two wires. Slave, master, and multi-master modes are all supported.
- LVD interrupts can signal the application of falling voltage levels, while the advanced POR circuit eliminates the need for a system supervisor.
- An internal 1.3 V reference provides an absolute reference for the analog system, including ADCs and DACs.
- An integrated switch-mode pump (SMP) generates normal operating voltages from a single 1.2 V battery cell, providing a low cost boost converter.

PSoC Device Characteristics

Depending on your PSoC device characteristics, the digital and analog systems can have 16, 8, or 4 digital blocks and 12, 6, or 4 analog blocks. The following table lists the resources available for specific PSoC device groups. The PSoC device covered by this datasheet is highlighted.

Table 1. PSoC Device Characteristics

PSoC Part Number	Digital I/O	Digital Rows	Digital Blocks	Analog Inputs	Analog Outputs	Analog Columns	Analog Blocks	SRAM Size	Flash Size
CY8C29x66	up to 64	4	16	up to 12	4	4	12	2 K	32 K
CY8C28xxx	up to 44	up to 3	up to 12	up to 44	up to 4	up to 6	up to 12 + 4 ^[3]	1 K	16 K
CY8C27x43	up to 44	2	8	up to 12	4	4	12	256	16 K
CY8C24x94	up to 56	1	4	up to 48	2	2	6	1 K	16 K
CY8C24x23A	up to 24	1	4	up to 12	2	2	6	256	4 K
CY8C23x33	up to 26	1	4	up to 12	2	2	4	256	8 K
CY8C22x45	up to 38	2	8	up to 38	0	4	6 ^[3]	1 K	16 K
CY8C21x45	up to 24	1	4	up to 24	0	4	6 ^[3]	512	8 K
CY8C21x34	up to 28	1	4	up to 28	0	2	4 ^[3]	512	8 K
CY8C21x23	up to 16	1	4	up to 8	0	2	4 ^[3]	256	4 K
CY8C20x34	up to 28	0	0	up to 28	0	0	3 ^[3,4]	512	8 K
CY8C20xx6	up to 36	0	0	up to 36	0	0	3 ^[3,4]	up to 2 K	up to 32 K

Notes

3. Limited analog functionality.

4. Two analog blocks and one CapSense®.

Organize and Connect

You build signal chains at the chip level by interconnecting user modules to each other and the I/O pins. You perform the selection, configuration, and routing so that you have complete control over all on-chip resources.

Generate, Verify, and Debug

When you are ready to test the hardware configuration or move on to developing code for the project, you perform the “Generate Configuration Files” step. This causes PSoC Designer to generate source code that automatically configures the device to your specification and provides the software for the system. The generated code provides application programming interfaces (APIs) with high-level functions to control and respond to hardware events at run time and interrupt service routines that you can adapt as needed.

A complete code development environment allows you to develop and customize your applications in either C, assembly language, or both.

The last step in the development process takes place inside PSoC Designer’s debugger (access by clicking the Connect icon). PSoC Designer downloads the HEX image to the ICE where it runs at full speed. PSoC Designer debugging capabilities rival those of systems costing many times more. In addition to traditional single-step, run-to-breakpoint and watch-variable features, the debug interface provides a large trace buffer and allows you to define complex breakpoint events that include monitoring address and data bus values, memory locations and external signals.

Table 5. 48-Pin Part Pinout (QFN) [9]

Pin No.	Type		Pin Name	Description
	Digital	Analog		
1	I/O	I	P2[3]	Direct switched capacitor block input
2	I/O	I	P2[1]	Direct switched capacitor block input
3	I/O		P4[7]	
4	I/O		P4[5]	
5	I/O		P4[3]	
6	I/O		P4[1]	
7	Power		SMP	Switch mode pump (SMP) connection to external components required
8	I/O		P3[7]	
9	I/O		P3[5]	
10	I/O		P3[3]	
11	I/O		P3[1]	
12	I/O		P5[3]	
13	I/O		P5[1]	
14	I/O		P1[7]	I ² C SCL
15	I/O		P1[5]	I ² C SDA
16	I/O		P1[3]	
17	I/O		P1[1]	Crystal (XTALin), I ² C SCL, ISSP-SCLK ^[8]
18	Power		V _{SS}	Ground connection
19	I/O		P1[0]	Crystal (XTALout), I ² C SDA, ISSP-SDATA ^[8]
20	I/O		P1[2]	
21	I/O		P1[4]	Optional EXTCLK
22	I/O		P1[6]	
23	I/O		P5[0]	
24	I/O		P5[2]	
25	I/O		P3[0]	
26	I/O		P3[2]	
27	I/O		P3[4]	
28	I/O		P3[6]	
29	Input		XRES	Active high external reset with internal pull-down
30	I/O		P4[0]	
31	I/O		P4[2]	
32	I/O		P4[4]	
33	I/O		P4[6]	
34	I/O	I	P2[0]	Direct switched capacitor block input
35	I/O	I	P2[2]	Direct switched capacitor block input
36	I/O		P2[4]	External analog ground (AGND)
37	I/O		P2[6]	External voltage reference (VREF)
38	I/O	I	P0[0]	Analog column mux input
39	I/O	I/O	P0[2]	Analog column mux input and column output
40	I/O	I/O	P0[4]	Analog column mux input and column output
41	I/O	I	P0[6]	Analog column mux input
42	Power		V _{DD}	Supply voltage
43	I/O	I	P0[7]	Analog column mux input
44	I/O	I/O	P0[5]	Analog column mux input and column output
45	I/O	I/O	P0[3]	Analog column mux input and column output
46	I/O	I	P0[1]	Analog column mux input
47	I/O		P2[7]	
48	I/O		P2[5]	

LEGEND: A = Analog, I = Input, and O = Output.

Notes

- These are the ISSP pins, which are not High Z at POR. See the *PSoC Programmable System-on-Chip Technical Reference Manual* for details.
- The QFN package has a center pad that must be connected to ground (V_{SS}).

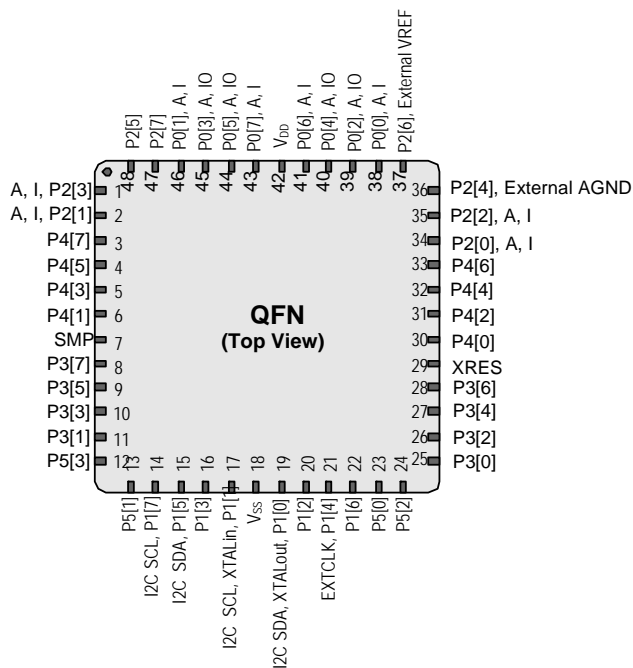
Figure 7. CY8C29666 48-Pin PSoC Device


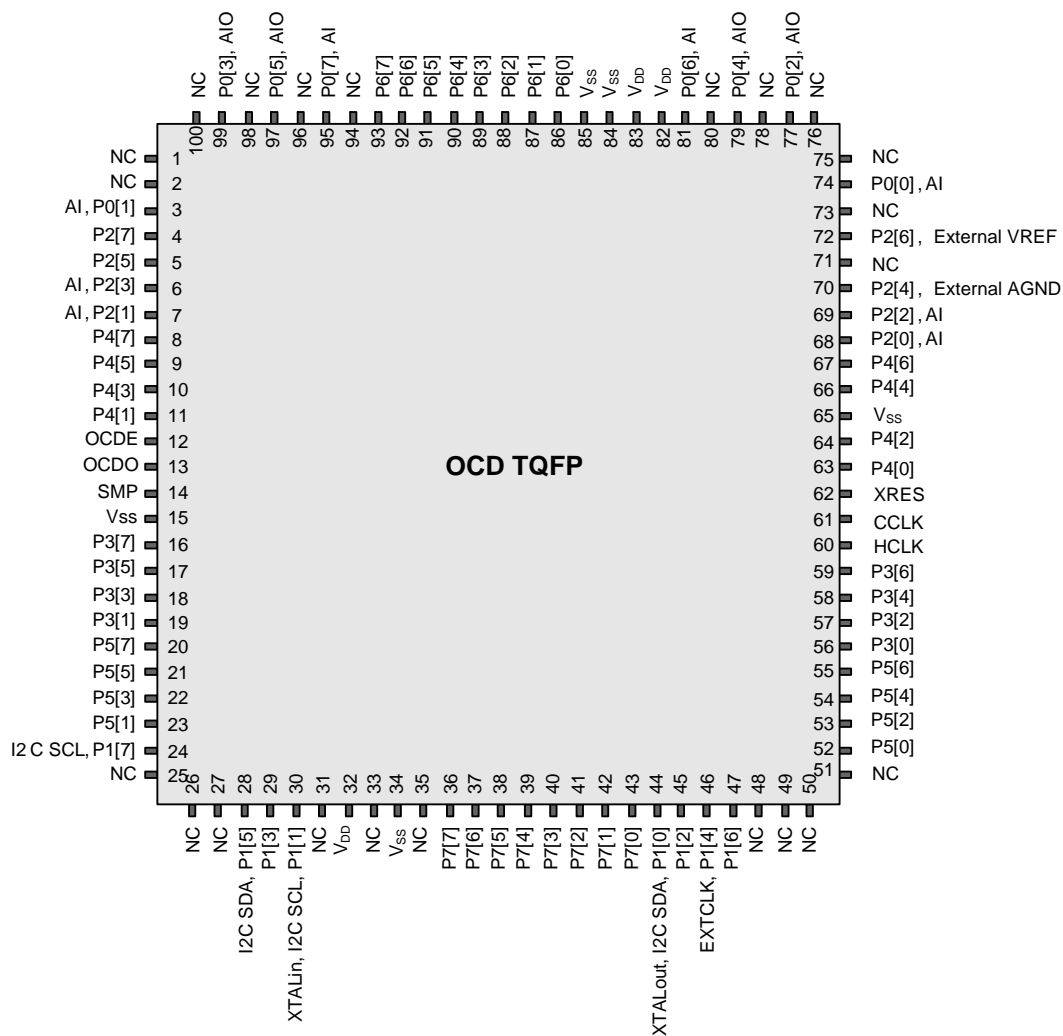
Figure 9. CY8C29000 OCD (Not for Production)


Table 10. Register Map Bank 1 Table: Configuration Space

Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access
PRT0DM0	00	RW	DBB20FN	40	RW	ASC10CR0	80	RW	RD12RI	C0	RW
PRT0DM1	01	RW	DBB20IN	41	RW	ASC10CR1	81	RW	RD12SYN	C1	RW
PRT0IC0	02	RW	DBB20OU	42	RW	ASC10CR2	82	RW	RD12IS	C2	RW
PRT0IC1	03	RW		43		ASC10CR3	83	RW	RD12LT0	C3	RW
PRT1DM0	04	RW	DBB21FN	44	RW	ASD11CR0	84	RW	RD12LT1	C4	RW
PRT1DM1	05	RW	DBB21IN	45	RW	ASD11CR1	85	RW	RD12RO0	C5	RW
PRT1IC0	06	RW	DBB21OU	46	RW	ASD11CR2	86	RW	RD12RO1	C6	RW
PRT1IC1	07	RW		47		ASD11CR3	87	RW		C7	
PRT2DM0	08	RW	DCB22FN	48	RW	ASC12CR0	88	RW	RD13RI	C8	RW
PRT2DM1	09	RW	DCB22IN	49	RW	ASC12CR1	89	RW	RD13SYN	C9	RW
PRT2IC0	0A	RW	DCB22OU	4A	RW	ASC12CR2	8A	RW	RD13IS	CA	RW
PRT2IC1	0B	RW		4B		ASC12CR3	8B	RW	RD13LT0	CB	RW
PRT3DM0	0C	RW	DCB23FN	4C	RW	ASD13CR0	8C	RW	RD13LT1	CC	RW
PRT3DM1	0D	RW	DCB23IN	4D	RW	ASD13CR1	8D	RW	RD13RO0	CD	RW
PRT3IC0	0E	RW	DCB23OU	4E	RW	ASD13CR2	8E	RW	RD13RO1	CE	RW
PRT3IC1	0F	RW		4F		ASD13CR3	8F	RW		CF	
PRT4DM0	10	RW	DBB30FN	50	RW	ASD20CR0	90	RW	GDI_O_IN	D0	RW
PRT4DM1	11	RW	DBB30IN	51	RW	ASD20CR1	91	RW	GDI_E_IN	D1	RW
PRT4IC0	12	RW	DBB30OU	52	RW	ASD20CR2	92	RW	GDI_O_OU	D2	RW
PRT4IC1	13	RW		53		ASD20CR3	93	RW	GDI_E_OU	D3	RW
PRT5DM0	14	RW	DBB31FN	54	RW	ASC21CR0	94	RW		D4	
PRT5DM1	15	RW	DBB31IN	55	RW	ASC21CR1	95	RW		D5	
PRT5IC0	16	RW	DBB31OU	56	RW	ASC21CR2	96	RW		D6	
PRT5IC1	17	RW		57		ASC21CR3	97	RW		D7	
PRT6DM0	18	RW	DCB32FN	58	RW	ASD22CR0	98	RW		D8	
PRT6DM1	19	RW	DCB32IN	59	RW	ASD22CR1	99	RW		D9	
PRT6IC0	1A	RW	DCB32OU	5A	RW	ASD22CR2	9A	RW		DA	
PRT6IC1	1B	RW		5B		ASD22CR3	9B	RW		DB	
PRT7DM0	1C	RW	DCB33FN	5C	RW	ASC23CR0	9C	RW		DC	
PRT7DM1	1D	RW	DCB33IN	5D	RW	ASC23CR1	9D	RW	OSC_GO_EN	DD	RW
PRT7IC0	1E	RW	DCB33OU	5E	RW	ASC23CR2	9E	RW	OSC_CR4	DE	RW
PRT7IC1	1F	RW		5F		ASC23CR3	9F	RW	OSC_CR3	DF	RW
DBB00FN	20	RW	CLK_CR0	60	RW		A0		OSC_CR0	E0	RW
DBB00IN	21	RW	CLK_CR1	61	RW		A1		OSC_CR1	E1	RW
DBB00OU	22	RW	ABF_CR0	62	RW		A2		OSC_CR2	E2	RW
	23		AMD_CR0	63	RW		A3		VLT_CR	E3	RW
DBB01FN	24	RW		64			A4		VLT_CMP	E4	R
DBB01IN	25	RW		65			A5			E5	
DBB01OU	26	RW	AMD_CR1	66	RW		A6			E6	
	27		ALT_CR0	67	RW		A7		DEC_CR2	E7	RW
DCB02FN	28	RW	ALT_CR1	68	RW		A8		IMO_TR	E8	W
DCB02IN	29	RW	CLK_CR2	69	RW		A9		ILO_TR	E9	W
DCB02OU	2A	RW		6A			AA		BDG_TR	EA	RW
	2B			6B			AB		ECO_TR	EB	W
DCB03FN	2C	RW	TMP_DR0	6C	RW		AC			EC	
DCB03IN	2D	RW	TMP_DR1	6D	RW		AD			ED	
DCB03OU	2E	RW	TMP_DR2	6E	RW		AE			EE	
	2F		TMP_DR3	6F	RW		AF			EF	
DBB10FN	30	RW	ACB00CR3	70	RW	RD10RI	B0	RW		F0	
DBB10IN	31	RW	ACB00CR0	71	RW	RD10SYN	B1	RW		F1	
DBB10OU	32	RW	ACB00CR1	72	RW	RD10IS	B2	RW		F2	
	33		ACB00CR2	73	RW	RD10LT0	B3	RW		F3	
DBB11FN	34	RW	ACB01CR3	74	RW	RD10LT1	B4	RW		F4	
DBB11IN	35	RW	ACB01CR0	75	RW	RD10RO0	B5	RW		F5	
DBB11OU	36	RW	ACB01CR1	76	RW	RD10RO1	B6	RW		F6	
	37		ACB01CR2	77	RW		B7		CPU_F	F7	RL
DCB12FN	38	RW	ACB02CR3	78	RW	RD11RI	B8	RW		F8	
DCB12IN	39	RW	ACB02CR0	79	RW	RD11SYN	B9	RW		F9	
DCB12OU	3A	RW	ACB02CR1	7A	RW	RD11IS	BA	RW	FLS_PR1	FA	RW
	3B		ACB02CR2	7B	RW	RD11LT0	BB	RW		FB	
DCB13FN	3C	RW	ACB03CR3	7C	RW	RD11LT1	BC	RW		FC	
DCB13IN	3D	RW	ACB03CR0	7D	RW	RD11RO0	BD	RW		FD	
DCB13OU	3E	RW	ACB03CR1	7E	RW	RD11RO1	BE	RW	CPU_SCR1	FE	#
	3F		ACB03CR2	7F	RW		BF		CPU_SCR0	FF	#

Blank fields are Reserved and should not be accessed.

Access is bit specific.

Table 16. 3.3-V DC Operational Amplifier Specifications

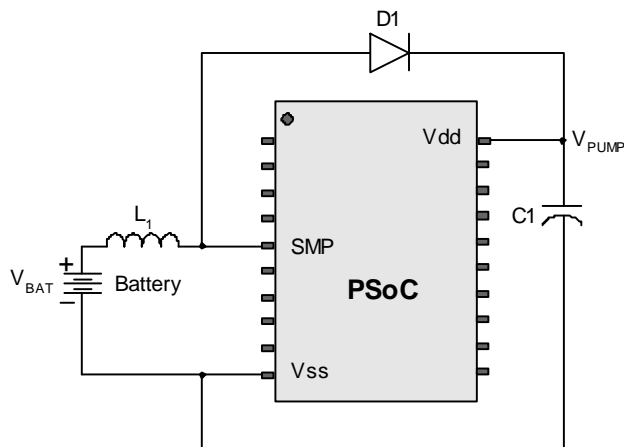
Symbol	Description	Min	Typ	Max	Unit	Notes
V_{OSOA}	Input offset voltage (absolute value)	–	1.4	10	mV	Power = High, Opamp bias = High setting is not allowed for 3.3 V V_{DD} operation.
	Power = Low, Opamp bias = Low	–	1.4	10	mV	
	Power = Low, Opamp bias = High	–	1.4	10	mV	
	Power = Medium, Opamp bias = Low	–	1.4	10	mV	
	Power = Medium, Opamp bias = High	–	1.4	10	mV	
	Power = High, Opamp bias = Low	–	1.4	10	mV	
	Power = High, Opamp bias = High	–	–	–	mV	
TCV_{OSOA}	Average input offset voltage drift	–	7	40	$\mu V/^{\circ}C$	
I_{EBOA}	Input leakage current (port 0 analog pins)	–	200	–	pA	Gross tested to 1 μA .
C_{INOA}	Input capacitance (port 0 analog pins)	–	4.5	9.5	pF	Package and pin dependent. Temp = 25 $^{\circ}C$
V_{CMOA}	Common mode voltage range	0	–	V_{DD}	V	The common-mode input voltage range is measured through an analog output buffer. The specification includes the limitations imposed by the characteristics of the analog output buffer.
$CMRR_{OA}$	Common mode rejection ratio	60	–	–	dB	
G_{OLOA}	Open loop gain	80	–	–	dB	
$V_{OHIGHOA}$	High output voltage swing (internal signals)	$V_{DD} - 0.01$	–	–	V	
V_{OLOWOA}	Low output voltage swing (internal signals)	–	–	0.01	V	
I_{SOA}	Supply current (including associated AGND buffer)					Power = High, Opamp bias = High setting is not allowed for 3.3 V V_{DD} operation.
	Power = Low, Opamp bias = Low	–	150	200	μA	
	Power = Low, Opamp bias = High	–	300	400	μA	
	Power = Medium, Opamp bias = Low	–	600	800	μA	
	Power = Medium, Opamp bias = High	–	1200	1600	μA	
	Power = High, Opamp bias = Low	–	2400	3200	μA	
	Power = High, Opamp bias = High	–	–	–	μA	
$PSRR_{OA}$	Supply voltage rejection ratio	54	80	–	dB	$V_{SS} \leq V_{IN} \leq (V_{DD} - 2.25)$ or $(V_{DD} - 1.25 V) \leq V_{IN} \leq V_{DD}$

DC Low-Power Comparator Specifications

Table 17 lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and $-40^{\circ}C \leq T_A \leq 85^{\circ}C$, 3.0 V to 3.6 V and $-40^{\circ}C \leq T_A \leq 85^{\circ}C$, or 2.4 V to 3.0 V and $-40^{\circ}C \leq T_A \leq 85^{\circ}C$, respectively. Typical parameters apply to 5 V at 25 $^{\circ}C$ and are for design guidance only.

Table 17. DC Low-Power Comparator Specifications

Symbol	Description	Min	Typ	Max	Unit
V_{REFLPC}	Low-power comparator (LPC) reference voltage range	0.2	–	$V_{DD} - 1$	V
I_{SLPC}	LPC supply current	–	10	40	μA
V_{OSLPC}	LPC voltage offset	–	2.5	30	mV

Figure 12. Basic Switch Mode Pump Circuit


DC Analog Reference Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, or 3.0 V to 3.6 V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, respectively. Typical parameters apply to 5 V and 3.3 V at 25°C and are for design guidance only.

The guaranteed specifications for RefHI and RefLO are measured through the analog continuous time PSoC blocks. The power levels for RefHI and RefLO refer to the analog reference control register. AGND is measured at P2[4] in AGND bypass mode. Each analog continuous time PSoC block adds a maximum of 10 mV additional offset error to guaranteed AGND specifications from the local AGND buffer. Reference control power can be set to medium or high unless otherwise noted.

Note Avoid using P2[4] for digital signaling when using an analog resource that depends on the analog reference. Some coupling of the digital signal may appear on the AGND.

Table 21. 5-V DC Analog Reference Specifications

Reference ARF_CR[5:3]	Reference Power Settings	Symbol	Reference	Description	Min	Typ	Max	Unit
0b000	RefPower = High Opamp bias = High	V_{REFHI}	Ref High	$V_{\text{DD}}/2 + \text{Bandgap}$	$V_{\text{DD}}/2 + 1.228$	$V_{\text{DD}}/2 + 1.290$	$V_{\text{DD}}/2 + 1.352$	V
		V_{AGND}	AGND	$V_{\text{DD}}/2$	$V_{\text{DD}}/2 - 0.078$	$V_{\text{DD}}/2 - 0.007$	$V_{\text{DD}}/2 + 0.063$	V
		V_{REFLO}	Ref Low	$V_{\text{DD}}/2 - \text{Bandgap}$	$V_{\text{DD}}/2 - 1.336$	$V_{\text{DD}}/2 - 1.295$	$V_{\text{DD}}/2 - 1.250$	V
	RefPower = High Opamp bias = Low	V_{REFHI}	Ref High	$V_{\text{DD}}/2 + \text{Bandgap}$	$V_{\text{DD}}/2 + 1.224$	$V_{\text{DD}}/2 + 1.293$	$V_{\text{DD}}/2 + 1.356$	V
		V_{AGND}	AGND	$V_{\text{DD}}/2$	$V_{\text{DD}}/2 - 0.056$	$V_{\text{DD}}/2 - 0.005$	$V_{\text{DD}}/2 + 0.043$	V
		V_{REFLO}	Ref Low	$V_{\text{DD}}/2 - \text{Bandgap}$	$V_{\text{DD}}/2 - 1.338$	$V_{\text{DD}}/2 - 1.298$	$V_{\text{DD}}/2 - 1.255$	V
	RefPower = Med Opamp bias = High	V_{REFHI}	Ref High	$V_{\text{DD}}/2 + \text{Bandgap}$	$V_{\text{DD}}/2 + 1.226$	$V_{\text{DD}}/2 + 1.293$	$V_{\text{DD}}/2 + 1.356$	V
		V_{AGND}	AGND	$V_{\text{DD}}/2$	$V_{\text{DD}}/2 - 0.057$	$V_{\text{DD}}/2 - 0.006$	$V_{\text{DD}}/2 + 0.044$	V
		V_{REFLO}	Ref Low	$V_{\text{DD}}/2 - \text{Bandgap}$	$V_{\text{DD}}/2 - 1.337$	$V_{\text{DD}}/2 - 1.298$	$V_{\text{DD}}/2 - 1.256$	V
	RefPower = Med Opamp bias = Low	V_{REFHI}	Ref High	$V_{\text{DD}}/2 + \text{Bandgap}$	$V_{\text{DD}}/2 + 1.226$	$V_{\text{DD}}/2 + 1.294$	$V_{\text{DD}}/2 + 1.359$	V
		V_{AGND}	AGND	$V_{\text{DD}}/2$	$V_{\text{DD}}/2 - 0.047$	$V_{\text{DD}}/2 - 0.004$	$V_{\text{DD}}/2 + 0.035$	V
		V_{REFLO}	Ref Low	$V_{\text{DD}}/2 - \text{Bandgap}$	$V_{\text{DD}}/2 - 1.338$	$V_{\text{DD}}/2 - 1.299$	$V_{\text{DD}}/2 - 1.258$	V

Table 21. 5-V DC Analog Reference Specifications (continued)

Reference ARF_CR[5:3]	Reference Power Settings	Symbol	Reference	Description	Min	Typ	Max	Unit
0b011	RefPower = High Opamp bias = High	V _{REFHI}	Ref High	3 × Bandgap	3.788	3.891	3.986	V
		V _{AGND}	AGND	2 × Bandgap	2.500	2.604	2.699	V
		V _{REFLO}	Ref Low	Bandgap	1.257	1.306	1.359	V
	RefPower = High Opamp bias = Low	V _{REFHI}	Ref High	3 × Bandgap	3.792	3.893	3.982	V
		V _{AGND}	AGND	2 × Bandgap	2.518	2.602	2.692	V
		V _{REFLO}	Ref Low	Bandgap	1.256	1.302	1.354	V
	RefPower = Med Opamp bias = High	V _{REFHI}	Ref High	3 × Bandgap	3.795	3.894	3.993	V
		V _{AGND}	AGND	2 × Bandgap	2.516	2.603	2.698	V
		V _{REFLO}	Ref Low	Bandgap	1.256	1.303	1.353	V
	RefPower = Med Opamp bias = Low	V _{REFHI}	Ref High	3 × Bandgap	3.792	3.895	3.986	V
		V _{AGND}	AGND	2 × Bandgap	2.522	2.602	2.685	V
		V _{REFLO}	Ref Low	Bandgap	1.255	1.301	1.350	V
0b100	RefPower = High Opamp bias = High	V _{REFHI}	Ref High	2 × Bandgap + P2[6] (P2[6] = 1.3 V)	2.495 + P2[6]	2.586 + P2[6]	2.657 + P2[6]	V
		V _{AGND}	AGND	2 × Bandgap	2.502	2.604	2.719	V
		V _{REFLO}	Ref Low	2 × Bandgap – P2[6] (P2[6] = 1.3 V)	2.531 – P2[6]	2.611 – P2[6]	2.681 – P2[6]	V
	RefPower = High Opamp bias = Low	V _{REFHI}	Ref High	2 × Bandgap + P2[6] (P2[6] = 1.3 V)	2.500 + P2[6]	2.591 + P2[6]	2.662 + P2[6]	V
		V _{AGND}	AGND	2 × Bandgap	2.519	2.602	2.693	V
		V _{REFLO}	Ref Low	2 × Bandgap – P2[6] (P2[6] = 1.3 V)	2.530 – P2[6]	2.605 – P2[6]	2.666 – P2[6]	V
	RefPower = Med Opamp bias = High	V _{REFHI}	Ref High	2 × Bandgap + P2[6] (P2[6] = 1.3 V)	2.503 + P2[6]	2.592 + P2[6]	2.662 + P2[6]	V
		V _{AGND}	AGND	2 × Bandgap	2.517	2.603	2.698	V
		V _{REFLO}	Ref Low	2 × Bandgap – P2[6] (P2[6] = 1.3 V)	2.529 – P2[6]	2.606 – P2[6]	2.665 – P2[6]	V
	RefPower = Med Opamp bias = Low	V _{REFHI}	Ref High	2 × Bandgap + P2[6] (P2[6] = 1.3 V)	2.505 + P2[6]	2.594 + P2[6]	2.665 + P2[6]	V
		V _{AGND}	AGND	2 × Bandgap	2.525	2.602	2.685	V
		V _{REFLO}	Ref Low	2 × Bandgap – P2[6] (P2[6] = 1.3 V)	2.528 – P2[6]	2.603 – P2[6]	2.661 – P2[6]	V

Table 22. 3.3-V DC Analog Reference Specifications (continued)

Reference ARF_CR[5:3]	Reference Power Settings	Symbol	Reference	Description	Min	Typ	Max	Unit
0b001	RefPower = High Opamp bias = High	V _{REFHI}	Ref High	P2[4]+P2[6] (P2[4] = V _{DD} /2, P2[6] = 0.5 V)	P2[4] + P2[6] – 0.098	P2[4] + P2[6] – 0.018	P2[4] + P2[6] + 0.055	V
		V _{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V _{REFLO}	Ref Low	P2[4] – P2[6] (P2[4] = V _{DD} /2, P2[6] = 0.5 V)	P2[4] – P2[6] – 0.055	P2[4] – P2[6] + 0.013	P2[4] – P2[6] + 0.086	V
	RefPower = High Opamp bias = Low	V _{REFHI}	Ref High	P2[4] + P2[6] (P2[4] = V _{DD} /2, P2[6] = 0.5 V)	P2[4] + P2[6] – 0.082	P2[4] + P2[6] – 0.011	P2[4] + P2[6] + 0.050	V
		V _{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V _{REFLO}	Ref Low	P2[4] – P2[6] (P2[4] = V _{DD} /2, P2[6] = 0.5 V)	P2[4] – P2[6] – 0.037	P2[4] – P2[6] + 0.006	P2[4] – P2[6] + 0.054	V
	RefPower = Med Opamp bias = High	V _{REFHI}	Ref High	P2[4] + P2[6] (P2[4] = V _{DD} /2, P2[6] = 0.5 V)	P2[4] + P2[6] – 0.079	P2[4] + P2[6] – 0.012	P2[4] + P2[6] + 0.047	V
		V _{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V _{REFLO}	Ref Low	P2[4]–P2[6] (P2[4] = V _{DD} /2, P2[6] = 0.5 V)	P2[4] – P2[6] – 0.038	P2[4] – P2[6] + 0.006	P2[4] – P2[6] + 0.057	V
	RefPower = Med Opamp bias = Low	V _{REFHI}	Ref High	P2[4]+P2[6] (P2[4] = V _{DD} /2, P2[6] = 0.5 V)	P2[4] + P2[6] – 0.080	P2[4] + P2[6] – 0.008	P2[4] + P2[6] + 0.055	V
		V _{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V _{REFLO}	Ref Low	P2[4]–P2[6] (P2[4] = V _{DD} /2, P2[6] = 0.5 V)	P2[4] – P2[6] – 0.032	P2[4] – P2[6] + 0.003	P2[4] – P2[6] + 0.042	V

Table 22. 3.3-V DC Analog Reference Specifications (continued)

Reference ARF_CR[5:3]	Reference Power Settings	Symbol	Reference	Description	Min	Typ	Max	Unit
0b010	RefPower = High Opamp bias = High	V _{REFHI}	Ref High	V _{DD}	V _{DD} – 0.06	V _{DD} – 0.010	V _{DD}	V
		V _{AGND}	AGND	V _{DD} /2	V _{DD} /2 – 0.05	V _{DD} /2 – 0.002	V _{DD} /2 + 0.040	V
		V _{REFLO}	Ref Low	V _{SS}	V _{SS}	V _{SS} + 0.009	V _{SS} + 0.056	V
	RefPower = High Opamp bias = Low	V _{REFHI}	Ref High	V _{DD}	V _{DD} – 0.060	V _{DD} – 0.006	V _{DD}	V
		V _{AGND}	AGND	V _{DD} /2	V _{DD} /2 – 0.028	V _{DD} /2 – 0.001	V _{DD} /2 + 0.025	V
		V _{REFLO}	Ref Low	V _{SS}	V _{SS}	V _{SS} + 0.005	V _{SS} + 0.034	V
	RefPower = Med Opamp bias = High	V _{REFHI}	Ref High	V _{DD}	V _{DD} – 0.058	V _{DD} – 0.008	V _{DD}	V
		V _{AGND}	AGND	V _{DD} /2	V _{DD} /2 – 0.037	V _{DD} /2 – 0.002	V _{DD} /2 + 0.033	V
		V _{REFLO}	Ref Low	V _{SS}	V _{SS}	V _{SS} + 0.007	V _{SS} + 0.046	V
	RefPower = Med Opamp bias = Low	V _{REFHI}	Ref High	V _{DD}	V _{DD} – 0.057	V _{DD} – 0.006	V _{DD}	V
		V _{AGND}	AGND	V _{DD} /2	V _{DD} /2 – 0.025	V _{DD} /2 – 0.001	V _{DD} /2 + 0.022	V
		V _{REFLO}	Ref Low	V _{SS}	V _{SS}	V _{SS} + 0.004	V _{SS} + 0.030	V
0b011	All power settings. Not allowed for 3.3 V	–	–	–	–	–	–	–
0b100	All power settings. Not allowed for 3.3 V	–	–	–	–	–	–	–

Table 22. 3.3-V DC Analog Reference Specifications (continued)

Reference ARF_CR[5:3]	Reference Power Settings	Symbol	Reference	Description	Min	Typ	Max	Unit
0b101	RefPower = High Opamp bias = High	V _{REFHI}	Ref High	P2[4] + Band-Gap (P2[4] = V _{DD} /2)	P2[4] + 1.213	P2[4] + 1.291	P2[4] + 1.367	V
		V _{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	V
		V _{REFLO}	Ref Low	P2[4] – Band-Gap (P2[4] = V _{DD} /2)	P2[4] – 1.333	P2[4] – 1.294	P2[4] – 1.208	V
	RefPower = High Opamp bias = Low	V _{REFHI}	Ref High	P2[4] + Band-Gap (P2[4] = V _{DD} /2)	P2[4] + 1.217	P2[4] + 1.294	P2[4] + 1.368	V
		V _{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	V
		V _{REFLO}	Ref Low	P2[4] – Band-Gap (P2[4] = V _{DD} /2)	P2[4] – 1.320	P2[4] – 1.296	P2[4] – 1.261	V
	RefPower = Med Opamp bias = High	V _{REFHI}	Ref High	P2[4] + Band-Gap (P2[4] = V _{DD} /2)	P2[4] + 1.217	P2[4] + 1.294	P2[4] + 1.369	V
		V _{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	V
		V _{REFLO}	Ref Low	P2[4] – Band-Gap (P2[4] = V _{DD} /2)	P2[4] – 1.322	P2[4] – 1.297	P2[4] – 1.262	V
	RefPower = Med Opamp bias = Low	V _{REFHI}	Ref High	P2[4] + Band-Gap (P2[4] = V _{DD} /2)	P2[4] + 1.219	P2[4] + 1.295	P2[4] + 1.37	V
		V _{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	V
		V _{REFLO}	Ref Low	P2[4] – Band-Gap (P2[4] = V _{DD} /2)	P2[4] – 1.324	P2[4] – 1.297	P2[4] – 1.262	V
0b110	RefPower = High Opamp bias = High	V _{REFHI}	Ref High	2 × BandGap	2.507	2.598	2.698	V
		V _{AGND}	AGND	BandGap	1.203	1.307	1.424	V
		V _{REFLO}	Ref Low	Vss	Vss	Vss + 0.012	Vss + 0.067	V
	RefPower = High Opamp bias = Low	V _{REFHI}	Ref High	2 × BandGap	2.516	2.598	2.683	V
		V _{AGND}	AGND	BandGap	1.241	1.303	1.376	V
		V _{REFLO}	Ref Low	Vss	Vss	Vss + 0.007	Vss + 0.040	V
	RefPower = Med Opamp bias = High	V _{REFHI}	Ref High	2 × BandGap	2.510	2.599	2.693	V
		V _{AGND}	AGND	BandGap	1.240	1.305	1.374	V
		V _{REFLO}	Ref Low	Vss	Vss	Vss + 0.008	Vss + 0.048	V
	RefPower = Med Opamp bias = Low	V _{REFHI}	Ref High	2 × BandGap	2.515	2.598	2.683	V
		V _{AGND}	AGND	BandGap	1.258	1.302	1.355	V
		V _{REFLO}	Ref Low	Vss	Vss	Vss + 0.005	Vss + 0.03	V
0b111	All power settings. Not allowed for 3.3 V.	–	–	–	–	–	–	–

AC Electrical Characteristics

AC Chip-Level Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, or 3.0 V to 3.6 V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, respectively. Typical parameters apply to 5 V and 3.3 V at 25°C and are for design guidance only.

Note See the individual user module datasheets for information on maximum frequencies for user modules.

Table 29. AC Chip-Level Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F _{IMO24} ^[21]	Internal main oscillator (IMO) frequency for 24 MHz	22.8	24	25.2 ^[22,23]	MHz	Trimmed for 5 V or 3.3 V operation using factory trim values. See Figure 11 on page 21 . SLIMO Mode = 0.
F _{IMO6}	IMO frequency for 6 MHz	5.5	6	6.5 ^[22,23]	MHz	Trimmed for 5 V or 3.3 V operation using factory trim values. See Figure 11 on page 21 . SLIMO Mode = 1.
F _{CPU1}	CPU frequency (5 V Nominal)	0.0914	24	25.2 ^[22]	MHz	SLIMO Mode = 0.
F _{CPU2}	CPU frequency (3.3 V Nominal)	0.0914	12	12.6 ^[23]	MHz	SLIMO Mode = 0.
F _{48M}	Digital PSoC block frequency	0	48	50.4 ^[22,24]	MHz	Refer to AC Digital Block Specifications on page 45 .
F _{24M}	Digital PSoC block frequency	0	24	25.2 ^[24]	MHz	
F _{32K1}	Internal low speed oscillator frequency	15	32	64	kHz	
F _{32K2}	External crystal oscillator	—	32.768	—	kHz	Accuracy is capacitor and crystal dependent. 50% duty cycle
F _{32K_U}	Internal low speed oscillator (ILO) untrimmed frequency	5	—	100	kHz	After a reset and before the M8C starts to run, the ILO is not trimmed. See the System Resets section of the PSoC Technical Reference Manual for details on this timing
F _{PLL}	PLL frequency	—	23.986	—	MHz	A multiple (x732) of crystal frequency
T _{PLLSLEW}	PLL lock time	0.5	—	10	ms	
T _{PLLSLEWLOW}	PLL lock time for low gain setting	0.5	—	50	ms	
T _{OS}	External crystal oscillator startup to 1%	—	250	500	ms	
T _{OSACC}	External crystal oscillator startup to 100 ppm	—	300	600	ms	The crystal oscillator frequency is within 100 ppm of its final value by the end of the T _{OSACC} period. Correct operation assumes a properly loaded 1 μW maximum drive level 32.768 kHz crystal. $3.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$.
T _{XRST}	External reset pulse width	10	—	—	μs	
DC _{24M}	24 MHz duty cycle	40	50	60	%	
DC _{ILO}	Internal low speed oscillator duty cycle	20	50	80	%	
Step _{24M}	24 MHz trim step size	—	50	—	kHz	
F _{out48M}	48 MHz output frequency	45.6	48.0	50.4 ^[22, 23]	MHz	Trimmed. Using factory trim values
F _{MAX}	Maximum frequency of signal on row input or row output.	—	—	12.3	MHz	

Notes

21. **Errata:** When the device is operated within 0°C to 70°C , the frequency tolerance is reduced to $\pm 2.5\%$, but if operated at extreme temperature (below 0°C or above 70°C), frequency tolerance deviates from $\pm 2.5\%$ to $\pm 5\%$. For more information, see [Errata on page 63](#).

22. $4.75\text{ V} < V_{DD} < 5.25\text{ V}$.

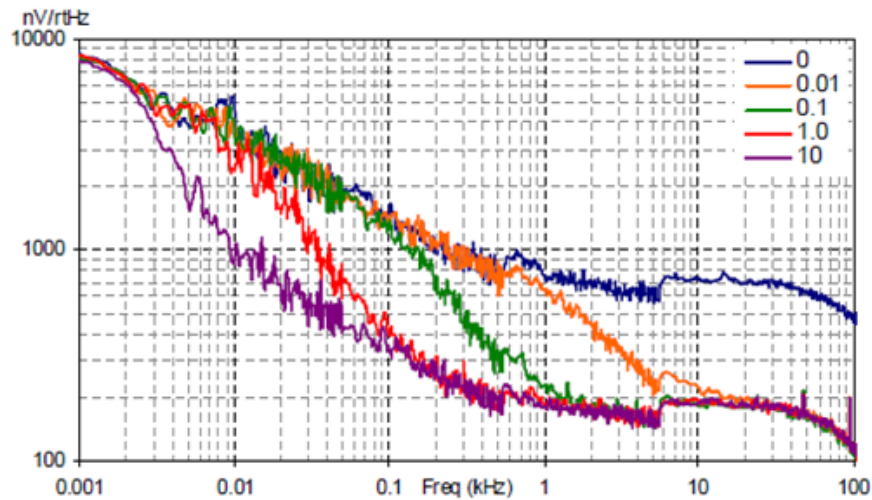
23. $3.0\text{ V} < V_{DD} < 3.6\text{ V}$. See application note [Adjusting PSoC® Trims for 3.3 V and 2.7 V Operation – AN2012](#) for information on trimming for operation at 3.3 V.

24. See the individual user module datasheets for information on maximum frequencies for user modules

Analog Reference Noise spectrum:

When bypassed by a capacitor on P2[4], the noise of the analog ground signal distributed to each block is reduced by a factor of up to 5 (14 dB). This is at frequencies above the corner frequency defined by the on-chip 8.1 K resistance and the external capacitor.

Figure 18. Typical AGND Noise with P2[4] Bypass
AGND = $1.6 \times V_{bg}$



At low frequencies, the opamp noise is proportional to $1/f$, power independent, and determined by device geometry. At high frequencies, increased power level reduces the noise spectrum level.

Note: The capacitor values shown in Figure 18 are in μF .

AC Low-Power Comparator Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$, 3.0 V to 3.6 V and $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$, or 2.4 V to 3.0 V and $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$, respectively. Typical parameters apply to 5 V at 25°C and are for design guidance only.

Table 33. AC Low-Power Comparator Specifications

Symbol	Description	Min	Typ	Max	Unit	Notes
t_{RLPC}	LPC response time	—	—	50	μs	$\geq 50\text{ mV}$ overdrive comparator reference set within V_{REFLPC}

AC Analog Output Buffer Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, or 3.0 V to 3.6 V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, respectively. Typical parameters apply to 5 V and 3.3 V at 25°C and are for design guidance only.

Table 35. 5-V AC Analog Output Buffer Specifications

Symbol	Description	Min	Typ	Max	Unit
t_{ROB}	Rising settling time to 0.1%, 1 V Step, 100 pF load Power = Low Power = High	—	—	4	μs
		—	—	4	μs
t_{SOB}	Falling settling time to 0.1%, 1 V step, 100 pF load Power = Low Power = High	—	—	3.4	μs
		—	—	3.4	μs
SR_{ROB}	Rising slew rate (20% to 80%), 1 V step, 100 pF load Power = Low Power = High	0.5	—	—	V/ μs
		0.5	—	—	V/ μs
SR_{FOB}	Falling slew rate (80% to 20%), 1 V step, 100 pF load Power = Low Power = High	0.55	—	—	V/ μs
		0.55	—	—	V/ μs
BW_{OB}	Small signal bandwidth, 20 mV _{pp} , 3 dB BW, 100 pF load Power = Low Power = High	0.8	—	—	MHz
		0.8	—	—	MHz
BW_{OB}	Large signal bandwidth, 1 V _{pp} , 3 dB BW, 100 pF load Power = Low Power = High	300	—	—	kHz
		300	—	—	kHz

Table 36. 3.3-V AC Analog Output Buffer Specifications

Symbol	Description	Min	Typ	Max	Unit
t_{ROB}	Rising settling time to 0.1%, 1 V Step, 100 pF load Power = Low Power = High	—	—	4.7	μs
		—	—	4.7	μs
t_{SOB}	Falling settling time to 0.1%, 1 V Step, 100 pF load Power = Low Power = High	—	—	4	μs
		—	—	4	μs
SR_{ROB}	Rising slew rate (20% to 80%), 1 V Step, 100 pF load Power = Low Power = High	0.36	—	—	V/ μs
		0.36	—	—	V/ μs
SR_{FOB}	Falling slew rate (80% to 20%), 1 V Step, 100 pF load Power = Low Power = High	0.40	—	—	V/ μs
		0.40	—	—	V/ μs
BW_{OB}	Small signal bandwidth, 20 mV _{pp} , 3 dB BW, 100 pF load Power = Low Power = High	0.7	—	—	MHz
		0.7	—	—	MHz
BW_{OB}	Large signal bandwidth, 1 V _{pp} , 3 dB BW, 100 pF load Power = Low Power = High	200	—	—	kHz
		200	—	—	kHz

AC External Clock Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, or 3.0 V to 3.6 V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, respectively. Typical parameters apply to 5 V and 3.3 V at 25°C and are for design guidance only.

Table 37. 5-V AC External Clock Specifications

Symbol	Description	Min	Typ	Max	Unit
F_{OSCEXT}	Frequency	0.093	—	24.6	MHz
—	High period	20.6	—	5300	ns
—	Low period	20.6	—	—	ns
—	Power-up IMO to switch	150	—	—	μs

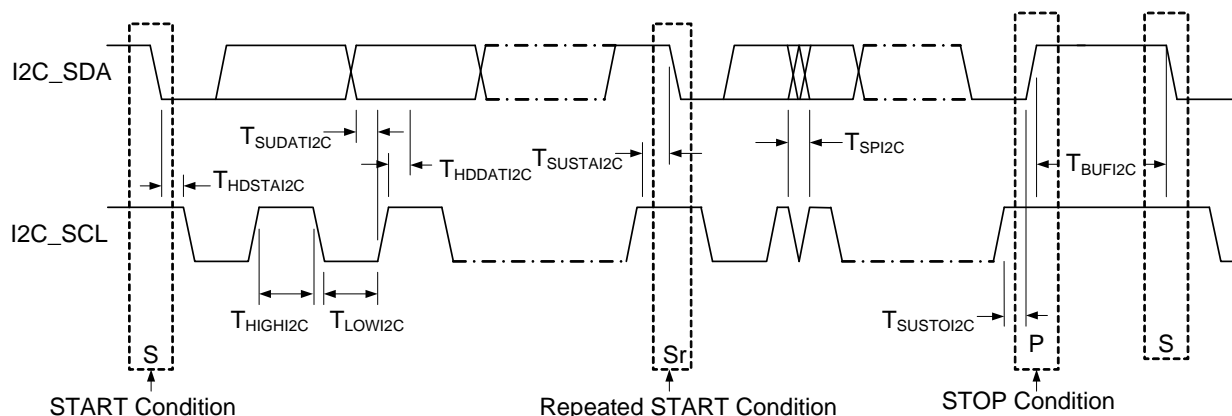
AC I²C Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, or 3.0 V to 3.6 V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, respectively. Typical parameters apply to 5 V and 3.3 V at 25°C and are for design guidance only.

Table 40. AC Characteristics of the I²C SDA and SCL Pins

Symbol	Description	Standard Mode		Fast Mode		Unit
		Min	Max	Min	Max	
F _{SCL I2C}	SCL clock frequency	0	100	0	400	kHz
T _{HDSTAI2C}	Hold time (repeated) START condition. After this period, the first clock pulse is generated.	4.0	–	0.6	–	μs
T _{LOWI2C}	LOW period of the SCL clock	4.7	–	1.3	–	μs
T _{HIGHI2C}	HIGH period of the SCL clock	4.0	–	0.6	–	μs
T _{SUSTAI2C}	Setup time for a repeated START condition	4.7	–	0.6	–	μs
T _{HDDATI2C}	Data hold time	0	–	0	–	μs
T _{SUDATI2C}	Data setup time	250	–	100 ^[29]	–	ns
T _{SUSTOI2C}	Setup time for STOP condition	4.0	–	0.6	–	μs
T _{BUFI2C}	Bus free time between a STOP and START condition	4.7	–	1.3	–	μs
T _{SPI2C}	Pulse width of spikes are suppressed by the input filter.	–	–	0	50	ns

Figure 19. Definition for Timing for Fast/Standard Mode on the I²C Bus



Note

29. A fast-mode I²C-bus device can be used in a standard-mode I²C-bus system, but the requirement $t_{\text{SU;DAT}} \geq 250$ ns must then be met. This is the automatic case if the device does not stretch the LOW period of the SCL signal. If such device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{\text{rmax}} + t_{\text{SU;DAT}} = 1000 + 250 = 1250$ ns (according to the standard-mode I²C-bus specification) before the SCL line is released.

Thermal Impedances

Table 41. Thermal Impedances per Package

Package	Typical θ_{JA} ^[30]
28-pin PDIP	69 °C/W
28-pin SSOP	94 °C/W
28-pin SOIC	67 °C/W
44-pin TQFP	60 °C/W
48-pin SSOP	69 °C/W
48-pin QFN ^[31]	28 °C/W
100-pin TQFP	50 °C/W

Capacitance on Crystal Pins

Table 42. Typical Package Capacitance on Crystal Pins

Package	Package Capacitance
28-pin PDIP	3.5 pF
28-pin SSOP	2.8 pF
28-pin SOIC	2.7 pF
44-pin TQFP	2.6 pF
48-pin SSOP	3.3 pF
48-pin QFN	1.8 pF
100-pin TQFP	3.1 pF

Solder Reflow Specifications

Table 43 shows the solder reflow temperature limits that must not be exceeded.

Table 43. Solder Reflow Specifications

Package	Maximum Peak Temperature (T_C)	Maximum Time above $T_C - 5$ °C
28-pin PDIP	260 °C	30 seconds
28-pin SSOP	260 °C	30 seconds
28-pin SOIC	260 °C	30 seconds
44-pin TQFP	260 °C	30 seconds
48-pin SSOP	260 °C	30 seconds
48-pin QFN	260 °C	30 seconds
100-pin TQFP	260 °C	30 seconds

Notes

30. $T_J = T_A + \text{POWER} \times \theta_{JA}$

31. To achieve the thermal impedance specified for the QFN package, refer to the application note *Design Guidelines for Cypress Quad Flat No Extended Lead (QFN) Packaged Devices – AN72845* available at <http://www.cypress.com>.

Ordering Information

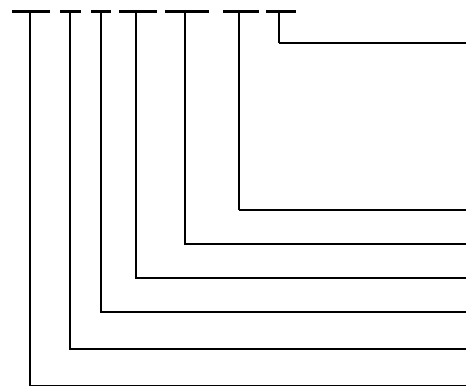
The following table lists the CY8C29x66 PSoC device's key package features and ordering codes.

Package	Ordering Code	Flash (KB)	RAM (KB)	Switch Mode Pump	Temperature Range	Digital PSoC Blocks	Analog PSoC Blocks	Digital I/O Pins	Analog Inputs	Analog Outputs	XRES Pin
28-pin (300-mil) DIP	CY8C29466-24PXI	32	2	Yes	-40 °C to +85 °C	16	12	24	12	4	Yes
28-pin (210-mil) SSOP	CY8C29466-24PVXI	32	2	Yes	-40 °C to +85 °C	16	12	24	12	4	Yes
28-pin (210-mil) SSOP (Tape and Reel)	CY8C29466-24PVXIT	32	2	Yes	-40 °C to +85 °C	16	12	24	12	4	Yes
28-pin (300-mil) SOIC	CY8C29466-24SXI	32	2	Yes	-40 °C to +85 °C	16	12	24	12	4	Yes
28-pin (300-mil) SOIC (Tape and Reel)	CY8C29466-24SXIT	32	2	Yes	-40 °C to +85 °C	16	12	24	12	4	Yes
44-pin TQFP	CY8C29566-24AXI	32	2	Yes	-40 °C to +85 °C	16	12	40	12	4	Yes
44-pin TQFP (Tape and Reel)	CY8C29566-24AXIT	32	2	Yes	-40 °C to +85 °C	16	12	40	12	4	Yes
48-pin (300-mil) SSOP	CY8C29666-24PVXI	32	2	Yes	-40 °C to +85 °C	16	12	44	12	4	Yes
48-pin (300-mil) SSOP (Tape and Reel)	CY8C29666-24PVXIT	32	2	Yes	-40 °C to +85 °C	16	12	44	12	4	Yes
100-Pin TQFP	CY8C29866-24AXI	32	2	Yes	-40 °C to +85 °C	16	12	64	12	4	Yes
100-Pin OCD TQFP ^[35]	CY8C29000-24AXI	32	2	Yes	-40 °C to +85 °C	16	12	64	12	4	Yes
48-Pin (7 x 7 x 1.0 mm) QFN (Sawn)	CY8C29666-24LTXI	32	2	Yes	-40 °C to +85 °C	16	12	44	12	4	Yes
48-Pin (7 x 7 x 1.0 mm) QFN (Sawn)	CY8C29666-24LTXIT	32	2	Yes	-40 °C to +85 °C	16	12	44	12	4	Yes

Note For Die sales information, contact a local Cypress sales office or field applications engineer (FAE).

Ordering Code Definitions

CY 8 C 29 xxx-SPxx



Package Type: Thermal Rating:
 PX = PDIP Pb-free C = Commercial
 SX = SOIC Pb-free I = Industrial
 PVX = SSOP Pb-free E = Extended
 LFX/LKX/LTX/LQX/LCX = QFN Pb-free
 AX = TQFP Pb-free
 Speed: 24 MHz
 Part Number
 Family Code
 Technology Code: C = CMOS
 Marketing Code: 8 = Cypress PSoC
 Company ID: CY = Cypress

Note

35. This part may be used for in-circuit debugging. It is NOT available for production.

Document Conventions

Units of Measure

Table 46 lists the unit of measures.

Table 46. Units of Measure

Symbol	Unit of Measure	Symbol	Unit of Measure
dB	decibels	ms	millisecond
°C	degree Celsius	ns	nanosecond
fF	femto farad	ps	picosecond
pF	picofarad	μV	microvolts
kHz	kilohertz	mV	millivolts
MHz	megahertz	mVpp	millivolts peak-to-peak
rt-Hz	root hertz	nV	nanovolts
kΩ	kilohm	V	volts
Ω	ohm	μW	microwatts
μA	microampere	W	watt
mA	milliampere	mm	millimeter
nA	nanoampere	ppm	parts per million
pA	picoampere	%	percent
μs	microsecond		

Numeric Conventions

Hexadecimal numbers are represented with all letters in uppercase with an appended lowercase 'h' (for example, '14h' or '3Ah'). Hexadecimal numbers may also be represented by a '0x' prefix, the C coding convention. Binary numbers have an appended lowercase 'b' (for example, '01010100b' or '01000011b'). Numbers not indicated by an 'h', 'b', or 0x are decimals.

Glossary

active high	<ol style="list-style-type: none"> 1. A logic signal having its asserted state as the logic 1 state. 2. A logic signal having the logic 1 state as the higher voltage of the two states.
analog blocks	The basic programmable opamp circuits. These are SC (switched capacitor) and CT (continuous time) blocks. These blocks can be interconnected to provide ADCs, DACs, multi-pole filters, gain stages, and much more.
analog-to-digital (ADC)	A device that changes an analog signal to a digital signal of corresponding magnitude. Typically, an ADC converts a voltage to a digital number. The digital-to-analog (DAC) converter performs the reverse operation.
Application programming interface (API)	A series of software routines that comprise an interface between a computer application and lower level services and functions (for example, user modules and libraries). APIs serve as building blocks for programmers that create software applications.
asynchronous	A signal whose data is acknowledged or acted upon immediately, irrespective of any clock signal.
bandgap reference	A stable voltage reference design that matches the positive temperature coefficient of V_T with the negative temperature coefficient of V_{BE} , to produce a zero temperature coefficient (ideally) reference.
bandwidth	<ol style="list-style-type: none"> 1. The frequency range of a message or information processing system measured in hertz. 2. The width of the spectral region over which an amplifier (or absorber) has substantial gain (or loss); it is sometimes represented more specifically as, for example, full width at half maximum.