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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	M8C
Core Size	8-Bit
Speed	24MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	64
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.25V
Data Converters	A/D 12x14b; D/A 4x9b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c29866-24axit

More Information

Cypress provides a wealth of data at www.cypress.com to help you to select the right PSoC device for your design, and to help you to quickly and effectively integrate the device into your design. For a comprehensive list of resources, see the knowledge base article "How to Design with PSoC® 1, PowerPSoC®, and PLC – KBA88292". Following is an abbreviated list for PSoC 1:

- Overview: PSoC Portfolio, PSoC Roadmap
- Product Selectors: PSoC 1, PSoC 3, PSoC 4, PSoC 5LP
- In addition, PSoC Designer includes a device selection tool.
- Application notes: Cypress offers a large number of PSoC application notes covering a broad range of topics, from basic to advanced level. Recommended application notes for getting started with PSoC 1 are:
  - Getting Started with PSoC® 1 – AN75320
  - PSoC® 1 - Getting Started with GPIO – AN2094
  - PSoC® 1 Analog Structure and Configuration – AN74170
  - PSoC® 1 Switched Capacitor Analog Blocks – AN2041
  - Selecting Analog Ground and Reference – AN2219

Note: For CY8C29X66 devices related Application note please click here.

- Development Kits:
  - CY3210-PSoCEval1 supports all PSoC 1 Mixed-Signal Array families, including automotive, except CY8C25/26xxx devices. The kit includes an LCD module, potentiometer, LEDs, and breadboarding space.
  - CY3214-PSoCEvalUSB features a development board for the CY8C24x94 PSoC device. Special features of the board include USB and CapSense development and debugging support.

Note: For CY8C29X66 devices related Development Kits please click here.

The MiniProg1 and MiniProg3 devices provide interfaces for flash programming and debug.

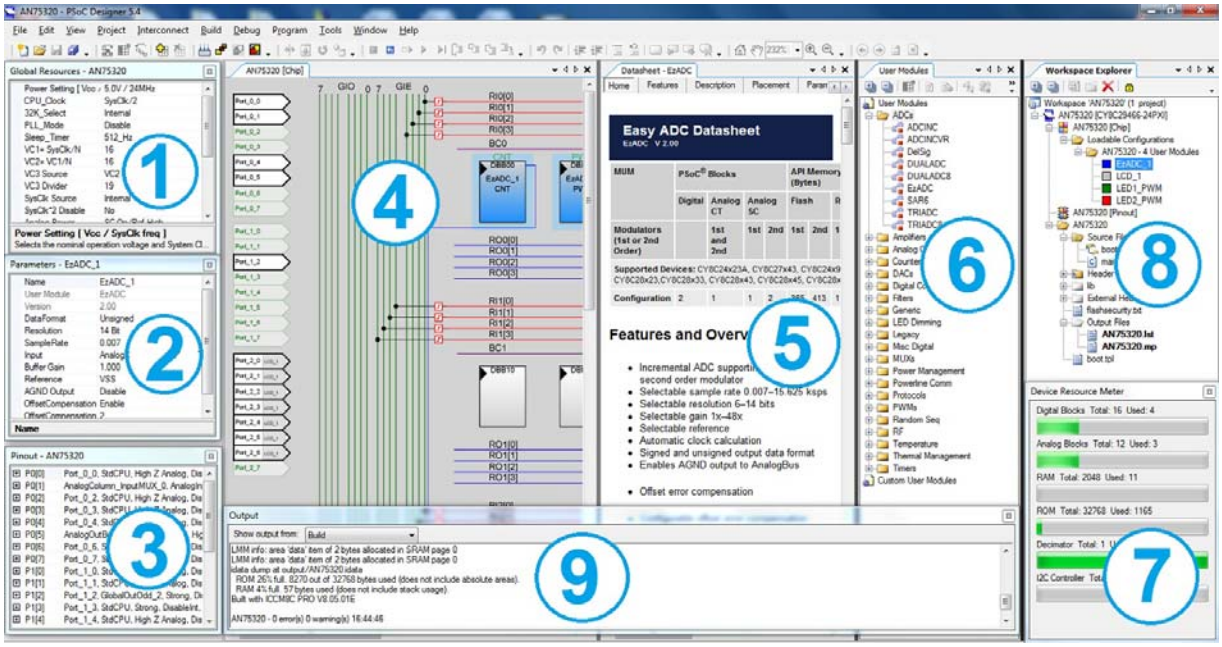
PSoC Designer

PSoC Designer is a free Windows-based Integrated Design Environment (IDE). Develop your applications using a library of pre-characterized analog and digital peripherals in a drag-and-drop design environment. Then, customize your design leveraging the dynamically generated API libraries of code. Figure 1 shows PSoC Designer windows. **Note:** This is not the default view.

1. **Global Resources –** all device hardware settings.
2. **Parameters –** the parameters of the currently selected User Modules.
3. **Pinout –** information related to device pins.
4. **Chip-Level Editor –** a diagram of the resources available on the selected chip.
5. **Datasheet –** the datasheet for the currently selected UM
6. **User Modules –** all available User Modules for the selected device.
7. **Device Resource Meter –** device resource usage for the current project configuration.
8. **Workspace –** a tree level diagram of files associated with the project.
9. **Output –** output from project build and debug operations.

Note: For detailed information on PSoC Designer, go to PSoC® Designer > Help > Documentation > Designer Specific Documents > IDE User Guide.

Figure 1. PSoC Designer Layout



Contents

Digital peripheral configurations include:

- PWMs (8- and 16-bit)
- PWMs with dead band (8- and 16-bit)
- Counters (8- to 32-bit)
- Timers (8- to 32-bit)
- UART 8-bit with selectable parity (up to 2)
- SPI slave and master (up to 2)
- I^2C slave and multi-master (one available as a system resource)
- CRC generator (8- to 32-bit)
- IrDA (up to 2)
- PRS generators (8- to 32-bit)

The digital blocks can be connected to any GPIO through a series of global buses that can route any signal to any pin. The buses also allow for signal multiplexing and for performing logic operations. This configurability frees your designs from the constraints of a fixed peripheral controller.

Digital blocks are provided in rows of four, where the number of blocks varies by PSoC device family. This allows you the optimum choice of system resources for your application. Family resources are shown in the table titled “PSoC Device Characteristics” on page 6.

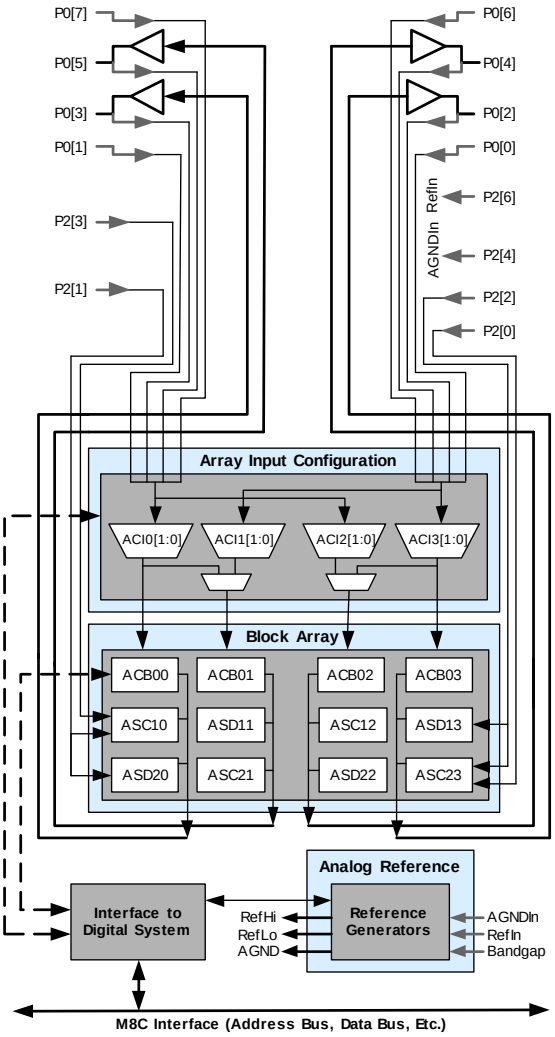
Analog System

The analog system is composed of 12 configurable blocks, each containing an opamp circuit that allows the creation of complex analog signal flows. Analog peripherals are very flexible and can be customized to support specific application requirements. Some of the more common PSoC analog functions (most available as user modules) are:

- ADCs (up to 4, with 6- to 14-bit resolution; selectable as incremental, delta sigma, and SAR)
- Filters (2-, 4-, 6-, and 8-pole band pass, low pass, and notch)
- Amplifiers (up to 4, with selectable gain to 48x)
- Instrumentation amplifiers (up to 2, with selectable gain to 93x)
- Comparators (up to 4, with 16 selectable thresholds)
- DACs (up to 4, with 6-bit to 9-bit resolution)
- Multiplying DACs (up to 4, with 6-bit to 9-bit resolution)
- High current output drivers (four with 30-mA drive as a core resource)
- 1.3-V reference (as a system resource)
- DTMF Dialer
- Modulators
- Correlators
- Peak detectors
- Many other topologies possible

Analog blocks are provided in columns of three, which includes one continuous time (CT) and two switched capacitor (SC) blocks, as shown in Figure 3.

Figure 3. Analog System Block Diagram



Development Tools

PSoC Designer™ is the revolutionary Integrated Design Environment (IDE) that you can use to customize PSoC to meet your specific application requirements. PSoC Designer software accelerates system design and time to market. Develop your applications using a library of precharacterized analog and digital peripherals (called user modules) in a drag-and-drop design environment. Then, customize your design by leveraging the dynamically generated application programming interface (API) libraries of code. Finally, debug and test your designs with the integrated debug environment, including in-circuit emulation and standard software debug features. PSoC Designer includes:

- Application editor graphical user interface (GUI) for device and user module configuration and dynamic reconfiguration
- Extensive user module catalog
- Integrated source-code editor (C and assembly)
- Free C compiler with no size restrictions or time limits
- Built-in debugger
- In-circuit emulation
- Built-in support for communication interfaces:
  - Hardware and software I^2C slaves and masters
  - Full-speed USB 2.0
  - Up to four full-duplex universal asynchronous receiver/transmitters (UARTs), SPI master and slave, and wireless

PSoC Designer supports the entire library of PSoC 1 devices and runs on Windows XP, Windows Vista, and Windows 7.

PSoC Designer Software Subsystems

Design Entry

In the chip-level view, choose a base device to work with. Then select different onboard analog and digital components that use the PSoC blocks, which are called user modules. Examples of user modules are analog-to-digital converters (ADCs), digital-to-analog converters (DACs), amplifiers, and filters. Configure the user modules for your chosen application and connect them to each other and to the proper pins. Then generate your project. This prepopulates your project with APIs and libraries that you can use to program your application.

The tool also supports easy development of multiple configurations and dynamic reconfiguration. Dynamic reconfiguration makes it possible to change configurations at run time. In essence, this allows you to use more than 100 percent of PSoC's resources for an application.

Code Generation Tools

The code generation tools work seamlessly within the PSoC Designer interface and have been tested with a full range of debugging tools. You can develop your design in C, assembly, or a combination of the two.

Assemblers. The assemblers allow you to merge assembly code seamlessly with C code. Link libraries automatically use absolute addressing or are compiled in relative mode, and linked with other software modules to get absolute addressing.

C Language Compilers. C language compilers are available that support the PSoC family of devices. The products allow you to create complete C programs for the PSoC family devices. The optimizing C compilers provide all of the features of C, tailored to the PSoC architecture. They come complete with embedded libraries providing port and bus operations, standard keypad and display support, and extended math functionality.

Debugger

PSoC Designer has a debug environment that provides hardware in-circuit emulation, allowing you to test the program in a physical system while providing an internal view of the PSoC device. Debugger commands allow you to read and program and read and write data memory, and read and write I/O registers. You can read and write CPU registers, set and clear breakpoints, and provide program run, halt, and step control. The debugger also allows you to create a trace buffer of registers and memory locations of interest.

Online Help System

The online help system displays online, context-sensitive help. Designed for procedural and quick reference, each functional subsystem has its own context-sensitive help. This system also provides tutorials and links to FAQs and an Online Support Forum to aid the designer.

In-Circuit Emulator

A low-cost, high-functionality In-Circuit Emulator (ICE) is available for development support. This hardware can program single devices.

The emulator consists of a base unit that connects to the PC using a USB port. The base unit is universal and operates with all PSoC devices. Emulation pods for each device family are available separately. The emulation pod takes the place of the PSoC device in the target board and performs full-speed (24 MHz) operation.

Organize and Connect

You build signal chains at the chip level by interconnecting user modules to each other and the I/O pins. You perform the selection, configuration, and routing so that you have complete control over all on-chip resources.

Generate, Verify, and Debug

When you are ready to test the hardware configuration or move on to developing code for the project, you perform the “Generate Configuration Files” step. This causes PSoC Designer to generate source code that automatically configures the device to your specification and provides the software for the system. The generated code provides application programming interfaces (APIs) with high-level functions to control and respond to hardware events at run time and interrupt service routines that you can adapt as needed.

A complete code development environment allows you to develop and customize your applications in either C, assembly language, or both.

The last step in the development process takes place inside PSoC Designer’s debugger (access by clicking the Connect icon). PSoC Designer downloads the HEX image to the ICE where it runs at full speed. PSoC Designer debugging capabilities rival those of systems costing many times more. In addition to traditional single-step, run-to-breakpoint and watch-variable features, the debug interface provides a large trace buffer and allows you to define complex breakpoint events that include monitoring address and data bus values, memory locations and external signals.

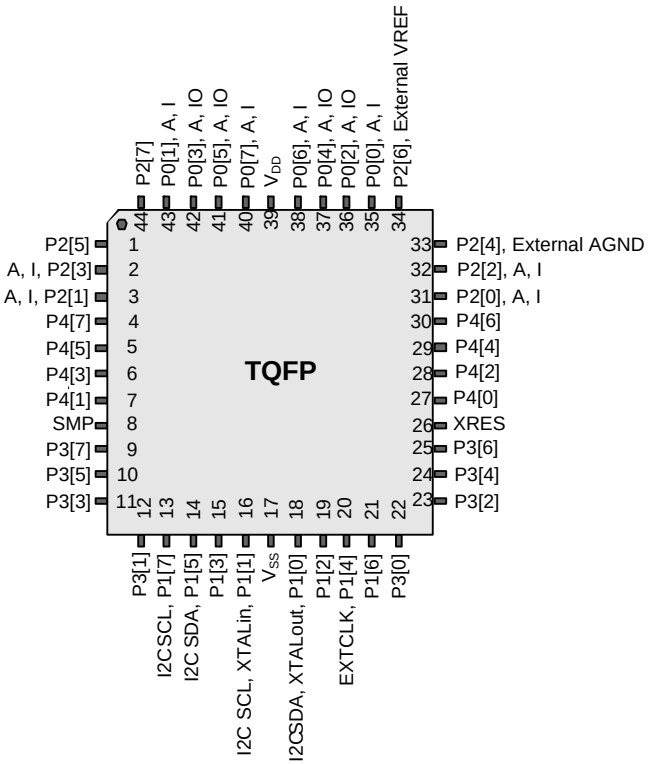
44-Pin Part Pinout

Table 3. 44-Pin Part Pinout (TQFP)

Pin No.	Type		Pin Name	Description
	Digital	Analog		
1	I/O		P2[5]	
2	I/O	I	P2[3]	Direct switched capacitor block input
3	I/O	I	P2[1]	Direct switched capacitor block input
4	I/O		P4[7]	
5	I/O		P4[5]	
6	I/O		P4[3]	
7	I/O		P4[1]	
8	Power		SMP	Switch mode pump (SMP) connection to external components required
9	I/O		P3[7]	
10	I/O		P3[5]	
11	I/O		P3[3]	
12	I/O		P3[1]	
13	I/O		P1[7]	I^2C SCL
14	I/O		P1[5]	I^2C SDA
15	I/O		P1[3]	
16	I/O		P1[1]	Crystal (XTALin), I^2C SCL, ISSP-SCLK[6]
17	Power		V_{SS}	Ground connection
18	I/O		P1[0]	Crystal (XTALout), I^2C SDA, ISSP-SDATA[6]
19	I/O		P1[2]	
20	I/O		P1[4]	Optional EXTCLK
21	I/O		P1[6]	
22	I/O		P3[0]	
23	I/O		P3[2]	
24	I/O		P3[4]	
25	I/O		P3[6]	
26	Input		XRES	Active high external reset with internal pull-down
27	I/O		P4[0]	
28	I/O		P4[2]	
29	I/O		P4[4]	
30	I/O		P4[6]	
31	I/O	I	P2[0]	Direct switched capacitor block input
32	I/O	I	P2[2]	Direct switched capacitor block input
33	I/O		P2[4]	External analog ground (AGND)
34	I/O		P2[6]	External voltage reference (VREF)
35	I/O	I	P0[0]	Analog column mux input
36	I/O	I/O	P0[2]	Analog column mux input and column output
37	I/O	I/O	P0[4]	Analog column mux input and column output
38	I/O	I	P0[6]	Analog column mux input
39	Power		V_{DD}	Supply voltage
40	I/O	I	P0[7]	Analog column mux input
41	I/O	I/O	P0[5]	Analog column mux input and column output
42	I/O	I/O	P0[3]	Analog column mux input and column output
43	I/O	I	P0[1]	Analog column mux input
44	I/O		P2[7]	

LEGEND: A = Analog, I = Input, and O = Output.

Figure 5. CY8C29566 44-Pin PSoC Device



Note
6. These are the ISSP pins, which are not High Z at POR. See the *PSoC Programmable System-on-Chip Technical Reference Manual* for details.

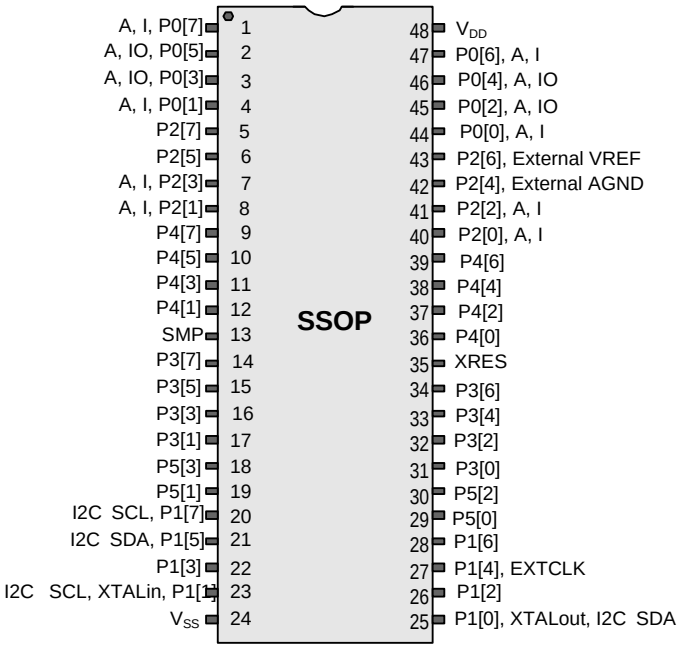
48-Pin Part Pinout

Table 4. 48-Pin Part Pinout (SSOP)

Pin No.	Type		Pin Name	Description
	Digital	Analog		
1	I/O	I	P0[7]	Analog column mux input
2	I/O	I/O	P0[5]	Analog column mux input and column output
3	I/O	I/O	P0[3]	Analog column mux input and column output
4	I/O	I	P0[1]	Analog column mux input
5	I/O		P2[7]	
6	I/O		P2[5]	
7	I/O	I	P2[3]	Direct switched capacitor block input
8	I/O	I	P2[1]	Direct switched capacitor block input
9	I/O		P4[7]	
10	I/O		P4[5]	
11	I/O		P4[3]	
12	I/O		P4[1]	
13	Power		SMP	Switch mode pump (SMP) connection to external components required
14	I/O		P3[7]	
15	I/O		P3[5]	
16	I/O		P3[3]	
17	I/O		P3[1]	
18	I/O		P5[3]	
19	I/O		P5[1]	
20	I/O		P1[7]	I^2C SCL
21	I/O		P1[5]	I^2C SDA
22	I/O		P1[3]	
23	I/O		P1[1]	Crystal (XTALin), I^2C SCL, ISSP-SCLK[7]
24	Power		V_{SS}	Ground connection
25	I/O		P1[0]	Crystal (XTALout), I^2C SDA, ISSP-SDATA[7]
26	I/O		P1[2]	
27	I/O		P1[4]	Optional EXTCLK
28	I/O		P1[6]	
29	I/O		P5[0]	
30	I/O		P5[2]	
31	I/O		P3[0]	
32	I/O		P3[2]	
33	I/O		P3[4]	
34	I/O		P3[6]	
35	Input		XRES	Active high external reset with internal pull-down
36	I/O		P4[0]	
37	I/O		P4[2]	
38	I/O		P4[4]	
39	I/O		P4[6]	
40	I/O	I	P2[0]	Direct switched capacitor block input
41	I/O	I	P2[2]	Direct switched capacitor block input
42	I/O		P2[4]	External Analog Ground (AGND)
43	I/O		P2[6]	External Voltage Reference (VREF)
44	I/O	I	P0[0]	Analog column mux input
45	I/O	I/O	P0[2]	Analog column mux input and column output
46	I/O	I/O	P0[4]	Analog column mux input and column output
47	I/O	I	P0[6]	Analog column mux input
48	Power		V_{DD}	Supply voltage

LEGEND: A = Analog, I = Input, and O = Output.

Figure 6. CY8C29666 48-Pin PSoC Device



Note
7. These are the ISSP pins, which are not High Z at POR. See the *PSoC Programmable System-on-Chip Technical Reference Manual* for details.

100-Pin Part Pinout

Table 6. 100-Pin Part Pinout (TQFP)

Pin No.	Type		Name	Description	Pin No.	Type		Name	Description
	Digital	Analog				Digital	Analog		
1			NC	No connection. Pin must be left floating	51			NC	No connection. Pin must be left floating
2			NC	No connection. Pin must be left floating	52	I/O		P5[0]	
3	I/O	I	P0[1]	Analog column mux input	53	I/O		P5[2]	
4	I/O		P2[7]		54	I/O		P5[4]	
5	I/O		P2[5]		55	I/O		P5[6]	
6	I/O	I	P2[3]	Direct switched capacitor block input	56	I/O		P3[0]	
7	I/O	I	P2[1]	Direct switched capacitor block input	57	I/O		P3[2]	
8	I/O		P4[7]		58	I/O		P3[4]	
9	I/O		P4[5]		59	I/O		P3[6]	
10	I/O		P4[3]		60			NC	No connection. Pin must be left floating
11	I/O		P4[1]		61			NC	No connection. Pin must be left floating
12			NC	No connection. Pin must be left floating	62	Input		XRES	Active high external reset with internal pull-down
13			NC	No connection. Pin must be left floating	63	I/O		P4[0]	
14	Power		SMP	Switch mode pump (SMP) connection to external components required	64	I/O		P4[2]	
15	Power		V_{SS}	Ground connection [10]	65	Power		V_{SS}	Ground connection [10]
16	I/O		P3[7]		66	I/O		P4[4]	
17	I/O		P3[5]		67	I/O		P4[6]	
18	I/O		P3[3]		68	I/O	I	P2[0]	Direct switched capacitor block input
19	I/O		P3[1]		69	I/O	I	P2[2]	Direct switched capacitor block input
20	I/O		P5[7]		70	I/O		P2[4]	External Analog Ground (AGND)
21	I/O		P5[5]		71			NC	No connection. Pin must be left floating
22	I/O		P5[3]		72	I/O		P2[6]	External Voltage Reference (VREF)
23	I/O		P5[1]		73			NC	No connection. Pin must be left floating
24	I/O		P1[7]	I^2C SCL	74	I/O	I	P0[0]	Analog column mux input
25			NC	No connection. Pin must be left floating	75			NC	No connection. Pin must be left floating
26			NC	No connection. Pin must be left floating	76			NC	No connection. Pin must be left floating
27			NC	No connection. Pin must be left floating	77	I/O	I/O	P0[2]	Analog column mux input and column output
28	I/O		P1[5]	I^2C SDA	78			NC	No connection. Pin must be left floating
29	I/O		P1[3]		79	I/O	I/O	P0[4]	Analog column mux input and column output
30	I/O		P1[1]	Crystal (XTALin), I^2C Serial Clock (SCL), ISSP-SCLK[11]	80			NC	No connection. Pin must be left floating
31			NC	No connection. Pin must be left floating	81	I/O	I	P0[6]	Analog column mux input
32	Power		V_{DD}	Supply voltage	82	Power		V_{DD}	Supply voltage
33			NC	No connection. Pin must be left floating	83	Power		V_{DD}	Supply voltage
34	Power		V_{SS}	Ground connection [10]	84	Power		V_{SS}	Ground connection [10]
35			NC	No connection. Pin must be left floating	85	Power		V_{SS}	Ground connection [10]
36	I/O		P7[7]		86	I/O		P6[0]	
37	I/O		P7[6]		87	I/O		P6[1]	
38	I/O		P7[5]		88	I/O		P6[2]	
39	I/O		P7[4]		89	I/O		P6[3]	
40	I/O		P7[3]		90	I/O		P6[4]	
41	I/O		P7[2]		91	I/O		P6[5]	
42	I/O		P7[1]		92	I/O		P6[6]	
43	I/O		P7[0]		93	I/O		P6[7]	
44	I/O		P1[0]	Crystal (XTALout), I^2C Serial Data (SDA), ISSP-SDATA[11]	94			NC	No connection. Pin must be left floating
45	I/O		P1[2]		95	I/O	I	P0[7]	Analog column mux input
46	I/O		P1[4]	Optional EXTCLK	96			NC	No connection. Pin must be left floating
47	I/O		P1[6]		97	I/O	I/O	P0[5]	Analog column mux input and column output
48			NC	No connection. Pin must be left floating	98			NC	No connection. Pin must be left floating
49			NC	No connection. Pin must be left floating	99	I/O	I/O	P0[3]	Analog column mux input and column output
50			NC	No connection. Pin must be left floating	100			NC	No connection. Pin must be left floating

LEGEND: A = Analog, I = Input, and O = Output.

Notes
10. All V_{SS} pins should be brought out to one common GND plane.
11. These are the ISSP pins, which are not High Z at POR. See the *PSoC Programmable System-on-Chip Technical Reference Manual* for details.

Electrical Specifications

This section presents the DC and AC electrical specifications of the CY8C29x66 PSoC device. For the most up-to-date electrical specifications, confirm that you have the most recent datasheet by going to the web at http://www.cypress.com.

Specifications are valid for –40 °C ≤ T_A ≤ 85 °C and T_J ≤ 100 °C, except where noted. Refer to Table 29 for the electrical specifications on the internal main oscillator (IMO) using SLIMO mode.

Figure 10. Voltage versus CPU Frequency

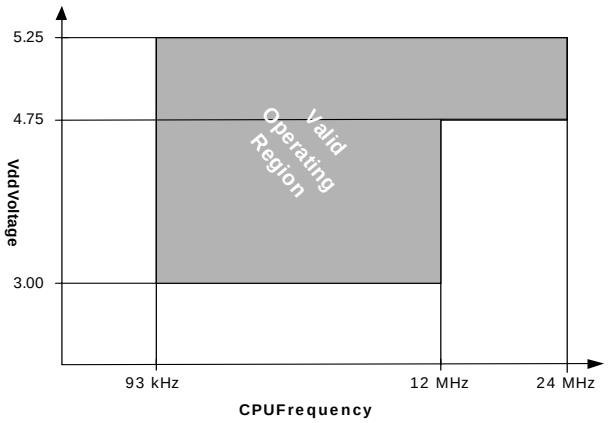
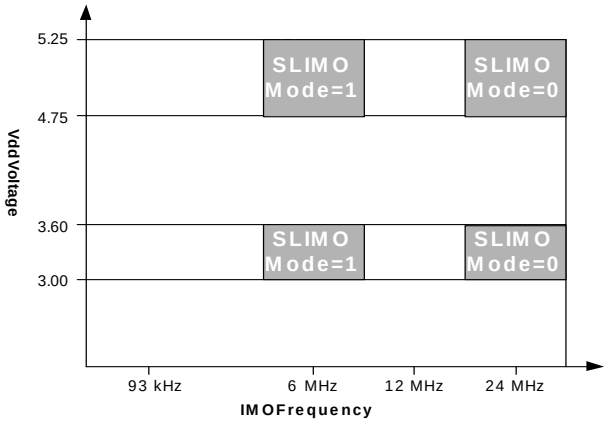


Figure 11. IMO Frequency Options



Absolute Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Table 11. Absolute Maximum Ratings

Symbol	Description	Min	Typ	Max	Unit	Notes
T_{STG}	Storage temperature	–55	25	+100	°C	Higher storage temperatures reduce data retention time. Recommended storage temperature is +25 °C ± 25 °C. Extended duration storage temperatures higher than 65 °C degrade reliability.
$T_{BAKETEMP}$	Bake temperature	–	125	See package label	°C	
$T_{BAKETIME}$	Bake time	See package label	–	72	Hours	
T_A	Ambient temperature with power applied	–40	–	+85	°C	
V_{DD}	Supply voltage on V_{DD} relative to V_{SS}	–0.5	–	+6.0	V	
V_{IO}	DC input voltage	V_{SS} – 0.5	–	V_{DD} + 0.5	V	
V_{IOZ}	DC voltage applied to tristate	V_{SS} – 0.5	–	V_{DD} + 0.5	V	
I_{MIO}	Maximum current into any port pin	–25	–	+50	mA	
I_{MAIO}	Maximum current into any port pin configured as analog driver	–50	–	+50	mA	
ESD	Electrostatic discharge voltage	2000	–	–	V	Human body model ESD.
LU	Latch-up current	–	–	200	mA	

Table 21. 5-V DC Analog Reference Specifications (continued)

Reference ARF_CR[5:3]	Reference Power Settings	Symbol	Reference	Description	Min	Typ	Max	Unit
0b011	RefPower = High Opamp bias = High	V_{REFHI}	Ref High	3 × Bandgap	3.788	3.891	3.986	V
		V_{AGND}	AGND	2 × Bandgap	2.500	2.604	2.699	V
		V_{REFLO}	Ref Low	Bandgap	1.257	1.306	1.359	V
	RefPower = High Opamp bias = Low	V_{REFHI}	Ref High	3 × Bandgap	3.792	3.893	3.982	V
		V_{AGND}	AGND	2 × Bandgap	2.518	2.602	2.692	V
		V_{REFLO}	Ref Low	Bandgap	1.256	1.302	1.354	V
	RefPower = Med Opamp bias = High	V_{REFHI}	Ref High	3 × Bandgap	3.795	3.894	3.993	V
		V_{AGND}	AGND	2 × Bandgap	2.516	2.603	2.698	V
		V_{REFLO}	Ref Low	Bandgap	1.256	1.303	1.353	V
	RefPower = Med Opamp bias = Low	V_{REFHI}	Ref High	3 × Bandgap	3.792	3.895	3.986	V
		V_{AGND}	AGND	2 × Bandgap	2.522	2.602	2.685	V
		V_{REFLO}	Ref Low	Bandgap	1.255	1.301	1.350	V
0b100	RefPower = High Opamp bias = High	V_{REFHI}	Ref High	2 × Bandgap + P2[6] (P2[6] = 1.3 V)	2.495 + P2[6]	2.586 + P2[6]	2.657 + P2[6]	V
		V_{AGND}	AGND	2 × Bandgap	2.502	2.604	2.719	V
		V_{REFLO}	Ref Low	2 × Bandgap – P2[6] (P2[6] = 1.3 V)	2.531 – P2[6]	2.611 – P2[6]	2.681 – P2[6]	V
	RefPower = High Opamp bias = Low	V_{REFHI}	Ref High	2 × Bandgap + P2[6] (P2[6] = 1.3 V)	2.500 + P2[6]	2.591 + P2[6]	2.662 + P2[6]	V
		V_{AGND}	AGND	2 × Bandgap	2.519	2.602	2.693	V
		V_{REFLO}	Ref Low	2 × Bandgap – P2[6] (P2[6] = 1.3 V)	2.530 – P2[6]	2.605 – P2[6]	2.666 – P2[6]	V
	RefPower = Med Opamp bias = High	V_{REFHI}	Ref High	2 × Bandgap + P2[6] (P2[6] = 1.3 V)	2.503 + P2[6]	2.592 + P2[6]	2.662 + P2[6]	V
		V_{AGND}	AGND	2 × Bandgap	2.517	2.603	2.698	V
		V_{REFLO}	Ref Low	2 × Bandgap – P2[6] (P2[6] = 1.3 V)	2.529 – P2[6]	2.606 – P2[6]	2.665 – P2[6]	V
	RefPower = Med Opamp bias = Low	V_{REFHI}	Ref High	2 × Bandgap + P2[6] (P2[6] = 1.3 V)	2.505 + P2[6]	2.594 + P2[6]	2.665 + P2[6]	V
		V_{AGND}	AGND	2 × Bandgap	2.525	2.602	2.685	V
		V_{REFLO}	Ref Low	2 × Bandgap – P2[6] (P2[6] = 1.3 V)	2.528 – P2[6]	2.603 – P2[6]	2.661 – P2[6]	V

DC Analog External Reference Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 23. 5-V DC Analog External Reference Specifications

Reference	Description	Min	Typ	Max	Unit
Ref Low	Ref Low = P2[4] – P2[6] (P2[4] = V_{CC}/2, P2[6] = 1.3 V)	1.12	1.221	1.28	V
AGND	AGND = P2[4] (P2[4] = V_{CC}/2)	2.487	2.499	2.513	V
Ref High	Ref Low = P2[4] + P2[6] (P2[4] = V_{CC}/2, P2[6] = 1.3 V)	3.67	3.759	3.93	V

Table 24. 3.3-V DC Analog External Reference Specifications

Reference	Description	Min	Typ	Max	Unit
Ref Low	Ref Low = P2[4] – P2[6] (P2[4] = V_{CC}/2, P2[6] = 1.3 V)	0.29	0.371	0.41	V
AGND	AGND = P2[4] (P2[4] = V_{CC}/2)	1.642	1.649	1.658	V
Ref High	Ref Low = P2[4] + P2[6] (P2[4] = V_{CC}/2, P2[6] = 1.3 V)	–	2.916	–	V

DC Analog PSoC Block Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 25. DC Analog PSoC Block Specifications

Symbol	Description	Min	Typ	Max	Unit	Notes
R_{CT}	Resistor unit value (continuous time)	–	12.2	–	kΩ	
C_{SC}	Capacitor unit value (switch cap)	–	80	–	fF	

Table 29. AC Chip-Level Specifications (continued)

Symbol	Description	Min	Typ	Max	Units	Notes
SR_{POWER_UP}	Power supply slew rate	–	–	250	V/ms	V_{DD} slew rate during power-up
$T_{POWERUP}$ [25]	Time from end of POR to CPU executing code	–	16	100	ms	Power-up from 0 V. See the System Resets section of the PSoC Technical Reference Manual
tjit_IMO[26]	24 MHz IMO cycle-to-cycle jitter (RMS)	–	200	700	ps	N = 32
	24 MHz IMO long term N cycle-to-cycle jitter (RMS)	–	300	900		
	24 MHz IMO period jitter (RMS)	–	100	400		
tjit_PLL [26]	24 MHz IMO cycle-to-cycle jitter (RMS)	–	200	800	ps	N = 32
	24 MHz IMO long term N cycle-to-cycle jitter (RMS)	–	300	1200		
	24 MHz IMO period jitter (RMS)	–	100	700		

Figure 13. PLL Lock Timing Diagram

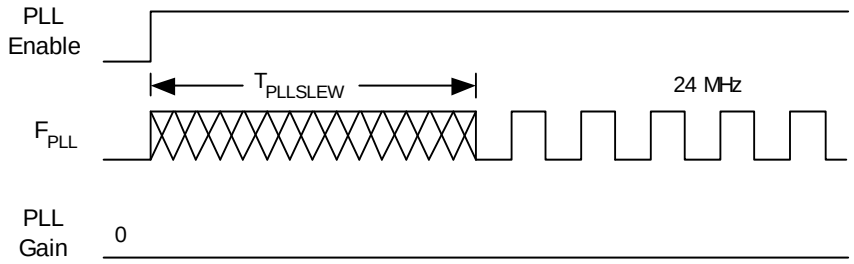


Figure 14. PLL Lock for Low Gain Setting Timing Diagram

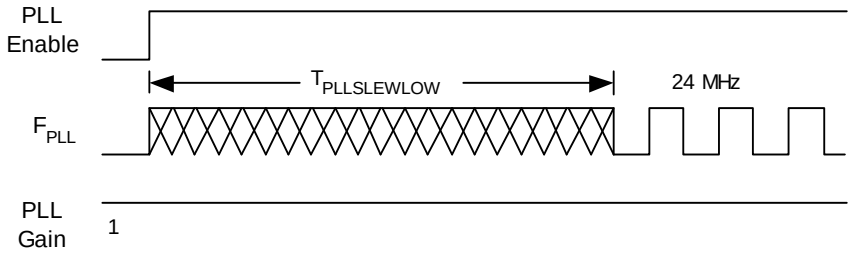
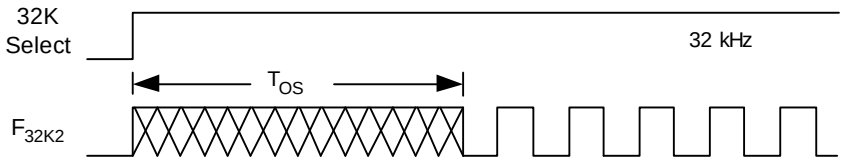


Figure 15. External Crystal Oscillator Startup Timing Diagram



Notes
25. Errata: When V_{DD} of the device is pulled below ground just before power-on; the first read from each 8K Flash bank may be corrupted apart from Flash bank 0. This can be solved by doing a dummy read from each Flash bank prior to use of the Flash banks. For more information, see Errata on page 63.
26. Refer to Cypress Jitter Specifications application note, Understanding Datasheet Jitter Specifications for Cypress Timing Products – AN5054 for more information.

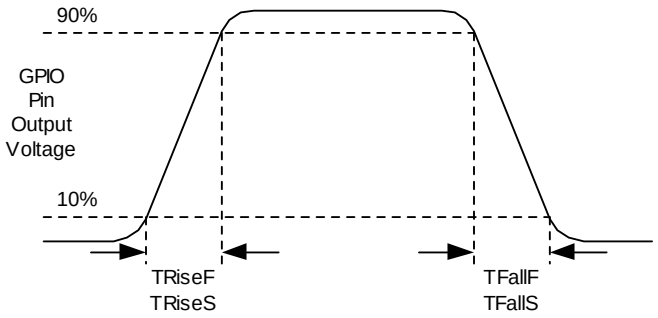
AC General Purpose I/O Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 30. AC GPIO Specifications

Symbol	Description	Min	Typ	Max	Unit	Notes
F_{GPIO}	GPIO operating frequency	0	–	12.3	MHz	Normal strong mode
tRiseF	Rise time, normal strong mode, Cload = 50 pF	3	–	18	ns	V_{DD} = 4.75 to 5.25 V, 10% to 90%
tFallF	Fall time, normal strong mode, Cload = 50 pF	2	–	18	ns	V_{DD} = 4.75 to 5.25 V, 10% to 90%
tRiseS	Rise time, slow strong mode, Cload = 50 pF	10	27	–	ns	V_{DD} = 3 to 5.25 V, 10% to 90%
tFallS	Fall time, slow strong mode, Cload = 50 pF	10	22	–	ns	V_{DD} = 3 to 5.25 V, 10% to 90%

Figure 16. GPIO Timing Diagram



AC Operational Amplifier Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Settling times, slew rates, and gain bandwidth are based on the analog continuous time PSoC block.

Power = High and Opamp bias = High is not supported at 3.3 V.

Table 31. 5-V AC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Unit
t_{ROA}	Rising settling time to 0.1% for a 1 V step (10 pF load, unity gain) Power = Low, Opamp bias = Low Power = Medium, Opamp bias = High Power = High, Opamp bias = High	 – – –	 – – –	 3.9 0.72 0.62	 µs µs µs
t_{SOA}	Falling settling time to 0.1% for a 1 V step (10 pF load, unity gain) Power = Low, Opamp bias = Low Power = Medium, Opamp bias = High Power = High, Opamp bias = High	 – – –	 – – –	 5.9 0.92 0.72	 µs µs µs
SR_{ROA}	Rising slew rate (20% to 80%) of a 1 V step (10 pF load, unity gain) Power = Low, Opamp bias = Low Power = Medium, Opamp bias = High Power = High, Opamp bias = High	 0.15 1.7 6.5	 – – –	 – – –	 V/µs V/µs V/µs
SR_{FOA}	Falling slew rate (20% to 80%) of a 1 V step (10 pF load, unity gain) Power = Low, Opamp bias = Low Power = Medium, Opamp bias = High Power = High, Opamp bias = High	 0.01 0.5 4.0	 – – –	 – – –	 V/µs V/µs V/µs
BW_{OA}	Gain bandwidth product Power = Low, Opamp bias = Low Power = Medium, Opamp bias = High Power = High, Opamp bias = High	 0.75 3.1 5.4	 – – –	 – – –	 MHz MHz MHz
E_{NOA}	Noise at 1 kHz (Power = Medium, Opamp bias = High)	–	100	–	nV/rt-Hz

AC Digital Block Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 34. AC Digital Block Specifications

Function	Description	Min	Typ	Max	Unit	Notes
All functions	Block input clock frequency					
	V_{DD} ≥ 4.75 V	–	–	50.4	MHz	
	V_{DD} < 4.75 V	–	–	25.2	MHz	
Timer	Input clock frequency					
	No capture, V_{DD} ≥ 4.75 V	–	–	50.4	MHz	
	No capture, V_{DD} < 4.75 V	–	–	25.2	MHz	
	With capture	–	–	25.2	MHz	
	Capture pulse width	50[27]	–	–	ns	
Counter	Input clock frequency					
	No enable input, V_{DD} ≥ 4.75 V	–	–	50.4	MHz	
	No enable input, V_{DD} < 4.75 V	–	–	25.2	MHz	
	With enable input	–	–	25.2	MHz	
	Enable input pulse width	50[27]	–	–	ns	
Dead Band	Kill pulse width					
	Asynchronous restart mode	20	–	–	ns	
	Synchronous restart mode	50[27]	–	–	ns	
	Disable mode	50[27]	–	–	ns	
	Input clock frequency					
	V_{DD} ≥ 4.75 V	–	–	50.4	MHz	
	V_{DD} < 4.75 V	–	–	25.2	MHz	
CRCPRS (PRS Mode)	Input clock frequency					
	V_{DD} ≥ 4.75 V	–	–	50.4	MHz	
	V_{DD} < 4.75 V	–	–	25.2	MHz	
CRCPRS (CRC Mode)	Input clock frequency	–	–	25.2	MHz	
SPIM	Input clock frequency	–	–	8.2	MHz	The SPI serial clock (SCLK) frequency is equal to the input clock frequency divided by 2
SPIS	Input clock (SCLK) frequency	–	–	4.1	MHz	The input clock is the SPI SCLK in SPIS mode
	Width of SS_negated between transmissions	50[27]	–	–	ns	
Transmitter	Input clock frequency					The baud rate is equal to the input clock frequency divided by 8
	V_{DD} ≥ 4.75 V, 2 stop bits	–	–	50.4	MHz	
	V_{DD} ≥ 4.75 V, 1 stop bit	–	–	25.2	MHz	
	V_{DD} < 4.75 V	–	–	25.2	MHz	
Receiver	Input clock frequency					The baud rate is equal to the input clock frequency divided by 8
	V_{DD} ≥ 4.75 V, 2 stop bits	–	–	50.4	MHz	
	V_{DD} ≥ 4.75 V, 1 stop bit	–	–	25.2	MHz	
	V_{DD} < 4.75 V	–	–	25.2	MHz	

Note
27. 50 ns minimum input pulse width is based on the input synchronizers running at 24 MHz (42 ns nominal period).

AC Analog Output Buffer Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 35. 5-V AC Analog Output Buffer Specifications

Symbol	Description	Min	Typ	Max	Unit
t_{ROB}	Rising settling time to 0.1%, 1 V Step, 100 pF load Power = Low Power = High	 – –	 – –	 4 4	 µs µs
t_{SOB}	Falling settling time to 0.1%, 1 V step, 100 pF load Power = Low Power = High	 – –	 – –	 3.4 3.4	 µs µs
SR_{ROB}	Rising slew rate (20% to 80%), 1 V step, 100 pF load Power = Low Power = High	 0.5 0.5	 – –	 – –	 V/µs V/µs
SR_{FOB}	Falling slew rate (80% to 20%), 1 V step, 100 pF load Power = Low Power = High	 0.55 0.55	 – –	 – –	 V/µs V/µs
BW_{OB}	Small signal bandwidth, 20 mV_{pp}, 3 dB BW, 100 pF load Power = Low Power = High	 0.8 0.8	 – –	 – –	 MHz MHz
BW_{OB}	Large signal bandwidth, 1 V_{pp}, 3 dB BW, 100 pF load Power = Low Power = High	 300 300	 – –	 – –	 kHz kHz

Table 36. 3.3-V AC Analog Output Buffer Specifications

Symbol	Description	Min	Typ	Max	Unit
t_{ROB}	Rising settling time to 0.1%, 1 V Step, 100 pF load Power = Low Power = High	 – –	 – –	 4.7 4.7	 µs µs
t_{SOB}	Falling settling time to 0.1%, 1 V Step, 100 pF load Power = Low Power = High	 – –	 – –	 4 4	 µs µs
SR_{ROB}	Rising slew rate (20% to 80%), 1 V Step, 100 pF load Power = Low Power = High	 0.36 0.36	 – –	 – –	 V/µs V/µs
SR_{FOB}	Falling slew rate (80% to 20%), 1 V Step, 100 pF load Power = Low Power = High	 0.40 0.40	 – –	 – –	 V/µs V/µs
BW_{OB}	Small signal bandwidth, 20 mV_{pp}, 3 dB BW, 100 pF load Power = Low Power = High	 0.7 0.7	 – –	 – –	 MHz MHz
BW_{OB}	Large signal bandwidth, 1 V_{pp}, 3 dB BW, 100 pF load Power = Low Power = High	 200 200	 – –	 – –	 kHz kHz

AC External Clock Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 37. 5-V AC External Clock Specifications

Symbol	Description	Min	Typ	Max	Unit
F_{OSCEXT}	Frequency	0.093	–	24.6	MHz
–	High period	20.6	–	5300	ns
–	Low period	20.6	–	–	ns
–	Power-up IMO to switch	150	–	–	µs

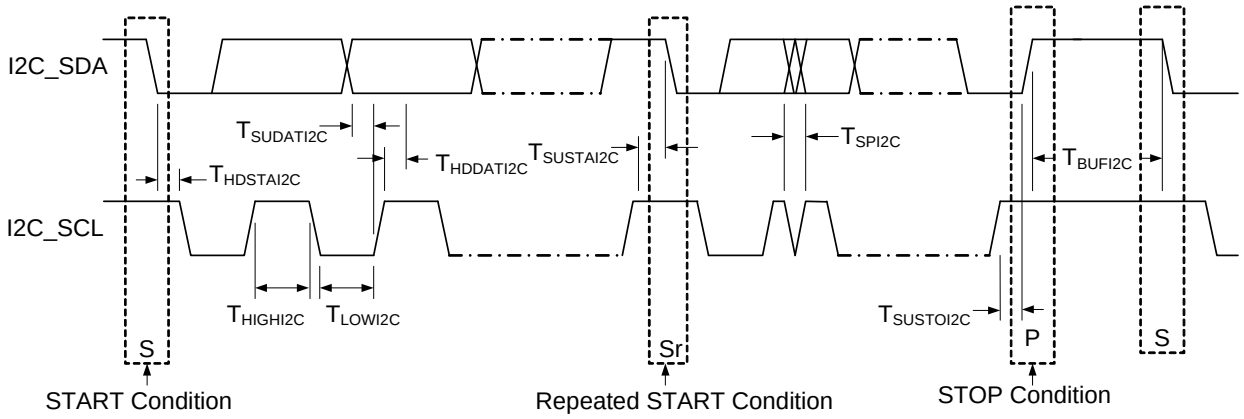
AC I²C Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 40. AC Characteristics of the I²C SDA and SCL Pins

Symbol	Description	Standard Mode		Fast Mode		Unit
		Min	Max	Min	Max	
F_{SCLI2C}	SCL clock frequency	0	100	0	400	kHz
$T_{HDSTAI2C}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated.	4.0	–	0.6	–	µs
T_{LOWI2C}	LOW period of the SCL clock	4.7	–	1.3	–	µs
$T_{HIGHI2C}$	HIGH period of the SCL clock	4.0	–	0.6	–	µs
$T_{SUSTAI2C}$	Setup time for a repeated START condition	4.7	–	0.6	–	µs
$T_{HDDATI2C}$	Data hold time	0	–	0	–	µs
$T_{SUDATI2C}$	Data setup time	250	–	100[29]	–	ns
$T_{SUSTOI2C}$	Setup time for STOP condition	4.0	–	0.6	–	µs
T_{BUFI2C}	Bus free time between a STOP and START condition	4.7	–	1.3	–	µs
T_{SPI2C}	Pulse width of spikes are suppressed by the input filter.	–	–	0	50	ns

Figure 19. Definition for Timing for Fast/Standard Mode on the I²C Bus



Note

29. A fast-mode I²C-bus device can be used in a standard-mode I²C-bus system, but the requirement $t_{SU;DAT}$ >= 250 ns must then be met. This is the automatic case if the device does not stretch the LOW period of the SCL signal. If such device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line t_{rmax} + $t_{SU;DAT}$ = 1000 + 250 = 1250 ns (according to the standard-mode I²C-bus specification) before the SCL line is released.

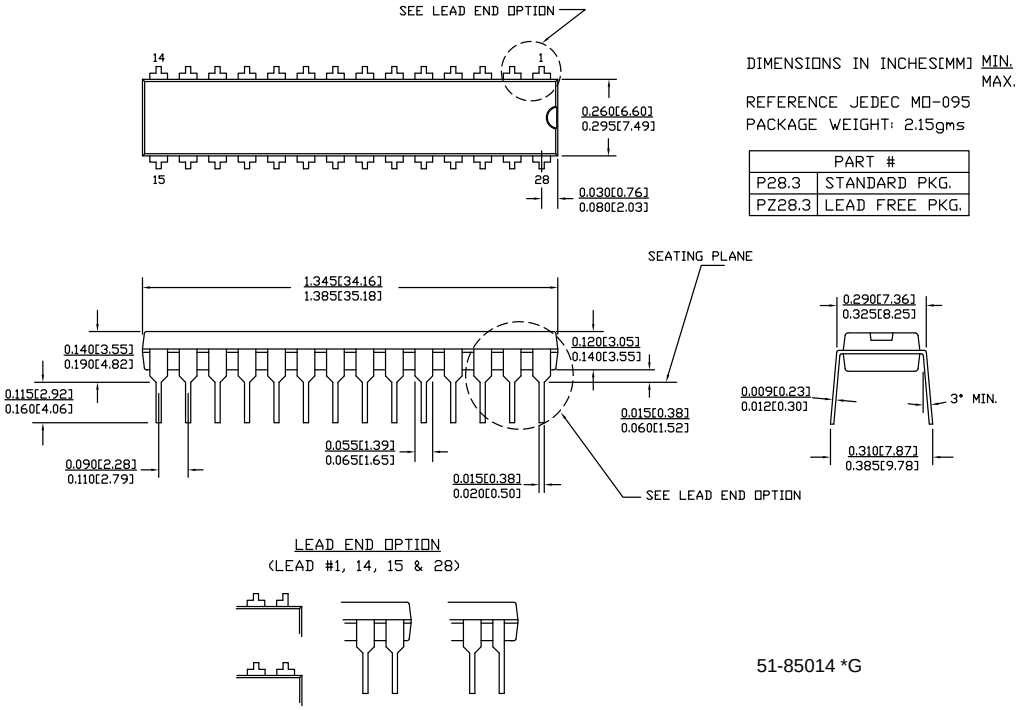
Packaging Information

This section illustrates the packaging specifications for the CY8C29x66 PSoC device, along with the thermal impedances for each package and the typical package capacitance on crystal pins.

Important Note Emulation tools may require a larger area on the target PCB than the chip's footprint. For a detailed description of the emulation tools' dimensions, refer to the emulator pod drawings at http://www.cypress.com.

Packaging Dimensions

Figure 20. 28-pin PDIP (300 Mils) Package Outline, 51-85014



Device Programmers

All device programmers can be purchased from the Cypress Online Store.

CY3216 Modular Programmer

The CY3216 Modular Programmer kit features a modular programmer and the MiniProg1 programming unit. The modular programmer includes three programming module cards and supports multiple Cypress products. The kit includes:

- Modular programmer base
- Three programming module cards
- MiniProg programming unit
- PSoC Designer software CD
- Getting Started guide
- USB 2.0 cable

CY3207ISSP In-System Serial Programmer (ISSP)

The CY3207ISSP is a production programmer. It includes protection circuitry and an industrial case that is more robust than the MiniProg in a production-programming environment.

Note CY3207ISSP needs special software and is not compatible with PSoC Programmer. The kit includes:

- CY3207 programmer unit
- PSoC ISSP software CD
- 110 ~ 240 V power supply, Euro-Plug adapter
- USB 2.0 cable

Accessories (Emulation and Programming)

Table 44. Emulation and Programming Accessories

Part #	Pin Package	Flex-Pod Kit[32]	Foot Kit[33]	Adapter[34]
CY8C29466-24PXI	28-pin PDIP	CY3250-29XXX	CY3250-28PDIP-FK	Adapters can be found at http://www.emulation.com.
CY8C29466-24PVXI	28-pin SSOP	CY3250-29XXX	CY3250-28SSOP-FK	
CY8C29466-24SXI	28-pin SOIC	CY3250-29XXX	CY3250-28SOIC-FK	
CY8C29566-24AXI	44-pin TQFP	CY3250-29XXX	CY3250-44TQFP-FK	
CY8C29666-24PVXI	48-pin SSOP	CY3250-29XXX	CY3250-48SSOP-FK	
CY8C29666-24LTXI	48-pin QFN	CY3250-29XXXQFN	CY3250-48QFN-FK	
CY8C29866-24AXI	100-pin TQFP	CY3250-29XXX	CY3250-100TQFP-FK	

Notes
32. Flex-Pod kit includes a practice flex-pod and a practice PCB, in addition to two flex-pods.
33. Foot kit includes surface mount feet that can be soldered to the target PCB.
34. Programming adapter converts non-DIP package to DIP footprint. Specific details and ordering information for each of the adapters can be found at http://www.emulation.com

Glossary (continued)

duty cycle	The relationship of a clock period high time to its low time, expressed as a percent.
emulator	Duplicates (provides an emulation of) the functions of one system with a different system, so that the second system appears to behave like the first system.
External Reset (XRES)	An active high signal that is driven into the PSoC device. It causes all operation of the CPU and blocks to stop and return to a pre-defined state.
Flash	An electrically programmable and erasable, non-volatile technology that provides you the programmability and data storage of EPROMs, plus in-system erasability. Non-volatile means that the data is retained when power is OFF.
Flash block	The smallest amount of Flash ROM space that may be programmed at one time and the smallest amount of Flash space that may be protected. A Flash block holds 64 bytes.
frequency	The number of cycles or events per unit of time, for a periodic function.
gain	The ratio of output current, voltage, or power to input current, voltage, or power, respectively. Gain is usually expressed in dB.
I^2C	A two-wire serial computer bus by Philips Semiconductors (now NXP Semiconductors). I2C is an Inter-Integrated Circuit. It is used to connect low-speed peripherals in an embedded system. The original system was created in the early 1980s as a battery control interface, but it was later used as a simple internal bus system for building control electronics. I2C uses only two bi-directional pins, clock and data, both running at +5 V and pulled high with resistors. The bus operates at 100 kbits/second in standard mode and 400 kbits/second in fast mode.
ICE	The in-circuit emulator that allows you to test the project in a hardware environment, while viewing the debugging device activity in a software environment (PSoC Designer).
input/output (I/O)	A device that introduces data into or extracts data from a system.
interrupt	A suspension of a process, such as the execution of a computer program, caused by an event external to that process, and performed in such a way that the process can be resumed.
interrupt service routine (ISR)	A block of code that normal code execution is diverted to when the M8C receives a hardware interrupt. Many interrupt sources may each exist with its own priority and individual ISR code block. Each ISR code block ends with the RETI instruction, returning the device to the point in the program where it left normal program execution.
jitter	1. A misplacement of the timing of a transition from its ideal position. A typical form of corruption that occurs on serial data streams. 2. The abrupt and unwanted variations of one or more signal characteristics, such as the interval between successive pulses, the amplitude of successive cycles, or the frequency or phase of successive cycles.
low-voltage detect (LVD)	A circuit that senses V_{DD} and provides an interrupt to the system when V_{DD} falls lower than a selected threshold.
M8C	An 8-bit Harvard-architecture microprocessor. The microprocessor coordinates all activity inside a PSoC by interfacing to the Flash, SRAM, and register space.
master device	A device that controls the timing for data exchanges between two devices. Or when devices are cascaded in width, the master device is the one that controls the timing for data exchanges between the cascaded devices and an external interface. The controlled device is called the ***slave device.***

Document History Page (continued)

Document Title: CY8C29466/CY8C29566/CY8C29666/CY8C29866, PSoC® Programmable System-on-Chip™ Document Number: 38-12013				
Revision	**ECN**	**Origin of Change**	**Submission Date**	**Description of Change**
*V	3991993	PMAD	05/08/2013	Updated Packaging Information: spec 51-85014 – Changed revision from *F to *G. spec 51-85061 – Changed revision from *E to *F. spec 001-13191 – Changed revision from *F to *G. Updated Reference Documents (Removed 001-17397 spec, 001-14503 spec related information). Added Errata.
*W	4081641	PMAD	07/31/2013	Added Errata footnotes (Note 1, 2, 14, 21, 25). Updated Features: Replaced "±2.5%" with "±5%". Added Note 1 and referred the same note in ±5% under "Precision, programmable clocking". Updated PSoC Functional Overview: Updated PSoC Core: Replaced "2.5%" with "5%" in 4th paragraph. Added Note 2 and referred the same note in 5%. Updated Electrical Specifications: Updated DC Electrical Characteristics: Updated DC Chip-Level Specifications: Added Note 14 and referred the same note in V_{DD} parameter. Updated AC Electrical Characteristics: Updated AC Chip-Level Specifications: Added Note 21 and referred the same note in F_{IMO24} parameter in Table 29. Replaced all instances of "24.6" with "25.2" in Table 29. Replaced all instances of "23.4" with "22.8" in Table 29. Replaced all instances of "49.2" with "50.4" in Table 29. Replaced "12.3" with "12.6" for maximum value of F_{CPU2} parameter in Table 29. Replaced "46.8" with "45.6" for minimum value of Fout48M parameter in Table 29. Added Note 25 and referred the same note in $T_{POWERUP}$ parameter in Table 29. Updated AC Digital Block Specifications: Replaced all instances of "49.2" with "50.4" in Table 34. Replaced all instances of "24.6" with "25.2" in Table 34. Updated Packaging Information: spec 51-85026 – Changed revision from *F to *G. spec 51-85048 – Changed revision from *G to *H. Updated Errata. Updated in new template.
*X	4378144	PMAD	05/13/2014	Updated Electrical Specifications: Updated AC Electrical Characteristics: Updated AC External Clock Specifications: Updated Table 37: Changed unit from "ms" to "µs" corresponding to "Power-up IMO to switch". Updated Packaging Information: spec 51-85026 – Changed revision from *G to *H. spec 51-85064 – Changed revision from *E to *F. spec 51-85048 – Changed revision from *H to *I. Completing Sunset Review.