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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

#### Details

Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	40 MIPs
Connectivity	I <sup>2</sup> C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, Motor Control PWM, QEI, POR, PWM, WDT
Number of I/O	15
Program Memory Size	12KB (12K x 8)
Program Memory Type	FLASH
EEPROM Size	·
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 4x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SOIC (0.295", 7.50mm Width)
Supplier Device Package	20-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33fj12mc201-e-so

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

# dsPIC33FJ12MC201/202

The dsPIC33FJ12MC201/202 supports 16/16 and 32/ 16 divide operations, both fractional and integer. All divide instructions are iterative operations. They must be executed within a REPEAT loop, resulting in a total execution time of 19 instruction cycles. The divide operation can be interrupted during any of those 19 cycles without loss of data. A 40-bit barrel shifter is used to perform up to a 16-bit left or right shift in a single cycle. The barrel shifter can be used by both MCU and DSP instructions.



### FIGURE 3-1: dsPIC33FJ12MC201/202 CPU CORE BLOCK DIAGRAM

### 3.5 Arithmetic Logic Unit (ALU)

The dsPIC33FJ12MC201/202 ALU is 16 bits wide and is capable of addition, subtraction, bit shifts, and logic operations. Unless otherwise mentioned, arithmetic operations are 2's complement in nature. Depending on the operation, the ALU can affect the values of the Carry (C), Zero (Z), Negative (N), Overflow (OV), and Digit Carry (DC) Status bits in the SR register. The C and DC Status bits operate as Borrow and Digit Borrow bits, respectively, for subtraction operations.

The ALU can perform 8-bit or 16-bit operations, depending on the mode of the instruction that is used. Data for the ALU operation can come from the W register array or data memory, depending on the addressing mode of the instruction. Likewise, output data from the ALU can be written to the W register array or a data memory location.

Refer to the *"16-bit MCU and DSC Programmer's Reference Manual"* (DS70157) for information on the SR bits affected by each instruction.

The dsPIC33FJ12MC201/202 CPU incorporates hardware support for both multiplication and division. This includes a dedicated hardware multiplier and support hardware for 16-bit-divisor division.

### 3.5.1 MULTIPLIER

Using the high-speed 17-bit x 17-bit multiplier of the DSP engine, the ALU supports unsigned, signed or mixed-sign operation in several MCU multiplication modes:

- 16-bit x 16-bit signed
- 16-bit x 16-bit unsigned
- 16-bit signed x 5-bit (literal) unsigned
- 16-bit unsigned x 16-bit unsigned
- 16-bit unsigned x 5-bit (literal) unsigned
- 16-bit unsigned x 16-bit signed
- · 8-bit unsigned x 8-bit unsigned

### 3.5.2 DIVIDER

The divide block supports 32-bit/16-bit and 16-bit/16-bit signed and unsigned integer divide operations with the following data sizes:

- 1. 32-bit signed/16-bit signed divide
- 2. 32-bit unsigned/16-bit unsigned divide
- 3. 16-bit signed/16-bit signed divide
- 4. 16-bit unsigned/16-bit unsigned divide

The quotient for all divide instructions ends up in W0 and the remainder in W1. 16-bit signed and unsigned DIV instructions can specify any W register for both the 16-bit divisor (Wn) and any W register (aligned) pair (W(m + 1):Wm) for the 32-bit dividend. The divide algorithm takes one cycle per bit of divisor, so both 32-bit/16-bit and 16-bit/16-bit instructions take the same number of cycles to execute.

### 3.6 DSP Engine

The DSP engine consists of a high-speed 17-bit x 17-bit multiplier, a barrel shifter and a 40-bit adder/ subtracter (with two target accumulators, round and saturation logic).

The dsPIC33FJ12MC201/202 is a single-cycle instruction flow architecture; therefore, concurrent operation of the DSP engine with MCU instruction flow is not possible. However, some MCU ALU and DSP engine resources can be used concurrently by the same instruction (e.g., ED, EDAC).

The DSP engine can also perform inherent accumulator-to-accumulator operations that require no additional data. These instructions are ADD, SUB, and NEG.

The DSP engine has options selected through bits in the CPU Core Control register (CORCON), as listed below:

- Fractional or integer DSP multiply (IF)
- Signed or unsigned DSP multiply (US)
- Conventional or convergent rounding (RND)
- Automatic saturation on/off for ACCA (SATA)
- Automatic saturation on/off for ACCB (SATB)
- Automatic saturation on/off for writes to data memory (SATDW)
- Accumulator Saturation mode selection (ACC-SAT)

A block diagram of the DSP engine is shown in Figure 3-3.

### TABLE 3-1: DSP INSTRUCTIONS SUMMARY

Instruction	Algebraic Operation	ACC Write Back
CLR	A = 0	Yes
ED	$A = (x - y)^2$	No
EDAC	$A = A + (x - y)^2$	No
MAC	A = A + (x * y)	Yes
MAC	$A = A + x^2$	No
MOVSAC	No change in A	Yes
MPY	A = x * y	No
MPY	$A = x^2$	No
MPY.N	A = -x * y	No
MSC	A = A - x * y	Yes

### 3.6.1 MULTIPLIER

The 17-bit x 17-bit multiplier is capable of signed or unsigned operation and can multiplex its output using a scaler to support either 1.31 fractional (Q31) or 32-bit integer results. Unsigned operands are zero-extended into the 17th bit of the multiplier input value. Signed operands are sign-extended into the 17th bit of the multiplier input value. Signed to 40 bits. Integer data is inherently represented as a signed 2's complement value, where the Most Significant bit (MSb) is defined as a sign bit. The range of an N-bit 2's complement integer is  $-2^{N-1}$  to  $2^{N-1} - 1$ .

- For a 16-bit integer, the data range is -32768 (0x8000) to 32767 (0x7FFF) including 0.
- For a 32-bit integer, the data range is
   -2,147,483,648 (0x8000 0000) to 2,147,483,647 (0x7FFF FFFF).

When the multiplier is configured for fractional multiplication, the data is represented as a 2's complement fraction, where the MSb is defined as a sign bit and the radix point is implied to lie just after the sign bit (QX format). The range of an N-bit 2's complement fraction with this implied radix point is -1.0 to  $(1 - 2^{1-N})$ . For a 16-bit fraction, the Q15 data range is -1.0 (0x8000) to 0.999969482 (0x7FFF) including 0 and has a precision of 3.01518x10<sup>-5</sup>. In Fractional mode, the 16 x 16 multiply operation generates a 1.31 product that has a precision of 4.65661 x 10<sup>-10</sup>.

The same multiplier is used to support the MCU multiply instructions, which include integer 16-bit signed, unsigned and mixed sign multiply operations.

The MUL instruction can be directed to use byte- or word-sized operands. Byte operands will direct a 16-bit result, and word operands will direct a 32-bit result to the specified register(s) in the W array.

### 3.6.2 DATA ACCUMULATORS AND ADDER/SUBTRACTER

The data accumulator consists of a 40-bit adder/ subtracter with automatic sign extension logic. It can select one of two accumulators (A or B) as its preaccumulation source and post-accumulation destination. For the ADD and LAC instructions, the data to be accumulated or loaded can be optionally scaled using the barrel shifter prior to accumulation.

## 3.6.2.1 Adder/Subtracter, Overflow and Saturation

The adder/subtracter is a 40-bit adder with an optional zero input into one side, and either true or complement data into the other input.

- In the case of addition, the Carry/Borrow input is active-high and the other input is true data (not complemented).
- In the case of subtraction, the Carry/Borrow input is active-low and the other input is complemented.

The adder/subtracter generates Overflow Status bits, SA/SB and OA/OB, which are latched and reflected in the STATUS register:

- Overflow from bit 39: this is a catastrophic overflow in which the sign of the accumulator is destroyed.
- Overflow into guard bits 32 through 39: this is a recoverable overflow. This bit is set whenever all the guard bits are not identical to each other.

The adder has an additional saturation block that controls accumulator data saturation, if selected. It uses the result of the adder, the Overflow Status bits described previously and the SAT<A:B> (CORCON<7:6>) and ACCSAT (CORCON<4>) mode control bits to determine when and to what value, to saturate.

Six STATUS register bits support saturation and overflow:

- OA: ACCA overflowed into guard bits
- OB: ACCB overflowed into guard bits
- SA: ACCA saturated (bit 31 overflow and saturation)

ACCA overflowed into guard bits and saturated (bit 39 overflow and saturation)

- SB: ACCB saturated (bit 31 overflow and saturation)
- or

ACCB overflowed into guard bits and saturated (bit 39 overflow and saturation)

- OAB: Logical OR of OA and OB
- SAB: Logical OR of SA and SB

The OA and OB bits are modified each time data passes through the adder/subtracter. When set, they indicate that the most recent operation has overflowed into the accumulator guard bits (bits 32 through 39). The OA and OB bits can also optionally generate an arithmetic warning trap when OA and OB are set and the corresponding Overflow Trap Flag Enable bits (OVATE, OVBTE) in the INTCON1 register are set (refer to **Section 7.0 "Interrupt Controller"**). This allows the user application to take immediate action; for example, to correct system gain.

### 6.1 System Reset

The dsPIC33FJ12MC201/202 family of devices have two types of Reset:

- Cold Reset
- Warm Reset

A cold Reset is the result of a POR or a BOR. On a cold Reset, the FNOSC configuration bits in the FOSC device configuration register selects the device clock source.

A warm Reset is the result of all other Reset sources, including the RESET instruction. On warm Reset, the device will continue to operate from the current clock source as indicated by the Current Oscillator Selection (COSC<2:0>) bits in the Oscillator Control (OSCCON<14:12>) register.

Oscillator Mode	Oscillator Startup Delay	Oscillator Startup Timer	PLL Lock Time	Total Delay
FRC, FRCDIV16, FRCDIVN	Toscd		_	Toscd
FRCPLL	Toscd	—	TLOCK	Toscd + Tlock
XT	Toscd	Tost	—	Toscd + Tost
HS	Toscd	Tost	—	Toscd + Tost
EC	—	—	—	—
XTPLL	Toscd	Tost	TLOCK	TOSCD + TOST + TLOCK
HSPLL	Toscd	Tost	TLOCK	TOSCD + TOST + TLOCK
ECPLL	—	—	TLOCK	TLOCK
SOSC	Toscd	Tost	—	Toscd + Tost
LPRC	Toscd	—	—	Toscd

### TABLE 6-1:OSCILLATOR DELAY

**Note 1:** TOSCD = Oscillator Start-up Delay (1.1 μs max for FRC, 70 μs max for LPRC). Crystal Oscillator start-up times vary with crystal characteristics, load capacitance, etc.

**2:** TOST = Oscillator Start-up Timer Delay (1024 oscillator clock period). For example, TOST = 102.4 μs for a 10 MHz crystal and TOST = 32 ms for a 32 kHz crystal.

**3:** TLOCK = PLL lock time (1.5 ms nominal), if PLL is enabled.

The device is kept in a Reset state until the system power supplies have stabilized at appropriate levels and the oscillator clock is ready. The sequence in which this occurs is detailed below and is shown in Figure 6-2.

### 7.3 Interrupt Control and Status Registers

The dsPIC33FJ12MC201/202 devices implement a total of 22 registers for the interrupt controller:

- INTCON1
- INTCON2
- IFSx
- IECx
- IPCx
- INTTREG

### 7.3.1 INTCON1 AND INTCON2

Global interrupt control functions are controlled from INTCON1 and INTCON2. INTCON1 contains the Interrupt Nesting Disable (NSTDIS) bit as well as the control and status flags for the processor trap sources. The INTCON2 register controls the external interrupt request signal behavior and the use of the Alternate Interrupt Vector Table.

### 7.3.2 IFSx

The IFS registers maintain all of the interrupt request flags. Each source of interrupt has a status bit, which is set by the respective peripherals or external signal and is cleared via software.

### 7.3.3 IECx

The IEC registers maintain all of the interrupt enable bits. These control bits are used to individually enable interrupts from the peripherals or external signals.

### 7.3.4 IPCx

The IPC registers are used to set the interrupt priority level for each source of interrupt. Each user interrupt source can be assigned to one of eight priority levels.

### 7.3.5 INTTREG

The INTTREG register contains the associated interrupt vector number and the new CPU interrupt priority level, which are latched into vector number (VECNUM<6:0>) and interrupt level (ILR<3:0>) bit fields in the INTTREG register. The new interrupt priority level is the priority of the pending interrupt.

The interrupt sources are assigned to the IFSx, IECx and IPCx registers in the same sequence that they are listed in Table 7-1. For example, the INT0 (External Interrupt 0) is shown as having vector number 8 and a natural order priority of 0. Thus, the INT0IF bit is found in IFS0<0>, the INT0IE bit in IEC0<0>, and the INT0IP bits in the first positions of IPC0 (IPC0<2:0>).

### 7.3.6 STATUS/CONTROL REGISTERS

Although they are not specifically part of the interrupt control hardware, two of the CPU Control registers contain bits that control interrupt functionality.

- The CPU STATUS register, SR, contains the IPL<2:0> bits (SR<7:5>). These bits indicate the current CPU interrupt priority level. The user application can change the current CPU priority level by writing to the IPL bits.
- The CORCON register contains the IPL3 bit which, together with IPL<2:0>, also indicates the current CPU priority level. IPL3 is a read-only bit so that trap events cannot be masked by the user software.

All Interrupt registers are described in Register 7-1 through Register 7-24 in the following pages.

### REGISTER 7-9: IEC0: INTERRUPT ENABLE CONTROL REGISTER 0 (CONTINUED)

- bit 1 IC1IE: Input Capture Channel 1 Interrupt Enable bit
  - 1 = Interrupt request enabled0 = Interrupt request not enabled
- bit 0 **INTOIE:** External Interrupt 0 Enable bit
  - 1 = Interrupt request enabled
  - 0 = Interrupt request not enabled

### REGISTER 7-21: IPC15: INTERRUPT PRIORITY CONTROL REGISTER 15

U-0	R/W-1	R/W-0	R/W-0	U-0	U-0	U-0	U-0		
_		FLTA1IP<2:0>			<u> </u>	_	<u> </u>		
bit 15	bit 15						bit 8		
U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0		
—	—	—	_	—	—	—	—		
bit 7							bit 0		
Legend:									
R = Readable bit W = Writa			able bit U = Unimplemented bit, read as '0'						
-n = Value at	POR	'1' = Bit is set		'0' = Bit is cleared x = Bit is unknown					
bit 15	Unimpleme	nted: Read as '	0'						
bit 14-12	FLTA1IP<2:	0>: PWM1 Faul	t A Interrupt F	Priority bits					
	111 = Interr	upt is priority 7 (	highest priori	ty interrupt)					
	•								
	•								
	•	unt in priority 1							
	001 =  Interrupt is priority 1								
bit 11 0	Unimplomo	ntod. Dood os '	0'						
	ommpieme	meu. Reau as	U						

### REGISTER 7-22: IPC16: INTERRUPT PRIORITY CONTROL REGISTER 16

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	_	—	—	—
bit 15							bit 8
U-0	R/W-1	R/W-0	R/W-0	U-0	U-0	U-0	U-0
—		U1EIP<2:0>		_	—	—	—
bit 7							bit 0

Legend:				
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'		
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown	

### 7.4 Interrupt Setup Procedures

### 7.4.1 INITIALIZATION

To configure an interrupt source at initialization:

- 1. Set the NSTDIS bit (INTCON1<15>) if nested interrupts are not desired.
- Select the user-assigned priority level for the interrupt source by writing the control bits into the appropriate IPCx register. The priority level will depend on the specific application and type of interrupt source. If multiple priority levels are not desired, the IPCx register control bits for all enabled interrupt sources can be programmed to the same non-zero value.

**Note:** At a device Reset, the IPCx registers are initialized such that all user interrupt sources are assigned to priority level 4.

- 3. Clear the interrupt flag status bit associated with the peripheral in the associated IFSx register.
- 4. Enable the interrupt source by setting the interrupt enable control bit associated with the source in the appropriate IECx register.

### 7.4.2 INTERRUPT SERVICE ROUTINE (ISR)

The method used to declare an Interrupt Service Routine (ISR) and initialize the IVT with the correct vector address depends on the programming language (C or assembler) and the language development tool suite used to develop the application.

In general, the user application must clear the interrupt flag in the appropriate IFSx register for the source of interrupt that the ISR handles. Otherwise, program will re-enter the ISR immediately after exiting the routine. If the ISR is coded in assembly language, it must be terminated using a RETFIE instruction to unstack the saved PC value, SRL value and old CPU priority level.

### 7.4.3 TRAP SERVICE ROUTINE (TSR)

A Trap Service Routine (TSR) is coded like an ISR, except that the appropriate trap status flag in the INTCON1 register must be cleared to avoid re-entry into the TSR.

### 7.4.4 INTERRUPT DISABLE

All user interrupts can be disabled using this procedure:

- 1. Push the current SR value onto the software stack using the PUSH instruction.
- 2. Force the CPU to priority level 7 by inclusive ORing the value OEh with SRL.

To enable user interrupts, the POP instruction can be used to restore the previous SR value.

Note:	Only user interrupts with a priority level of
	7 or lower can be disabled. Trap sources
	(level 8-level 15) cannot be disabled.

The DISI instruction provides a convenient way to disable interrupts of priority levels 1-6 for a fixed period of time. Level 7 interrupt sources are not disabled by the DISI instruction.

### REGISTER 8-4: OSCTUN: FRC OSCILLATOR TUNING REGISTER<sup>(2)</sup>

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0		
_	_	—		_		—	_		
bit 15			·				bit 8		
U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
_			TUN<5:0> <sup>(1)</sup>						
bit 7		bit 0							
Legend:									
R = Readable	bit	W = Writable I	bit	U = Unimpler	nented bit, read	l as '0'			
-n = Value at POR '1' = Bit is set				'0' = Bit is cle	ared	x = Bit is unkr	iown		
bit 15-6	Unimplemen	ted: Read as 'd	כי						
bit 5-0	<b>TUN&lt;5:0&gt;:</b> FI	RC Oscillator T	uning bits <sup>(1)</sup>						
	011111 <b>= Ce</b>	nter frequency	+11.625% (8	.23 MHz)					
	011110 <b>= Ce</b>	nter frequency	+11.25% (8.2	20 MHz)					
	•								
	•								
	• 000001 = Ce	nter frequency	+0 375% (7 4	10 MHz)					
	000000 = Ce	nter frequency	(7.37 MHz nd	ominal)					
	111111 = Center frequency -0.375% (7.345 MHz)								
	•			-					
	•								
	•		44.0050/ /0						
	100001 = Ce	nter frequency	-11.625% (6.	52 MHz)					
	T00000 = Ce	nter frequency	-12% (6.49 N	(IHZ)					

- **Note 1:** OSCTUN functionality has been provided to help customers compensate for temperature effects on the FRC frequency over a wide range of temperatures. The tuning step size is an approximation and is neither characterized nor tested.
  - 2: This register is reset only on a Power-on Reset (POR).

### REGISTER 10-20: RPOR6: PERIPHERAL PIN SELECT OUTPUT REGISTER 6

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	RP13R<4:0>				
bit 15							bit 8
U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—			RP12R<4:0>		
bit 7		•					bit 0
Legend:							

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'		
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown	

bit 15-13	Unimplemented: Read as '0'
-----------	----------------------------

- bit 12-8 **RP13R<4:0>:** Peripheral Output Function is Assigned to RP13 Output Pin bits (see Table 10-2 for peripheral function numbers)
- bit 7-5 Unimplemented: Read as '0'
- bit 4-0 **RP12R<4:0>:** Peripheral Output Function is Assigned to RP12 Output Pin bits (see Table 10-2 for peripheral function numbers)

### REGISTER 10-21: RPOR7: PERIPHERAL PIN SELECT OUTPUT REGISTER 7

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—			RP15R<4:0>		
bit 15							bit 8

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—			RP14R<4:0>		
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-13 Unimplemented: Read as '0'

bit 12-8 **RP15R<4:0>:** Peripheral Output Function is Assigned to RP15 Output Pin bits (see Table 10-2 for peripheral function numbers)

bit 7-5 Unimplemented: Read as '0'

bit 4-0 **RP14R<4:0>:** Peripheral Output Function is Assigned to RP14 Output Pin bits (see Table 10-2 for peripheral function numbers)

R/W-0	U-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0
UARTEN <sup>(1)</sup>		USIDL	IREN <sup>(2)</sup>	RTSMD		UEN	<1:0>
bit 15							bit 8
R/W-0 HC	R/W-0	R/W-0 HC	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
WAKE	LPBACK	ABAUD	URXINV	BRGH	PDSE	L<1:0>	STSEL
bit 7							bit 0
Legend:		HC = Hardwa	re cleared				
R = Readable	bit	W = Writable	bit	U = Unimpler	mented bit, read	d as '0'	
-n = Value at I	POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	nown
bit 15 <b>UARTEN:</b> UARTx Enable bit <sup>(1)</sup> 1 = UARTx is enabled; all UARTx pins are controlled by UARTx as defined by UEN<1:0> 0 = UARTx is disabled; all UARTx pins are controlled by port latches; UARTx power consumption minimal							0> onsumption
bit 14	Unimplemen	ted: Read as '	0'				
bit 13	USIDL: Stop i	in Idle Mode bit	t				
	1 = Discontin 0 = Continue	ue module ope module operat	eration when o tion in Idle mo	device enters lo ode	dle mode		
bit 12	IREN: IrDA <sup>®</sup> I	Encoder and D	ecoder Enabl	e bit <sup>(2)</sup>			
	1 = IrDA enco0 = IrDA enco	oder and decoo oder and decoo	der enabled der disabled				
bit 11	RTSMD: Mod	le Selection for	UxRTS Pin b	it			
	<ul> <li>1 = UxRTS pin in Simplex mode</li> <li>0 = UxRTS pin in Flow Control mode</li> </ul>						
bit 10	Unimplemen	ted: Read as '	0'				
bit 9-8	UEN<1:0>: U	ARTx Enable b	oits				
<ul> <li>11 = UxTX, UxRX and BCLK pins are enabled and used; UxCTS pin controlled by port latches</li> <li>10 = UxTX, UxRX, UxCTS and UxRTS pins are enabled and used</li> <li>01 = UxTX, UxRX and UxRTS pins are enabled and used; UxCTS pin controlled by port latches</li> <li>00 = UxTX and UxRX pins are enabled and used; UxCTS and UxRTS/BCLK pins controlled by port latches</li> </ul>							
bit 7	WAKE: Wake	-up on Start bit	Detect Durin	g Sleep Mode	Enable bit		
	<ul> <li>1 = UARTx will continue to sample the UxRX pin; interrupt generated on falling edge; bit cleared in hardware on following rising edge</li> <li>0 = No wake-up enabled</li> </ul>						
bit 6	LPBACK: UA	RTx Loopback	Mode Select	bit			
	1 = Enable L	oopback mode					
	0 = Loopback	k mode is disab	bled				
bit 5	ABAUD: Auto	-Baud Enable	bit				
	1 = Enable ba	aud rate meas her data; cleare	urement on the	e next charac e upon comple	ter – requires re tion	eception of a Sy	ync field (55h)
	0 = Baud rate	e measurement	t disabled or c	completed			
Note 1: Re ino	fer to <b>Section 1</b> rmation on enat	7. "UART" (DS oling the UART	S70188) in the module for re	e <i>"dsPIC33F/P</i> eceive or trans	PIC24H Family I mit operation.	Reference Manı	ual" for

### **REGISTER 19-1: UXMODE: UARTX MODE REGISTER**

**2:** This feature is only available for the 16x BRG mode (BRGH = 0).

R/W-0	R/W-0	R/W-0	U-0	R/W-0 HC	R/W-0	R-0	R-1
UTXISEL1	UTXINV	UTXISEL0		UTXBRK	UTXEN <sup>(1)</sup>	UTXBF	TRMT
bit 15							bit 8
L							
R/W-0	R/W-0	R/W-0	R-1	R-0	R-0	R/C-0	R-0
URXISE	EL<1:0>	ADDEN	RIDLE	PERR	FERR	OERR	URXDA
bit 7					•	·	bit 0
Legend:		HC = Hardwar	e cleared				
R = Readable	bit	W = Writable b	oit	U = Unimpler	mented bit, read	as '0'	
-n = Value at P	OR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	iown
bit 15,13 bit 14	<ul> <li>bit 15,13 UTXISEL&lt;1:0&gt;: Transmission Interrupt Mode Selection bits <ol> <li>Reserved; do not use</li> <li>Interrupt when a character is transferred to the Transmit Shift Register, and as a result, the transmit buffer becomes empty</li> <li>Interrupt when the last character is shifted out of the Transmit Shift Register; all transmit operations are completed</li> <li>Interrupt when a character is transferred to the Transmit Shift Register (this implies there at least one character open in the transmit buffer)</li> </ol> </li> <li>bit 14 UTXINV: Transmit Polarity Inversion bit <ul> <li>If IREN = 0:</li> <li>I = UxTX Idle state is '0'</li> <li>I = UxTX Idle state is '1'</li> <li>If IREN = 1:</li> </ul> </li> </ul>						esult, the ansmit s there is
bit 12	Unimplement	ted: Read as '0	)'				
bit 11	UTXBRK: Tra	ansmit Break bit	t				
bit 10	<ul> <li>1 = Send Sync Break on next transmission – Start bit, followed by twelve '0' bits, followed by Stop bit; cleared by hardware upon completion</li> <li>0 = Sync Break transmission disabled or completed</li> <li>UTXEN: Transmit Enable bit<sup>(1)</sup></li> <li>1 = Transmit enabled _UTX sin centrelled by LIAPTy.</li> </ul>						
	0 = Transmit by port.	disabled, any p	bending trans	smission is abo	rted and buffer	is reset. UxTX	pin controlled
bit 9	UTXBF: Trans	smit Buffer Full	Status bit (re	ead-only)			
	1 = Transmit 0 = Transmit	buffer is full buffer is not ful	l, at least one	e more charact	er can be writte	n	
bit 8	TRMT: Transr	nit Shift Registe	er Empty bit	(read-only)			
	1 = Transmit 0 = Transmit	Shift Register is Shift Register is	empty and t s not empty,	ransmit buffer is a transmission	s empty (the last is in progress o	transmission h r queued	as completed)
bit 7-6	URXISEL<1:0	D>: Receive Inte	errupt Mode	Selection bits			
	<ul> <li>11 = Interrupt is set on UxRSR transfer making the receive buffer full (i.e., has 4 data characters)</li> <li>10 = Interrupt is set on UxRSR transfer making the receive buffer 3/4 full (i.e., has 3 data characters)</li> <li>0x = Interrupt is set when any character is received and transferred from the UxRSR to the receive buffer. Receive buffer has one or more characters.</li> </ul>						

### REGISTER 19-2: UxSTA: UARTx STATUS AND CONTROL REGISTER

**Note 1:** Refer to **Section 17. "UART**" (DS70188) in the *"dsPIC33F/PIC24H Family Reference Manual"* for information on enabling the UART module for transmit operation.

Base Instr #	Assembly Mnemonic		Assembly Syntax	Description	# of Words	# of Cycles	Status Flags Affected
48	MPY	MPY Wm*Wn,Ad	cc,Wx,Wxd,Wy,Wyd	Multiply Wm by Wn to Accumulator	1	1	OA,OB,OAB, SA,SB,SAB
		MPY Wm*Wm,A	cc,Wx,Wxd,Wy,Wyd	Square Wm to Accumulator	1	1	OA,OB,OAB, SA,SB,SAB
49	MPY.N	MPY.N Wm*Wn,Ad	cc,Wx,Wxd,Wy,Wyd	-(Multiply Wm by Wn) to Accumulator	1	1	None
50	MSC	MSC	Wm*Wm,Acc,Wx,Wxd,Wy,Wyd , AWB	Multiply and Subtract from Accumulator	1	1	OA,OB,OAB, SA,SB,SAB
51	MUL	MUL.SS	Wb,Ws,Wnd	{Wnd + 1, Wnd} = signed(Wb) * signed(Ws)	1	1	None
		MUL.SU	Wb,Ws,Wnd	{Wnd + 1, Wnd} = signed(Wb) * unsigned(Ws)	1	1	None
		MUL.US	Wb,Ws,Wnd	{Wnd + 1, Wnd} = unsigned(Wb) * signed(Ws)	1	1	None
		MUL.UU	Wb,Ws,Wnd	{Wnd + 1, Wnd} = unsigned(Wb) * unsigned(Ws)	1	1	None
		MUL.SU	Wb,#lit5,Wnd	{Wnd + 1, Wnd} = signed(Wb) * unsigned(lit5)	1	1	None
		MUL.UU	Wb,#lit5,Wnd	{Wnd + 1, Wnd} = unsigned(Wb) * unsigned(lit5)	1	1	None
		MUL	f	W3:W2 = f * WREG	1	1	None
52	NEG	NEG	Acc	Negate Accumulator	1	1	OA,OB,OAB, SA,SB,SAB
		NEG	f	$f = \overline{f} + 1$	1	1	C,DC,N,OV,Z
		NEG	f,WREG	WREG = $\overline{f}$ + 1	1	1	C,DC,N,OV,Z
		NEG	Ws,Wd	$Wd = \overline{Ws} + 1$	1	1	C,DC,N,OV,Z
53	NOP	NOP		No Operation	1	1	None
		NOPR		No Operation	1	1	None
54	POP	POP	f	Pop f from Top-of-Stack (TOS)	1	1	None
		POP	Wdo	Pop from Top-of-Stack (TOS) to Wdo	1	1	None
		POP.D	Wnd	Pop from Top-of-Stack (TOS) to W(nd):W(nd + 1)	1	2	None
		POP.S		Pop Shadow Registers	1	1	All
55	PUSH	PUSH	f	Push f to Top-of-Stack (TOS)	1	1	None
		PUSH	Wso	Push Wso to Top-of-Stack (TOS)	1	1	None
		PUSH.D	Wns	Push W(ns):W(ns + 1) to Top-of-Stack (TOS)	1	2	None
		PUSH.S		Push Shadow Registers	1	1	None
56	PWRSAV	PWRSAV	#lit1	Go into Sleep or Idle mode	1	1	WDTO,Sleep
57	RCALL	RCALL	Expr	Relative Call	1	2	None
		RCALL	Wn	Computed Call	1	2	None
58	REPEAT	REPEAT	#lit14	Repeat Next Instruction lit14 + 1 times	1	1	None
50		REPEAT	Wn	Repeat Next Instruction (Wn) + 1 times	1	1	None
59	RESET	RESET		Software device Reset	1	1	None
61	RETFIE	RETFIE	#1:+10 m	Return with literal in Wn	1	3 (2)	None
62	REILW	REILW	#IICIO,WN	Return from Subrouting	1	3(2)	None
63	RETURN	RETURN	£	f = Poteto L off through Corry f	1	3 (2)	
03	RLC	RLC	f NDEC	WPEG = Potate Loft through Carry f	1	1	C,N,Z
		RLC	WS Wd	Wd = Rotate Left through Carry Ws	1	1	C. N. Z
64	RLNC	RLNC	f	f = Rotate Left (No Carry) f	1	1	N 7
		RLNC	- f.WREG	WREG = Rotate Left (No Carry) f	1	1	N 7
		RLNC	Ws,Wd	Wd = Rotate Left (No Carry) Ws	1	1	N.Z
65	RRC	RRC	f	f = Rotate Right through Carry f	1	1	C,N,Z
		RRC	f,WREG	WREG = Rotate Right through Carry f	1	1	C,N,Z
		RRC	Ws,Wd	Wd = Rotate Right through Carry Ws	1	1	C,N,Z

### TABLE 22-2: INSTRUCTION SET OVERVIEW (CONTINUED)

### TABLE 24-21: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER, POWER-UP TIMER TIMING REQUIREMENTS

AC CHARACTERISTICS			<b>Stand</b> a (unles Opera	ard Ope s other ting tem	rating ( wise sta perature	Conditio ated) e -40°( -40°(	ns: 3.0V to 3.6V C ≤ TA ≤+85°C for Industrial C ≤TA ≤+125°C for Extended
Param No.	Symbol	Characteristic <sup>(1)</sup>	Min	Тур <sup>(2)</sup>	Max	Units	Conditions
SY10	ТмсL	MCLR Pulse Width (low)	2	_	_	μs	-40°C to +85°C
SY11	TPWRT	Power-up Timer Period <sup>(1)</sup>		2 4 16 32 64 128	_	ms	-40°C to +85°C User programmable
SY12	TPOR	Power-on Reset Delay <sup>(3)</sup>	3	10	30	μs	-40°C to +85°C
SY13	Tioz	I/O High-Impedance from MCLR Low or Watchdog Timer Reset <sup>(1)</sup>	0.68	0.72	1.2	μs	—
SY20	Twdt1	Watchdog Timer Time-out Period <sup>(1)</sup>				ms	See Section 21.4 "Watch- dog Timer (WDT)" and LPRC parameter F21a (Table 24-19).
SY30	Tost	Oscillator Start-up Time	_	1024 Tosc	_	_	Tosc = OSC1 period
SY35	TFSCM	Fail-Safe Clock Monitor Delay <sup>(1)</sup>		500	900	μs	-40°C to +85°C

Note 1: These parameters are characterized but not tested in manufacturing.

**2:** Data in "Typ" column is at 3.3V, 25°C unless otherwise stated.

3: These parameters are characterized, but are not tested in manufacturing.

AC CHARACTERISTICS			<b>Standar</b> (unless Operatir	d Opera otherwing tempe	ting Con se statec rature	<b>ditions:</b> I) 40°C ≤⊺ 40°C ≤T	<b>3.0V to 3.6V</b> TA ≤+85°C for Industrial A ≤+125°C for Extended
Param No.	Symbol	Characteristic	Min.	Тур	Max.	Units	Conditions
	ŀ	ADC Accuracy (12-bit Mod	e) – Meas	suremen	ts with e	xternal	Vref+/Vref- <sup>(3)</sup>
AD20a	Nr	Resolution <sup>(4)</sup>	1:	2 data bi	ts	bits	—
AD21a	INL	Integral Nonlinearity	-2	—	+2	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.6V
AD22a	DNL	Differential Nonlinearity	>-1	—	<1	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.6V
AD23a	Gerr	Gain Error	—	3.4	10	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.6V
AD24a	EOFF	Offset Error	—	0.9	5.0	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.6V
AD25a	—	Monotonicity	_	—	—		Guaranteed <sup>(1)</sup>
		ADC Accuracy (12-bit Mod	e) – Mea	suremer	nts with i	nternal	Vref+/Vref- <sup>(3)</sup>
AD20a	Nr	Resolution <sup>(4)</sup>	1	2 data bi	ts	bits	
AD21a	INL	Integral Nonlinearity	-2		+2	LSb	VINL = AVSS = 0V, AVDD = 3.6V
AD22a	DNL	Differential Nonlinearity	>-1	—	<1	LSb	VINL = AVSS = 0V, AVDD = 3.6V
AD23a	Gerr	Gain Error	2	10.5	20	LSb	VINL = AVSS = 0V, AVDD = 3.6V
AD24a	EOFF	Offset Error	2	3.8	10	LSb	VINL = AVSS = 0V, AVDD = 3.6V
AD25a	—	Monotonicity		—	—	_	Guaranteed <sup>(1)</sup>
		Dynamic	Perform	ance (12	-bit Mod	e) <sup>(2)</sup>	
AD30a	THD	Total Harmonic Distortion	—	—	-75	dB	_
AD31a	SINAD	Signal to Noise and Distortion	68.5	69.5	—	dB	—
AD32a	SFDR	Spurious Free Dynamic Range	80			dB	_
AD33a	Fnyq	Input Signal Bandwidth			250	kHz	
AD34a	ENOB	Effective Number of Bits	11.09	11.3	—	bits	

### TABLE 24-43: ADC MODULE SPECIFICATIONS (12-BIT MODE)

**Note 1:** The A/D conversion result never decreases with an increase in the input voltage, and has no missing codes.

2: These parameters are characterized by similarity, but are not tested in manufacturing.

3: These parameters are characterized, but are tested at 20 ksps only.

4: Injection currents > | 0 | can affect the ADC results by approximately 4-6 counts.

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NOTES:

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### 25.1 Package Marking Information (Continued)



**Note:** If the full Microchip part number cannot be marked on one line, it is carried over to the next line, thus limiting the number of available characters for customer-specific information.

### TABLE 25-1: MAJOR SECTION UPDATES

Section Name	Update Description
Section 24.0 "Packaging Information"	Added 28-lead SSOP package marking information.
"Product Identification System"	Added Plastic Shrink Small Outline (SSOP) package information.

### **Revision D (June 2009)**

This revision includes minor typographical and formatting changes throughout the data sheet text.

Global changes include:

- Changed all instances of OSCI to OSC1 and OSCO to OSC2
- Changed all instances of PGCx/EMUCx and PGDx/EMUDx (where x = 1, 2, or 3) to PGECx and PGEDx

Changed all instances of VDDCORE and VDDCORE/VCAP to VCAP/VDDCORE

All other major changes are referenced by their respective section in the following table.

### TABLE 25-2: MAJOR SECTION UPDATES

Section Name	Update Description
"High-Performance, 16-bit Digital Signal Controllers"	Added Note 2 to the 28-Pin QFN-S and 44-Pin QFN pin diagrams, which references pin connections to Vss.
Section 2.0 "Guidelines for Getting Started with 16-bit Digital Signal Controllers"	Added new section to the data sheet that provides guidelines on getting started with 16-bit Digital Signal Controllers.
Section 8.0 "Oscillator Configuration"	Updated the Oscillator System Diagram (see Figure 8-1).
	Added Note 1 to the Oscillator Tuning (OSCTUN) register (see Register 8-4).
Section 10.0 "I/O Ports"	Removed Table 10-1 and added reference to pin diagrams for I/O pin availability and functionality.
Section 17.0 "Serial Peripheral Interface (SPI)"	Added Note 2 to the SPIx Control Register 1 (see Register 17-2).
Section 19.0 "Universal Asynchronous Receiver Transmitter (UART)"	Updated the UTXINV bit settings in the UxSTA register and added Note 1 (see Register 19-2).
Section 24.0 "Electrical Characteristics"	Updated the Min value for parameter DC12 (RAM Retention Voltage) and added Note 4 to the DC Temperature and Voltage Specifications (see Table 24-4).
	Updated the Min value for parameter DI35 (see Table 24-20).
	Updated AD08 and added reference to Note 2 for parameters AD05a, AD06a, and AD08a (see Table 24-38).

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NOTES:

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