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Details

Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	40 MIPS
Connectivity	I ² C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, Motor Control PWM, QEI, POR, PWM, WDT
Number of I/O	15
Program Memory Size	12KB (12K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 4x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	20-DIP (0.300", 7.62mm)
Supplier Device Package	20-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33fj12mc201-i-p

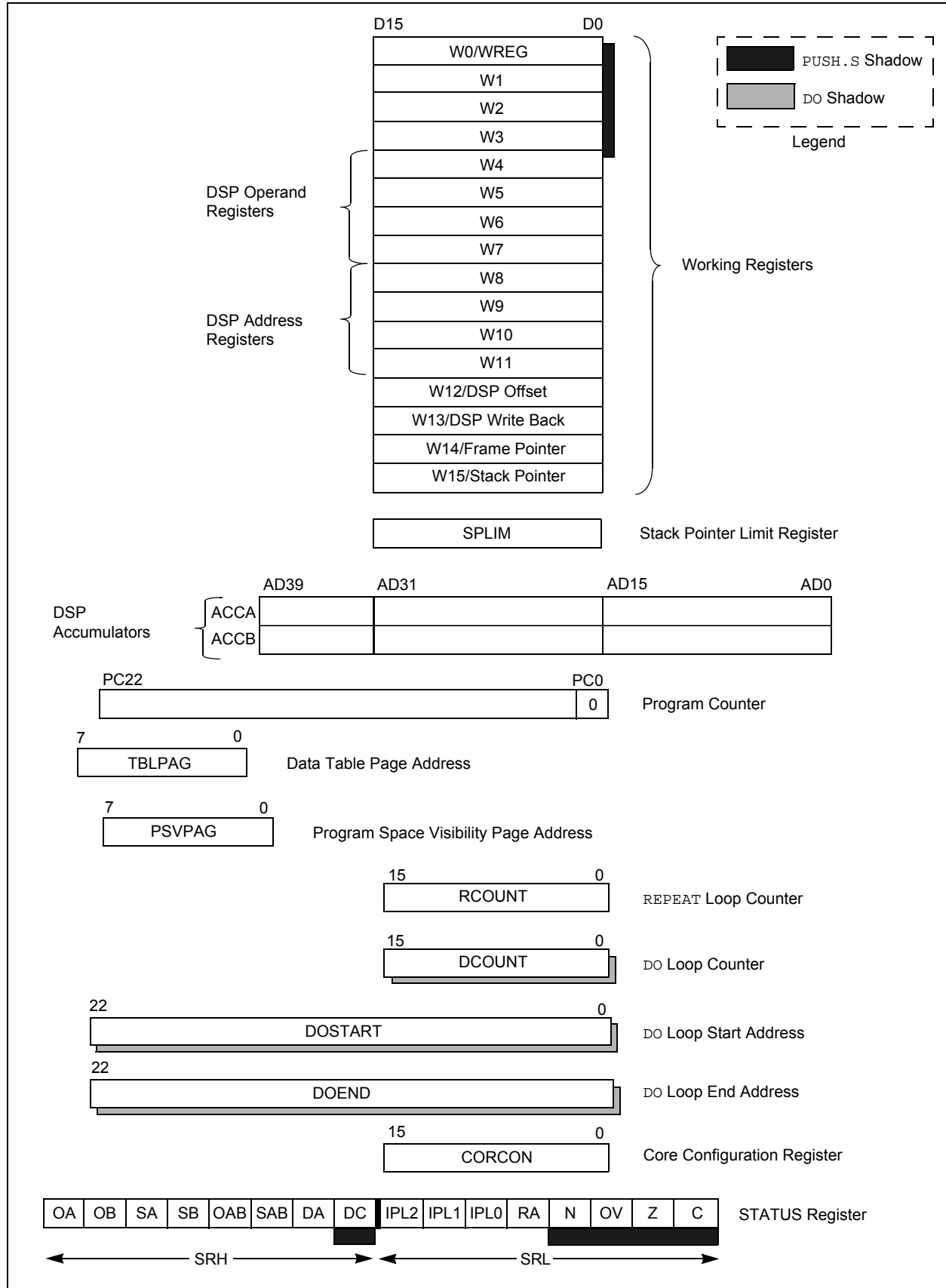
dsPIC33FJ12MC201/202

TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Type	Buffer Type	PPS	Description
INDX	I	ST	Yes	Quadrature Encoder Index Pulse input.
QEA	I	ST	Yes	Quadrature Encoder Phase A input in QEI mode.
QEB	I	ST	Yes	Auxiliary Timer External Clock/Gate input in Timer mode.
UPDN	O	CMOS	Yes	Quadrature Encoder Phase A input in QEI mode.
				Auxiliary Timer External Clock/Gate input in Timer mode.
				Position Up/Down Counter Direction State.
FLTA1	I	ST	Yes	PWM1 Fault A input.
PWM1L1	O	—	No	PWM1 Low output 1
PWM1H1	O	—	No	PWM1 High output 1
PWM1L2	O	—	No	PWM1 Low output 2
PWM1H2	O	—	No	PWM1 High output 2
PWM1L3	O	—	No	PWM1 Low output 3
PWM1H3	O	—	No	PWM1 High output 3
FLTA2	I	ST	Yes	PWM2 Fault A input.
PWM2L1	O	—	No	PWM2 Low output 1
PWM2H1	O	—	No	PWM2 High output 1
PGED1	I/O	ST	No	Data I/O pin for programming/debugging communication channel 1.
PGEC1	I	ST	No	Clock input pin for programming/debugging communication channel 1.
PGED2	I/O	ST	No	Data I/O pin for programming/debugging communication channel 2.
PGEC2	I	ST	No	Clock input pin for programming/debugging communication channel 2.
PGED3	I/O	ST	No	Data I/O pin for programming/debugging communication channel 3.
PGEC3	I	ST	No	Clock input pin for programming/debugging communication channel 3.
MCLR	I/P	ST	No	Master Clear (Reset) input. This pin is an active-low Reset to the device.
AVDD	P	P	No	Positive supply for analog modules. This pin must be connected at all times.
AVSS	P	P	No	Ground reference for analog modules.
VDD	P	—	No	Positive supply for peripheral logic and I/O pins.
VCAP	P	—	No	CPU logic filter capacitor connection.
VSS	P	—	No	Ground reference for logic and I/O pins.
VREF+	I	Analog	No	Analog voltage reference (high) input.
VREF-	I	Analog	No	Analog voltage reference (low) input.

Legend: CMOS = CMOS compatible input or output Analog = Analog input P = Power
ST = Schmitt Trigger input with CMOS levels O = Output I = Input
PPS = Peripheral Pin Select

FIGURE 3-2: dsPIC33FJ12MC201/202 PROGRAMMER'S MODEL



4.6 Interfacing Program and Data Memory Spaces

The dsPIC33FJ12MC201/202 architecture uses a 24-bit-wide program space and a 16-bit-wide data space. The architecture is also a modified Harvard scheme, meaning that data can also be present in the program space. To use this data successfully, it must be accessed in a way that preserves the alignment of information in both spaces.

Aside from normal execution, the dsPIC33FJ12MC201/202 architecture provides two methods by which program space can be accessed during operation:

- Using table instructions to access individual bytes, or words, anywhere in the program space
- Remapping a portion of the program space into the data space (Program Space Visibility)

Table instructions allow an application to read or write to small areas of the program memory. This capability makes the method ideal for accessing data tables that need to be updated periodically. It also allows access to all bytes of the program word. The remapping method allows an application to access a large block of data on a read-only basis, which is ideal for lookups from a large table of static data. The application can only access the lsw of the program word.

4.6.1 ADDRESSING PROGRAM SPACE

Since the address ranges for the data and program spaces are 16 and 24 bits, respectively, a method is needed to create a 23-bit or 24-bit program address from 16-bit data registers. The solution depends on the interface method to be used.

For table operations, the 8-bit Table Page register (TBLPAG) is used to define a 32K word region within the program space. This is concatenated with a 16-bit EA to arrive at a full 24-bit program space address. In this format, the MSb of TBLPAG is used to determine if the operation occurs in the user memory (TBLPAG<7> = 0) or the configuration memory (TBLPAG<7> = 1).

For remapping operations, the 8-bit Program Space Visibility register (PSVPAG) is used to define a 16K word page in the program space. When the MSb of the EA is '1', PSVPAG is concatenated with the lower 15 bits of the EA to form a 23-bit program space address. Unlike table operations, this limits remapping operations strictly to the user memory area.

Table 4-28 and Figure 4-7 show how the program EA is created for table operations and remapping accesses from the data EA.

TABLE 4-28: PROGRAM SPACE ADDRESS CONSTRUCTION

Access Type	Access Space	Program Space Address				
		<23>	<22:16>	<15>	<14:1>	<0>
Instruction Access (Code Execution)	User	0	PC<22:1>			0
		0xx xxxx xxxx xxxx xxxx xxx0				
TBLRD/TBLWT (Byte/Word Read/Write)	User	TBLPAG<7:0>		Data EA<15:0>		
		0xxx xxxx		xxxx xxxx xxxx xxxx		
	Configuration	TBLPAG<7:0>		Data EA<15:0>		
		1xxx xxxx		xxxx xxxx xxxx xxxx		
Program Space Visibility (Block Remap/Read)	User	0	PSVPAG<7:0>		Data EA<14:0> ⁽¹⁾	
		0	xxxx xxxx		xxx xxxx xxxx xxxx	

Note 1: Data EA<15> is always '1' in this case, but is not used in calculating the program space address. Bit 15 of the address is PSVPAG<0>.

8.1 CPU Clocking System

The dsPIC33FJ12MC201/202 devices provide seven system clock options:

- Fast RC (FRC) Oscillator
- FRC Oscillator with PLL
- Primary (XT, HS or EC) Oscillator
- Primary Oscillator with PLL
- Secondary (LP) Oscillator
- Low-Power RC (LPRC) Oscillator
- FRC Oscillator with postscaler

8.1.1 SYSTEM CLOCK SOURCES

8.1.1.1 Fast RC

The Fast RC (FRC) internal oscillator runs at a nominal frequency of 7.37 MHz. User software can tune the FRC frequency. User software can optionally specify a factor (ranging from 1:2 to 1:256) by which the FRC clock frequency is divided. This factor is selected using the FRCDIV<2:0> (CLKDIV<10:8>) bits.

8.1.1.2 Primary

The primary oscillator can use one of the following as its clock source:

- XT (Crystal): Crystals and ceramic resonators in the range of 3 MHz to 10 MHz. The crystal is connected to the OSC1 and OSC2 pins.
- HS (High-Speed Crystal): Crystals in the range of 10 MHz to 40 MHz. The crystal is connected to the OSC1 and OSC2 pins.
- EC (External Clock): The external clock signal is directly applied to the OSC1 pin.

8.1.1.3 Secondary

The secondary (LP) oscillator is designed for low power and uses a 32.768 kHz crystal or ceramic resonator. The LP oscillator uses the SOSCI and SOSCO pins.

8.1.1.4 Low-Power RC

The Low-Power RC (LPRC) internal oscillator runs at a nominal frequency of 32.768 kHz. It is also used as a reference clock by the Watchdog Timer (WDT) and Fail-Safe Clock Monitor (FSCM).

8.1.1.5 FRC

The clock signals generated by the FRC and primary oscillators can be optionally applied to an on-chip Phase-Locked Loop (PLL) to provide a wide range of output frequencies for device operation. PLL configuration is described in **Section 8.1.3 “PLL Configuration”**.

The FRC frequency depends on the FRC accuracy (see Table 24-18) and the value of the FRC Oscillator Tuning register (see Register 8-4).

8.1.2 SYSTEM CLOCK SELECTION

The oscillator source used at a device Power-on Reset event is selected using Configuration bit settings. The oscillator Configuration bit settings are located in the Configuration registers in the program memory. (Refer to **Section 21.1 “Configuration Bits”** for further details.) The Initial Oscillator Selection Configuration bits, FNOSC<2:0> (FOSCSEL<2:0>), and the Primary Oscillator Mode Select Configuration bits, POSCMD<1:0> (FOSC<1:0>), select the oscillator source that is used at a Power-on Reset. The FRC primary oscillator is the default (unprogrammed) selection.

The Configuration bits allow users to choose among 12 different clock modes, shown in Table 8-1.

The output of the oscillator (or the output of the PLL if a PLL mode has been selected) FOSC is divided by 2 to generate the device instruction clock (FCY) and the peripheral clock time base (FP). FCY defines the operating speed of the device, and speeds up to 40 MHz are supported by the dsPIC33FJ12MC201/202 architecture.

Instruction execution speed or device operating frequency, FCY, is given by:

EQUATION 8-1: DEVICE OPERATING FREQUENCY

$$FCY = \frac{FOSC}{2}$$

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REGISTER 9-3: PMD3: PERIPHERAL MODULE DISABLE CONTROL REGISTER 3

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	R/W-0	U-0	U-0	U-0	U-0
—	—	—	PWM2MD	—	—	—	—
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-5 **Unimplemented:** Read as '0'

bit 4 **PWM2MD:** PWM2 Module Disable bit

1 = PWM2 module is disabled

0 = PWM2 module is enabled

bit 3-0 **Unimplemented:** Read as '0'

10.0 I/O PORTS

Note 1: This data sheet summarizes the features of the dsPIC33FJ12MC201/202 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 10. "I/O Ports"** (DS70193) of the "*dsPIC33F/PIC24H Family Reference Manual*", which is available from the Microchip website (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

All of the device pins (except VDD, VSS, MCLR, and OSC1/CLKI) are shared among the peripherals and the parallel I/O ports. All I/O input ports feature Schmitt Trigger inputs for improved noise immunity.

10.1 Parallel I/O (PIO) Ports

Generally a parallel I/O port that shares a pin with a peripheral is subservient to the peripheral. The peripheral's output buffer data and control signals are provided to a pair of multiplexers. The multiplexers select whether the peripheral or the associated port has ownership of the output data and control signals of

the I/O pin. The logic also prevents "loop through," in which a port's digital output can drive the input of a peripheral that shares the same pin. Figure 10-1 shows how ports are shared with other peripherals and the associated I/O pin to which they are connected.

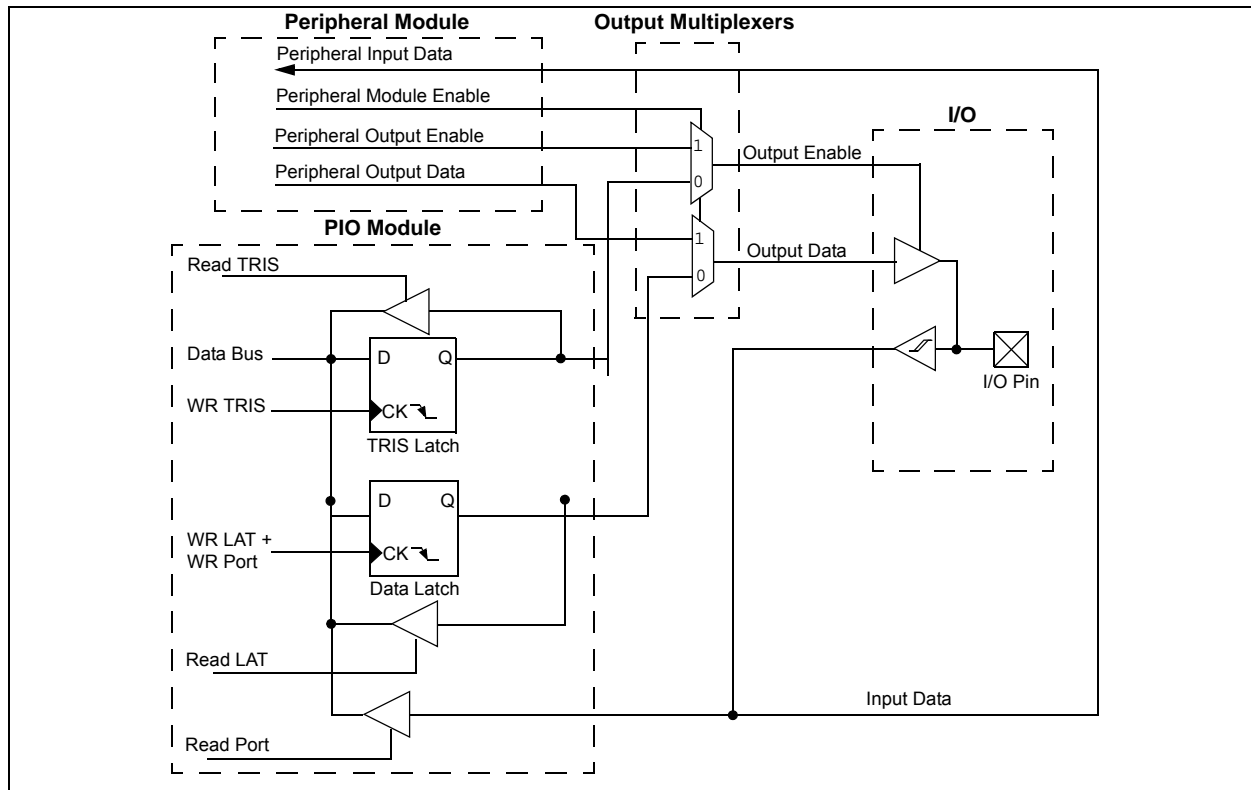
When a peripheral is enabled and the peripheral is actively driving an associated pin, the use of the pin as a general purpose output pin is disabled. The I/O pin can be read, but the output driver for the parallel port bit is disabled. If a peripheral is enabled, but the peripheral is not actively driving a pin, that pin can be driven by a port.

All port pins have three registers directly associated with their operation as digital I/O. The data direction register (TRISx) determines whether the pin is an input or an output. If the data direction bit is a '1', the pin is an input. All port pins are defined as inputs after a Reset. Reads from the latch (LATx) read the latch. Writes to the latch write the latch. Reads from the port (PORTx) read the port pins, while writes to the port pins write the latch.

Any bit and its associated data and control registers that are not valid for a particular device will be disabled. This means the corresponding LATx and TRISx registers and the port pin will read as zeros.

When a pin is shared with another peripheral or function that is defined as an input only, it is nevertheless regarded as a dedicated port because there is no other competing source of outputs.

FIGURE 10-1: BLOCK DIAGRAM OF A TYPICAL SHARED PORT STRUCTURE



NOTES:

13.0 INPUT CAPTURE

Note 1: This data sheet summarizes the features of the dsPIC33FJ12MC201/202 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 12. “Input Capture”** (DS70198) of the “dsPIC33F/PIC24H Family Reference Manual”, which is available from the Microchip website (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

The Input Capture module is useful in applications requiring frequency (period) and pulse measurement. The dsPIC33FJ12MC201/202 devices support up to eight input capture channels.

The Input Capture module captures the 16-bit value of the selected Time Base register when an event occurs at the ICx pin. The events that cause a capture event are listed below in three categories:

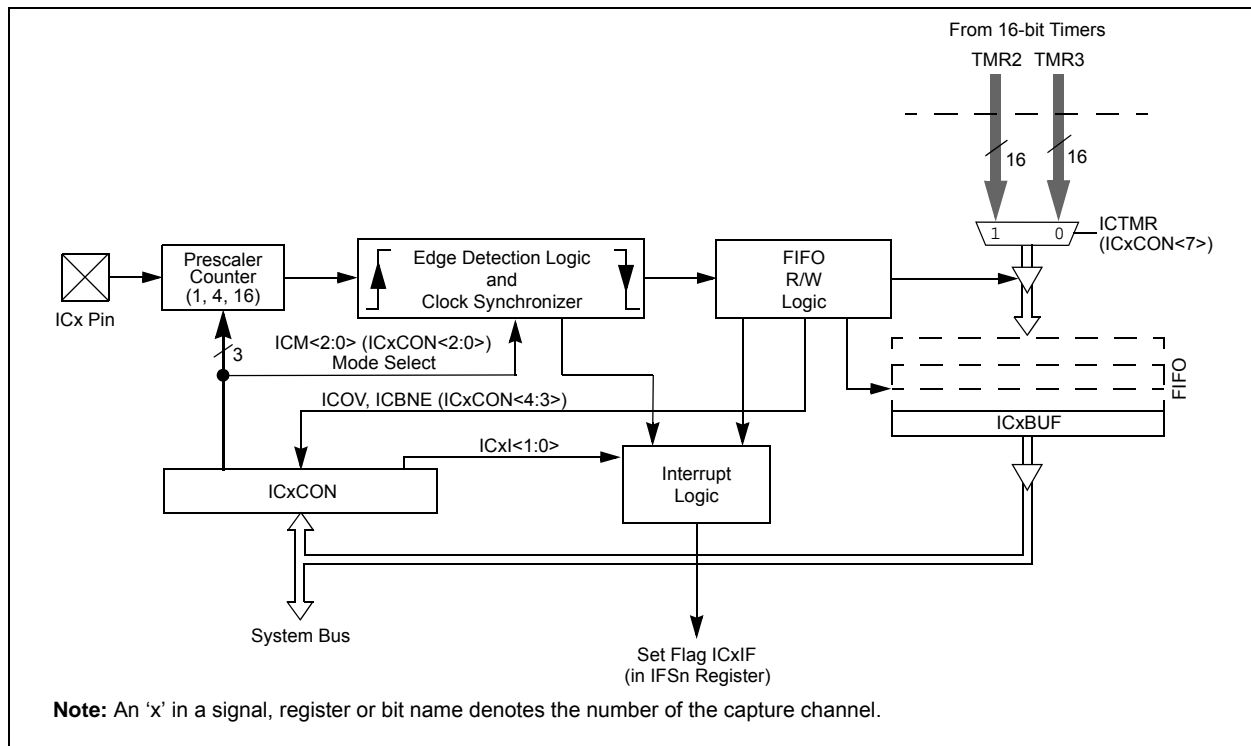
1. Simple Capture Event modes:
 - Capture timer value on every falling edge of input at ICx pin
 - Capture timer value on every rising edge of input at ICx pin
2. Capture timer value on every edge (rising and falling)
3. Prescaler Capture Event modes:
 - Capture timer value on every 4th rising edge of input at ICx pin
 - Capture timer value on every 16th rising edge of input at ICx pin

Each Input Capture channel can select one of two 16-bit timers (Timer2 or Timer3) for the time base. The selected timer can use either an internal or external clock.

Other operational features include:

- Device wake-up from capture pin during CPU Sleep and Idle modes
- Interrupt on Input Capture event
- 4-word FIFO buffer for capture values
 - Interrupt optionally generated after 1, 2, 3, or 4 buffer locations are filled
- Use of Input Capture to provide additional sources of external interrupts

FIGURE 13-1: INPUT CAPTURE BLOCK DIAGRAM



dsPIC33FJ12MC201/202

13.1 Input Capture Registers

REGISTER 13-1: ICxCON: INPUT CAPTURE x CONTROL REGISTER

U-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
—	—	ICSIDL	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R-0, HC	R-0, HC	R/W-0	R/W-0	R/W-0
ICTMR	ICI<1:0>		ICOV	ICBNE	ICM<2:0>		
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13 **ICSIDL:** Input Capture Module Stop in Idle Control bit
 1 = Input capture module will halt in CPU Idle mode
 0 = Input capture module will continue to operate in CPU Idle mode

bit 12-8 **Unimplemented:** Read as '0'

bit 7 **ICTMR:** Input Capture Timer Select bits
 1 = TMR2 contents are captured on capture event
 0 = TMR3 contents are captured on capture event

bit 6-5 **ICI<1:0>:** Select Number of Captures per Interrupt bits
 11 = Interrupt on every fourth capture event
 10 = Interrupt on every third capture event
 01 = Interrupt on every second capture event
 00 = Interrupt on every capture event

bit 4 **ICOV:** Input Capture Overflow Status Flag bit (read-only)
 1 = Input capture overflow occurred
 0 = No input capture overflow occurred

bit 3 **ICBNE:** Input Capture Buffer Empty Status bit (read-only)
 1 = Input capture buffer is not empty, at least one more capture value can be read
 0 = Input capture buffer is empty

bit 2-0 **ICM<2:0>:** Input Capture Mode Select bits
 111 = Input capture functions as interrupt pin only when device is in Sleep or Idle mode
 (Rising edge detect only, all other control bits are not applicable.)
 110 = Unused (module disabled)
 101 = Capture mode, every 16th rising edge
 100 = Capture mode, every 4th rising edge
 011 = Capture mode, every rising edge
 010 = Capture mode, every falling edge
 001 = Capture mode, every edge (rising and falling)
 (ICI<1:0> bits do not control interrupt generation for this mode.)
 000 = Input capture module turned off

14.1 Output Compare Modes

Configure the Output Compare modes by setting the appropriate Output Compare Mode (OCM<2:0>) bits in the Output Compare Control (OCxCON<2:0>) register. Table 14-1 lists the different bit settings for the Output Compare modes. Figure 14-2 illustrates the output compare operation for various modes. The user application must disable the associated timer when writing to the output compare control registers to avoid malfunctions.

Note: See **Section 13. “Output Compare”** in the “*dsPIC33F/PIC24H Family Reference Manual*” (DS70209) for OCxR and OCxRS register restrictions.

TABLE 14-1: OUTPUT COMPARE MODES

OCM<2:0>	Mode	OCx Pin Initial State	OCx Interrupt Generation
000	Module Disabled	Controlled by GPIO register	—
001	Active-Low One-Shot	0	OCx Rising edge
010	Active-High One-Shot	1	OCx Falling edge
011	Toggle Mode	Current output is maintained	OCx Rising and Falling edge
100	Delayed One-Shot	0	OCx Falling edge
101	Continuous Pulse mode	0	OCx Falling edge
110	PWM mode without fault protection	0, if OCxR is zero 1, if OCxR is non-zero	No interrupt
111	PWM mode with fault protection	0, if OCxR is zero 1, if OCxR is non-zero	OCFA Falling edge for OC1 to OC4

REGISTER 18-1: I2CxCON: I2Cx CONTROL REGISTER

R/W-0	U-0	R/W-0	R/W-1 HC	R/W-0	R/W-0	R/W-0	R/W-0
I2CEN	—	I2CSIDL	SCLREL	IPMIEN	A10M	DISSLW	SMEN
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0 HC	R/W-0 HC	R/W-0 HC	R/W-0 HC	R/W-0 HC
GCEN	STREN	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN
bit 7							bit 0

Legend:	U = Unimplemented bit, read as '0'		
R = Readable bit	W = Writable bit	HS = Set in hardware	HC = Cleared in hardware
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

- bit 15 **I2CEN:** I2Cx Enable bit
1 = Enables the I2Cx module and configures the SDAx and SCLx pins as serial port pins
0 = Disables the I2Cx module. All I²C pins are controlled by port functions.
- bit 14 **Unimplemented:** Read as '0'
- bit 13 **I2CSIDL:** Stop in Idle Mode bit
1 = Discontinue module operation when device enters an Idle mode
0 = Continue module operation in Idle mode
- bit 12 **SCLREL:** SCLx Release Control bit (when operating as I²C slave)
1 = Release SCLx clock
0 = Hold SCLx clock low (clock stretch)
If STREN = 1:
Bit is R/W (i.e., software can write '0' to initiate stretch and write '1' to release clock). Hardware clear at beginning of slave transmission. Hardware clear at end of slave reception.
If STREN = 0:
Bit is R/S (i.e., software can only write '1' to release clock). Hardware clear at beginning of slave transmission.
- bit 11 **IPMIEN:** Intelligent Peripheral Management Interface (IPMI) Enable bit
1 = IPMI mode is enabled; all addresses Acknowledged
0 = IPMI mode disabled
- bit 10 **A10M:** 10-bit Slave Address bit
1 = I2CxADD is a 10-bit slave address
0 = I2CxADD is a 7-bit slave address
- bit 9 **DISSLW:** Disable Slew Rate Control bit
1 = Slew rate control disabled
0 = Slew rate control enabled
- bit 8 **SMEN:** SMBus Input Levels bit
1 = Enable I/O pin thresholds compliant with SMBus specification
0 = Disable SMBus input thresholds
- bit 7 **GCEN:** General Call Enable bit (when operating as I²C slave)
1 = Enable interrupt when a general call address is received in the I2CxRSR (module is enabled for reception)
0 = General call address disabled
- bit 6 **STREN:** SCLx Clock Stretch Enable bit (when operating as I²C slave)
Used in conjunction with SCLREL bit.
1 = Enable software or receive clock stretching
0 = Disable software or receive clock stretching

REGISTER 18-2: I2CxSTAT: I2Cx STATUS REGISTER (CONTINUED)

- bit 3 **S:** Start bit
1 = Indicates that a Start (or Repeated Start) bit has been detected last
0 = Start bit was not detected last
Hardware set or clear when Start, Repeated Start or Stop detected.
- bit 2 **R_W:** Read/Write Information bit (when operating as I²C slave)
1 = Read – indicates data transfer is output from slave
0 = Write – indicates data transfer is input to slave
Hardware set or clear after reception of I²C device address byte.
- bit 1 **RBF:** Receive Buffer Full Status bit
1 = Receive complete, I2CxRCV is full
0 = Receive not complete, I2CxRCV is empty
Hardware set when I2CxRCV is written with received byte. Hardware clear when software reads I2CxRCV.
- bit 0 **TBF:** Transmit Buffer Full Status bit
1 = Transmit in progress, I2CxTRN is full
0 = Transmit complete, I2CxTRN is empty
Hardware set when software writes I2CxTRN. Hardware clear at completion of data transmission.

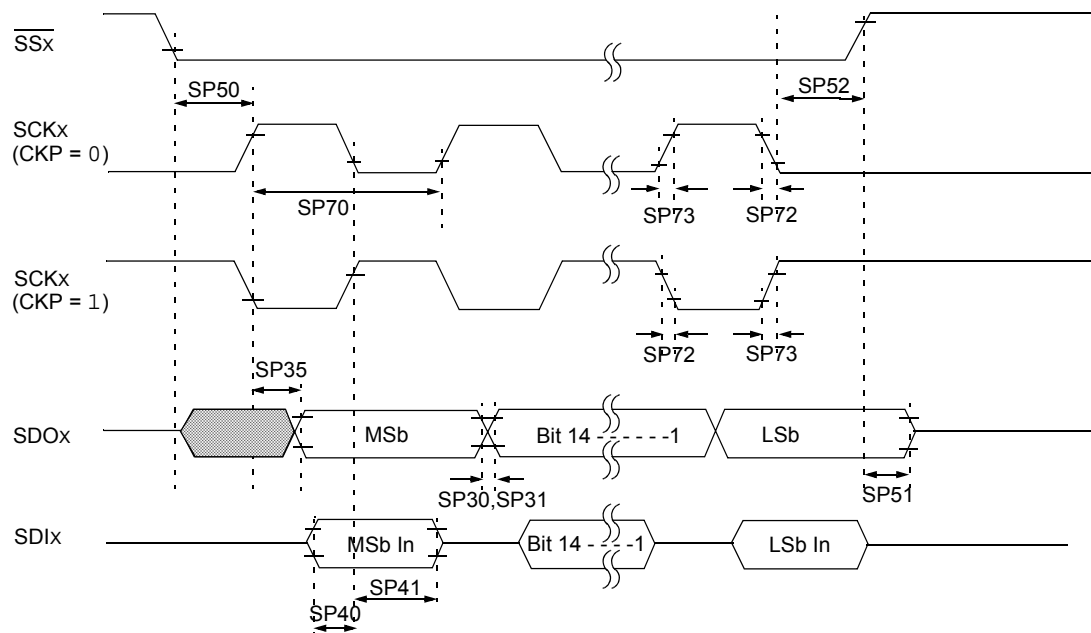
dsPIC33FJ12MC201/202

TABLE 22-2: INSTRUCTION SET OVERVIEW

Base Instr #	Assembly Mnemonic	Assembly Syntax	Description	# of Words	# of Cycles	Status Flags Affected
1	ADD	ADD <i>Acc</i>	Add Accumulators	1	1	OA,OB,SA,SB
		ADD <i>f</i>	$f = f + \text{WREG}$	1	1	C,DC,N,OV,Z
		ADD <i>f</i> , <i>WREG</i>	$\text{WREG} = f + \text{WREG}$	1	1	C,DC,N,OV,Z
		ADD #lit10, <i>Wn</i>	$\text{Wd} = \text{lit10} + \text{Wd}$	1	1	C,DC,N,OV,Z
		ADD <i>Wb</i> , <i>Ws</i> , <i>Wd</i>	$\text{Wd} = \text{Wb} + \text{Ws}$	1	1	C,DC,N,OV,Z
		ADD <i>Wb</i> , #lit5, <i>Wd</i>	$\text{Wd} = \text{Wb} + \text{lit5}$	1	1	C,DC,N,OV,Z
		ADD <i>Wso</i> , #Slit4, <i>Acc</i>	16-bit Signed Add to Accumulator	1	1	OA,OB,SA,SB
2	ADDC	ADDC <i>f</i>	$f = f + \text{WREG} + (\text{C})$	1	1	C,DC,N,OV,Z
		ADDC <i>f</i> , <i>WREG</i>	$\text{WREG} = f + \text{WREG} + (\text{C})$	1	1	C,DC,N,OV,Z
		ADDC #lit10, <i>Wn</i>	$\text{Wd} = \text{lit10} + \text{Wd} + (\text{C})$	1	1	C,DC,N,OV,Z
		ADDC <i>Wb</i> , <i>Ws</i> , <i>Wd</i>	$\text{Wd} = \text{Wb} + \text{Ws} + (\text{C})$	1	1	C,DC,N,OV,Z
		ADDC <i>Wb</i> , #lit5, <i>Wd</i>	$\text{Wd} = \text{Wb} + \text{lit5} + (\text{C})$	1	1	C,DC,N,OV,Z
3	AND	AND <i>f</i>	$f = f \text{ .AND. } \text{WREG}$	1	1	N,Z
		AND <i>f</i> , <i>WREG</i>	$\text{WREG} = f \text{ .AND. } \text{WREG}$	1	1	N,Z
		AND #lit10, <i>Wn</i>	$\text{Wd} = \text{lit10} \text{ .AND. } \text{Wd}$	1	1	N,Z
		AND <i>Wb</i> , <i>Ws</i> , <i>Wd</i>	$\text{Wd} = \text{Wb} \text{ .AND. } \text{Ws}$	1	1	N,Z
		AND <i>Wb</i> , #lit5, <i>Wd</i>	$\text{Wd} = \text{Wb} \text{ .AND. } \text{lit5}$	1	1	N,Z
4	ASR	ASR <i>f</i>	$f = \text{Arithmetic Right Shift } f$	1	1	C,N,OV,Z
		ASR <i>f</i> , <i>WREG</i>	$\text{WREG} = \text{Arithmetic Right Shift } f$	1	1	C,N,OV,Z
		ASR <i>Ws</i> , <i>Wd</i>	$\text{Wd} = \text{Arithmetic Right Shift } \text{Ws}$	1	1	C,N,OV,Z
		ASR <i>Wb</i> , <i>Wns</i> , <i>Wnd</i>	$\text{Wnd} = \text{Arithmetic Right Shift } \text{Wb} \text{ by } \text{Wns}$	1	1	N,Z
		ASR <i>Wb</i> , #lit5, <i>Wnd</i>	$\text{Wnd} = \text{Arithmetic Right Shift } \text{Wb} \text{ by } \text{lit5}$	1	1	N,Z
5	BCLR	BCLR <i>f</i> , #bit4	Bit Clear <i>f</i>	1	1	None
		BCLR <i>Ws</i> , #bit4	Bit Clear <i>Ws</i>	1	1	None
6	BRA	BRA <i>C</i> , <i>Expr</i>	Branch if Carry	1	1 (2)	None
		BRA <i>GE</i> , <i>Expr</i>	Branch if greater than or equal	1	1 (2)	None
		BRA <i>GEU</i> , <i>Expr</i>	Branch if unsigned greater than or equal	1	1 (2)	None
		BRA <i>GT</i> , <i>Expr</i>	Branch if greater than	1	1 (2)	None
		BRA <i>GTU</i> , <i>Expr</i>	Branch if unsigned greater than	1	1 (2)	None
		BRA <i>LE</i> , <i>Expr</i>	Branch if less than or equal	1	1 (2)	None
		BRA <i>LEU</i> , <i>Expr</i>	Branch if unsigned less than or equal	1	1 (2)	None
		BRA <i>LT</i> , <i>Expr</i>	Branch if less than	1	1 (2)	None
		BRA <i>LTU</i> , <i>Expr</i>	Branch if unsigned less than	1	1 (2)	None
		BRA <i>N</i> , <i>Expr</i>	Branch if Negative	1	1 (2)	None
		BRA <i>NC</i> , <i>Expr</i>	Branch if Not Carry	1	1 (2)	None
		BRA <i>NN</i> , <i>Expr</i>	Branch if Not Negative	1	1 (2)	None
		BRA <i>NOV</i> , <i>Expr</i>	Branch if Not Overflow	1	1 (2)	None
		BRA <i>NZ</i> , <i>Expr</i>	Branch if Not Zero	1	1 (2)	None
		BRA <i>OA</i> , <i>Expr</i>	Branch if Accumulator A overflow	1	1 (2)	None
		BRA <i>OB</i> , <i>Expr</i>	Branch if Accumulator B overflow	1	1 (2)	None
		BRA <i>OV</i> , <i>Expr</i>	Branch if Overflow	1	1 (2)	None
		BRA <i>SA</i> , <i>Expr</i>	Branch if Accumulator A saturated	1	1 (2)	None
		BRA <i>SB</i> , <i>Expr</i>	Branch if Accumulator B saturated	1	1 (2)	None
		BRA <i>Expr</i>	Branch Unconditionally	1	2	None
		BRA <i>Z</i> , <i>Expr</i>	Branch if Zero	1	1 (2)	None
		BRA <i>Wn</i>	Computed Branch	1	2	None
7	BSET	BSET <i>f</i> , #bit4	Bit Set <i>f</i>	1	1	None
		BSET <i>Ws</i> , #bit4	Bit Set <i>Ws</i>	1	1	None
8	BSW	BSW.C <i>Ws</i> , <i>Wb</i>	Write C bit to <i>Ws</i> < <i>Wb</i> >	1	1	None
		BSW.Z <i>Ws</i> , <i>Wb</i>	Write Z bit to <i>Ws</i> < <i>Wb</i> >	1	1	None
9	BTG	BTG <i>f</i> , #bit4	Bit Toggle <i>f</i>	1	1	None
		BTG <i>Ws</i> , #bit4	Bit Toggle <i>Ws</i>	1	1	None

dsPIC33FJ12MC201/202

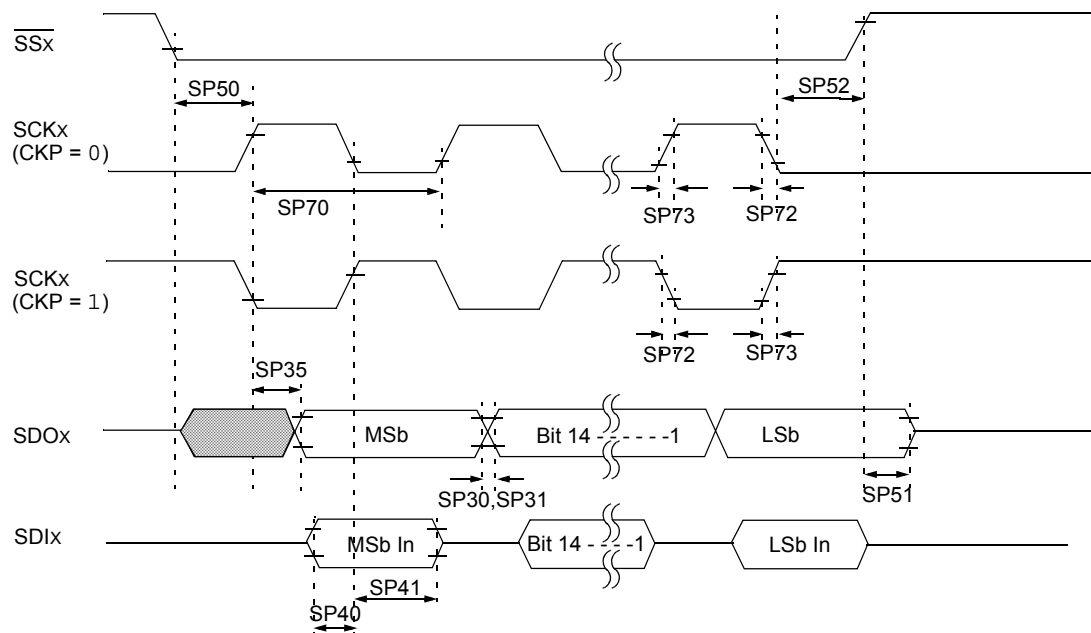
FIGURE 24-20: SPIx SLAVE MODE (FULL-DUPLEX CKE = 0, CKP = 1, SMP = 0) TIMING CHARACTERISTICS



Note: Refer to Figure 24-1 for load conditions.

dsPIC33FJ12MC201/202

FIGURE 24-21: SPIx SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 0, SMP = 0) TIMING CHARACTERISTICS



Note: Refer to Figure 24-1 for load conditions.

TABLE 24-40: I2Cx BUS DATA TIMING REQUIREMENTS (MASTER MODE)

AC CHARACTERISTICS				Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended			
Param No.	Symbol	Characteristic ⁽³⁾		Min ⁽¹⁾	Max	Units	Conditions
IM10	TLO:SCL	Clock Low Time	100 kHz mode	$T_{CY}/2 (BRG + 1)$	—	μs	—
			400 kHz mode	$T_{CY}/2 (BRG + 1)$	—	μs	—
			1 MHz mode ⁽²⁾	$T_{CY}/2 (BRG + 1)$	—	μs	—
IM11	THI:SCL	Clock High Time	100 kHz mode	$T_{CY}/2 (BRG + 1)$	—	μs	—
			400 kHz mode	$T_{CY}/2 (BRG + 1)$	—	μs	—
			1 MHz mode ⁽²⁾	$T_{CY}/2 (BRG + 1)$	—	μs	—
IM20	TF:SCL	SDAx and SCLx Fall Time	100 kHz mode	—	300	ns	Cb is specified to be from 10 to 400 pF
			400 kHz mode	$20 + 0.1 C_B$	300	ns	
			1 MHz mode ⁽²⁾	—	100	ns	
IM21	TR:SCL	SDAx and SCLx Rise Time	100 kHz mode	—	1000	ns	Cb is specified to be from 10 to 400 pF
			400 kHz mode	$20 + 0.1 C_B$	300	ns	
			1 MHz mode ⁽²⁾	—	300	ns	
IM25	TSU:DAT	Data Input Setup Time	100 kHz mode	250	—	ns	—
			400 kHz mode	100	—	ns	
			1 MHz mode ⁽²⁾	40	—	ns	
IM26	THD:DAT	Data Input Hold Time	100 kHz mode	0	—	μs	—
			400 kHz mode	0	0.9	μs	
			1 MHz mode ⁽²⁾	0.2	—	μs	
IM30	TSU:STA	Start Condition Setup Time	100 kHz mode	$T_{CY}/2 (BRG + 1)$	—	μs	Only relevant for Repeated Start condition
			400 kHz mode	$T_{CY}/2 (BRG + 1)$	—	μs	
			1 MHz mode ⁽²⁾	$T_{CY}/2 (BRG + 1)$	—	μs	
IM31	THD:STA	Start Condition Hold Time	100 kHz mode	$T_{CY}/2 (BRG + 1)$	—	μs	After this period the first clock pulse is generated
			400 kHz mode	$T_{CY}/2 (BRG + 1)$	—	μs	
			1 MHz mode ⁽²⁾	$T_{CY}/2 (BRG + 1)$	—	μs	
IM33	TSU:STO	Stop Condition Setup Time	100 kHz mode	$T_{CY}/2 (BRG + 1)$	—	μs	—
			400 kHz mode	$T_{CY}/2 (BRG + 1)$	—	μs	
			1 MHz mode ⁽²⁾	$T_{CY}/2 (BRG + 1)$	—	μs	
IM34	THD:STO	Stop Condition Hold Time	100 kHz mode	$T_{CY}/2 (BRG + 1)$	—	ns	—
			400 kHz mode	$T_{CY}/2 (BRG + 1)$	—	ns	
			1 MHz mode ⁽²⁾	$T_{CY}/2 (BRG + 1)$	—	ns	
IM40	TAA:SCL	Output Valid From Clock	100 kHz mode	—	3500	ns	—
			400 kHz mode	—	1000	ns	—
			1 MHz mode ⁽²⁾	—	400	ns	—
IM45	TBF:SDA	Bus Free Time	100 kHz mode	4.7	—	μs	Time the bus must be free before a new transmission can start
			400 kHz mode	1.3	—	μs	
			1 MHz mode ⁽²⁾	0.5	—	μs	
IM50	CB	Bus Capacitive Loading		—	400	pF	—
IM51	PGD	Pulse Gobbler Delay		65	390	ns	See Note 4

Note 1: BRG is the value of the I²C Baud Rate Generator. Refer to **Section 19. “Inter-Integrated Circuit (I²C™)”** (DS70195) in the “dsPIC33F/PIC24H Family Reference Manual”. Please see the Microchip web site (www.microchip.com) for the latest family reference manual sections.

2: Maximum pin capacitance = 10 pF for all I2Cx pins (for 1 MHz mode only).

3: These parameters are characterized by similarity, but are not tested in manufacturing.

4: Typical value for this parameter is 130 ns.

FIGURE 24-24: I2Cx BUS START/STOP BITS TIMING CHARACTERISTICS (SLAVE MODE)

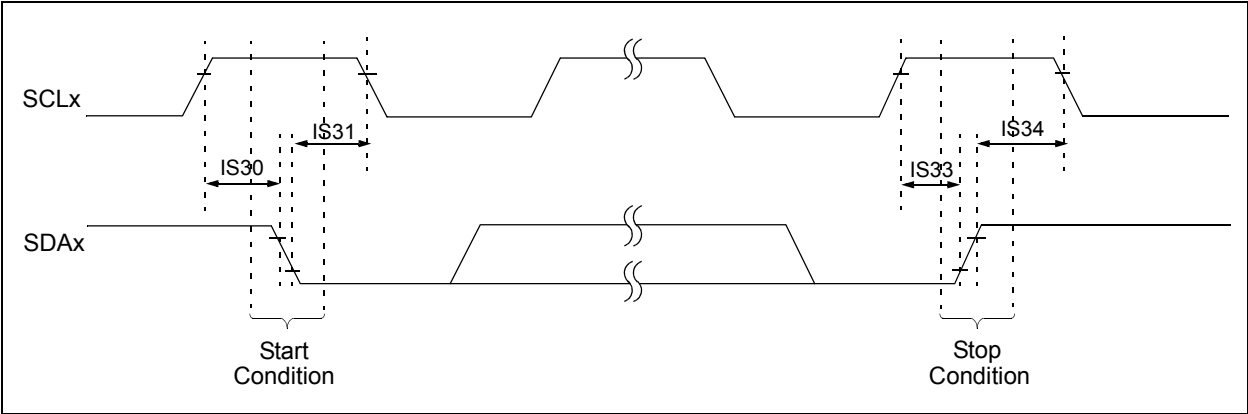


FIGURE 24-25: I2Cx BUS DATA TIMING CHARACTERISTICS (SLAVE MODE)

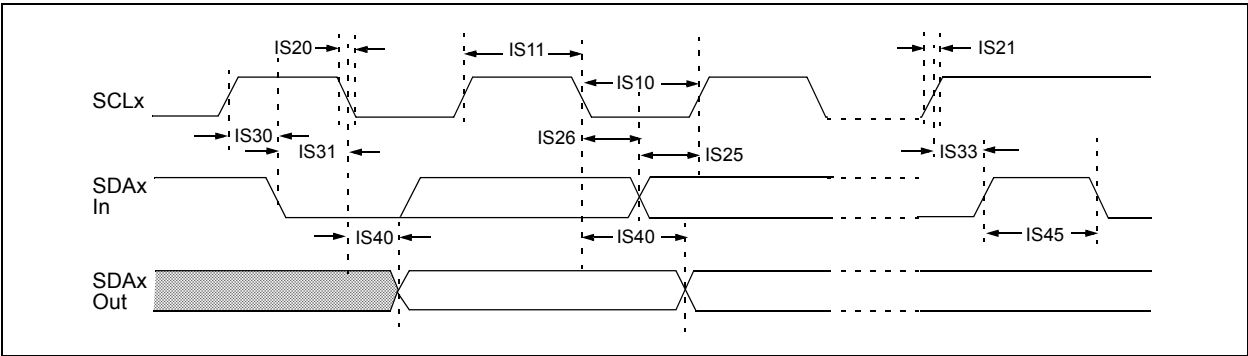


TABLE 24-46: ADC CONVERSION (10-BIT MODE) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	Symbol	Characteristic	Min.	Typ ⁽¹⁾	Max.	Units	Conditions
Clock Parameters⁽²⁾							
AD50	TAD	ADC Clock Period	76	—	—	ns	—
AD51	tRC	ADC Internal RC Oscillator Period	—	250	—	ns	—
Conversion Rate							
AD55	tCONV	Conversion Time	—	12 TAD	—	—	—
AD56	FCNV	Throughput Rate	—	—	1.1	Msp/s	—
AD57	TsAMP	Sample Time	2.0 TAD	—	—	—	—
Timing Parameters							
AD60	tPCS	Conversion Start from Sample Trigger ⁽¹⁾	2.0 TAD	—	3.0 TAD	—	Auto-Convert Trigger (SSRC<2:0> = 111) not selected
AD61	tPSS	Sample Start from Setting Sample (SAMP) bit ⁽¹⁾	2.0 TAD	—	3.0 TAD	—	—
AD62	tCSS	Conversion Completion to Sample Start (ASAM = 1) ⁽¹⁾	—	0.5 TAD	—	—	—
AD63	tDPU	Time to Stabilize Analog Stage from ADC Off to ADC On ⁽¹⁾	—	—	20	μs	—

Note 1: These parameters are characterized but not tested in manufacturing.

2: Because the sample caps will eventually lose charge, clock rates below 10 kHz may affect linearity performance, especially at elevated temperatures.

TABLE 25-1: MAJOR SECTION UPDATES

Section Name	Update Description
Section 19.0 “10-bit/12-bit Analog-to-Digital Converter (ADC)”	<p>Updated ADC Conversion Clock Select bits in the AD1CON3 register from ADCS<5:0> to ADCS<7:0>. Any references to these bits have also been updated throughout this data sheet (Register 19-3).</p> <p>Replaced Figure 19-1 (ADC1 Module Block Diagram for dsPIC33FJ12MC201) and added Figure 19-2 (ADC1 Block Diagram for dsPIC33FJ12MC202).</p> <p>Removed Equation 19-1: ADC Conversion Clock Period and Figure 19-2: ADC Transfer Function (10-Bit Example).</p> <p>Added Note 2 to Figure 19-2: ADC Conversion Clock Period Block Diagram.</p> <p>Updated ADC1 Input Channel 1, 2, 3 Select Register (see Register 19-4) as follows:</p> <ul style="list-style-type: none"> • Changed bit 10-9 (CH123NB - dsPIC33FJ12MC201 devices only) description for bit value of 10 (if AD12B = 0). • Updated bit 8 (CH123SB) to reflect device-specific information. • Updated bit 0 (CH123SA) to reflect device-specific information. • Changed bit 2-1 (CH123NA - dsPIC33FJ12MC201 devices only) description for bit value of 10 (if AD12B = 0). <p>Updated ADC1 Input Channel 0 Select Register (see Register 19-5) as follows:</p> <ul style="list-style-type: none"> • Changed bit value descriptions for bits 12-8 • Changed bit value descriptions for bits 4-0 (dsPIC33FJ12MC201 devices) <p>Modified Notes 1 and 2 in the ADC1 Input Scan Select Register Low (see Register 19-6)</p> <p>Modified Notes 1 and 2 in the ADC1 Port Configuration Register Low (see Register 19-7)</p>
Section 20.0 “Special Features”	<p>Added FICD register information for address 0xF8000E in the Device Configuration Register Map (see Table 20-1).</p> <p>Added FICD register content (BKBUG, COE, JTAGEN, and ICS<1:0> to the dsPIC33FJ12MC201/202 Configuration Bits Description (see Table 20-2).</p> <p>Added a note regarding the placement of low-ESR capacitors, after the second paragraph of Section 20.2 “On-Chip Voltage Regulator” and to Figure 20-2.</p> <p>Removed the words “if enabled” from the second sentence in the fifth paragraph of Section 20.3 “BOR: Brown-out Reset”</p>

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