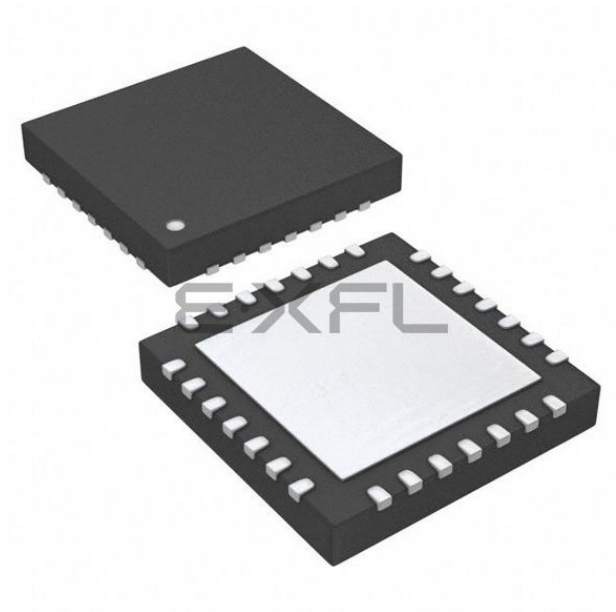


**Welcome to E-XFL.COM**

## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

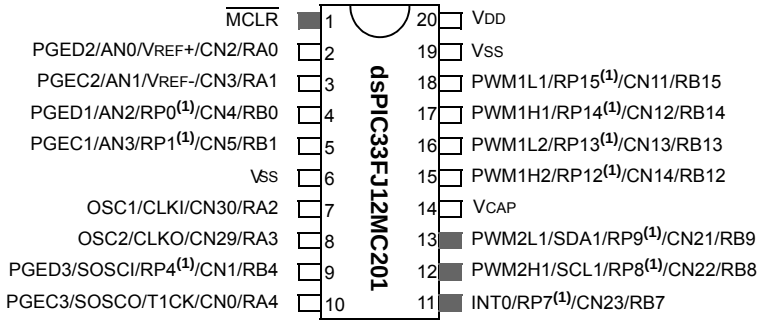
## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | dsPIC |
| Core Size | 16-Bit |
| Speed | 40 MIPs |
| Connectivity | I²C, IrDA, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, Motor Control PWM, QEI, POR, PWM, WDT |
| Number of I/O | 21 |
| Program Memory Size | 12KB (12K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 1K x 8 |
| Voltage - Supply (Vcc/Vdd) | 3V ~ 3.6V |
| Data Converters | A/D 6x10b/12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 28-VQFN Exposed Pad |
| Supplier Device Package | 28-QFN (6x6) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/dspic33fj12mc202-i-ml |

## Pin Diagrams

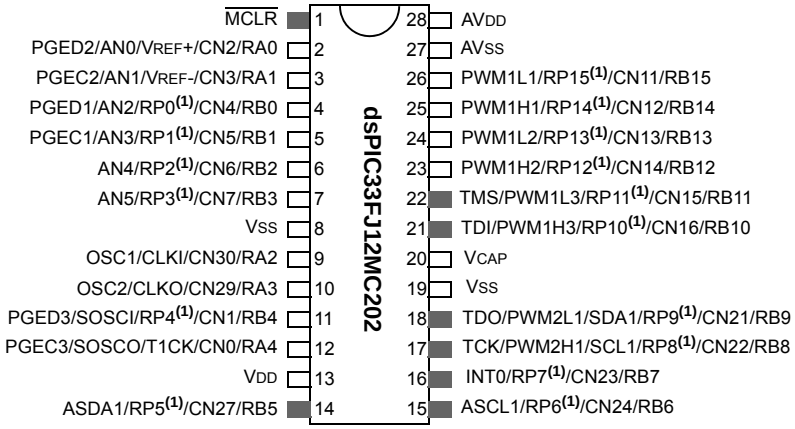
### 20-PIN PDIP, SOIC, SSOP

■ = Pins are up to 5V tolerant




### 28-PIN SPDIP, SOIC, SSOP

■ = Pins are up to 5V tolerant




**Note 1:** The RPn pins can be used by any remappable peripheral. See Table 1 for the list of available peripherals.


© 2007-2011 Microchip Technology Inc.

## Table of Contents



### TO OUR VALUED CUSTOMERS

It is our intention to provide our valued customers with the best documentation possible to ensure successful use of your Microchip products. To this end, we will continue to improve our publications to better suit your needs. Our publications will be refined and enhanced as new volumes and updates are introduced.

If you have any questions or comments regarding this publication, please contact the Marketing Communications Department via E-mail at **docerrors@microchip.com** or fax the **Reader Response Form** in the back of this data sheet to (480) 792-4150. We welcome your feedback.

#### Most Current Data Sheet

To obtain the most up-to-date version of this data sheet, please register at our Worldwide Web site at:

**http://www.microchip.com**

You can determine the version of a data sheet by examining its literature number found on the bottom outside corner of any page. The last character of the literature number is the version number, (e.g., DS30000A is version A of document DS30000).

#### Errata

An errata sheet, describing minor operational differences from the data sheet and recommended workarounds, may exist for current devices. As device/documentation issues become known to us, we will publish an errata sheet. The errata will specify the revision of silicon and revision of document to which it applies.

To determine if an errata sheet exists for a particular device, please check with one of the following:

- Microchip's Worldwide Web site; **http://www.microchip.com**
- Your local Microchip sales office (see last page)

When contacting a sales office, please specify which device, revision of silicon and data sheet (include literature number) you are using.

#### Customer Notification System

Register on our web site at **www.microchip.com** to receive the most current information on all of our products.


© 2007-2011 Microchip Technology Inc.

**REGISTER 7-17: IPC4: INTERRUPT PRIORITY CONTROL REGISTER 4**

| U-0 | R/W-1 | R/W-0 | R/W-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | CNIP<2:0> | | | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| U-0 | R/W-1 | R/W-0 | R/W-0 | U-0 | R/W-1 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | MI2C1IP<2:0> | | | — | SI2C1IP<2:0> | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **Unimplemented:** Read as '0'

bit 14-12 **CNIP<2:0>:** Change Notification Interrupt Priority bits
111 = Interrupt is priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is priority 1
000 = Interrupt source is disabled

bit 11-7 **Unimplemented:** Read as '0'

bit 6-4 **MI2C1IP<2:0>:** I2C1 Master Events Interrupt Priority bits
111 = Interrupt is priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is priority 1
000 = Interrupt source is disabled

bit 3 **Unimplemented:** Read as '0'

bit 2-0 **SI2C1IP<2:0>:** I2C1 Slave Events Interrupt Priority bits
111 = Interrupt is priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is priority 1
000 = Interrupt source is disabled


© 2007-2011 Microchip Technology Inc.

**REGISTER 8-1: OSCCON: OSCILLATOR CONTROL REGISTER(1,3) (CONTINUED)**

bit 3 **CF:** Clock Fail Detect bit (read/clear by application)
1 = FSCM has detected clock failure
0 = FSCM has not detected clock failure

bit 2 **Unimplemented:** Read as '0'

bit 1 **LPOSCEN:** Secondary (LP) Oscillator Enable bit
1 = Enable secondary oscillator
0 = Disable secondary oscillator

bit 0 **OSWEN:** Oscillator Switch Enable bit
1 = Request oscillator switch to selection specified by NOSC<2:0> bits
0 = Oscillator switch is complete

**Note 1:** Writes to this register require an unlock sequence. Refer to **Section 7. "Oscillator"** (DS70186) in the *"dsPIC33F/PIC24H Family Reference Manual"* (available from the Microchip web site) for details.

**2:** Direct clock switches between any primary oscillator mode with PLL and FRCPLL mode are not permitted. This applies to clock switches in either direction. In these instances, the application must switch to FRC mode as a transition clock source between the two PLL modes.

**3:** This register is reset only on a Power-on Reset (POR).


© 2007-2011 Microchip Technology Inc.

## 10.0 I/O PORTS

**Note 1:** This data sheet summarizes the features of the dsPIC33FJ12MC201/202 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 10. "I/O Ports"** (DS70193) of the *"dsPIC33F/PIC24H Family Reference Manual"*, which is available from the Microchip website (www.microchip.com).

**2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

All of the device pins (except VDD, VSS, $\overline{\text{MCLR}}$, and OSC1/CLKI) are shared among the peripherals and the parallel I/O ports. All I/O input ports feature Schmitt Trigger inputs for improved noise immunity.

### 10.1 Parallel I/O (PIO) Ports

Generally a parallel I/O port that shares a pin with a peripheral is subservient to the peripheral. The peripheral's output buffer data and control signals are provided to a pair of multiplexers. The multiplexers select whether the peripheral or the associated port has ownership of the output data and control signals of the I/O pin. The logic also prevents "loop through," in which a port's digital output can drive the input of a peripheral that shares the same pin. Figure 10-1 shows how ports are shared with other peripherals and the associated I/O pin to which they are connected.

When a peripheral is enabled and the peripheral is actively driving an associated pin, the use of the pin as a general purpose output pin is disabled. The I/O pin can be read, but the output driver for the parallel port bit is disabled. If a peripheral is enabled, but the peripheral is not actively driving a pin, that pin can be driven by a port.

All port pins have three registers directly associated with their operation as digital I/O. The data direction register (TRISx) determines whether the pin is an input or an output. If the data direction bit is a '1', the pin is an input. All port pins are defined as inputs after a Reset. Reads from the latch (LATx) read the latch. Writes to the latch write the latch. Reads from the port (PORTx) read the port pins, while writes to the port pins write the latch.

Any bit and its associated data and control registers that are not valid for a particular device will be disabled. This means the corresponding LATx and TRISx registers and the port pin will read as zeros.

When a pin is shared with another peripheral or function that is defined as an input only, it is nevertheless regarded as a dedicated port because there is no other competing source of outputs.

**FIGURE 10-1: BLOCK DIAGRAM OF A TYPICAL SHARED PORT STRUCTURE**

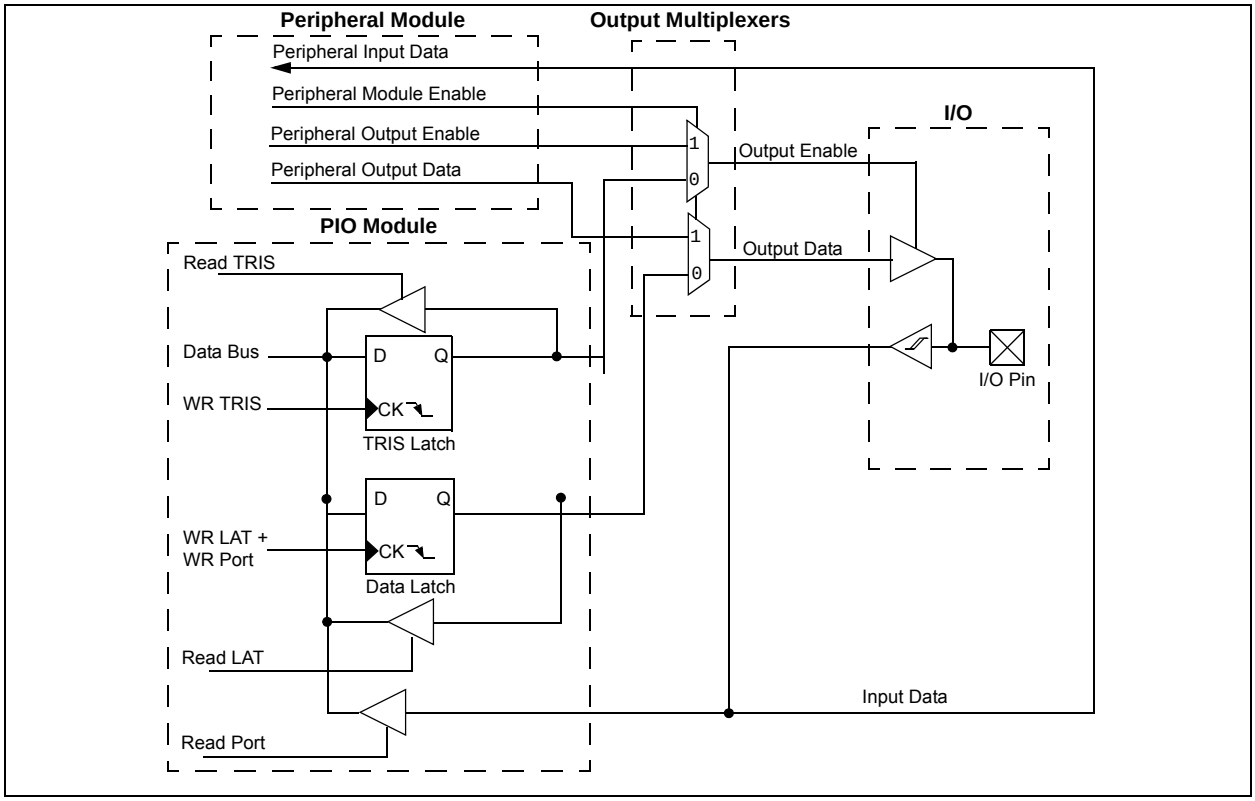


**TABLE 10-1: SELECTABLE INPUT SOURCES (MAPS INPUT TO FUNCTION)(1)**

| Input Name | Function Name | Register | Configuration Bits |
|---|---|---|---|
| External Interrupt 1 | INT1 | RPINR0 | INT1R<4:0> |
| External Interrupt 2 | INT2 | RPINR1 | INT2R<4:0> |
| Timer2 External Clock | T2CK | RPINR3 | T2CKR<4:0> |
| Timer3 External Clock | T3CK | RPINR3 | T3CKR<4:0> |
| Input Capture 1 | IC1 | RPINR7 | IC1R<4:0> |
| Input Capture 2 | IC2 | RPINR7 | IC2R<4:0> |
| Input Capture 7 | IC7 | RPINR10 | IC7R<4:0> |
| Input Capture 8 | IC8 | RPINR10 | IC8R<4:0> |
| Output Compare Fault A | OCFA | RPINR11 | OCFAR<4:0> |
| PWM1 Fault | $\overline{\text{FLTA1}}$ | RPINR12 | FLTA1R<4:0> |
| PWM2 Fault | $\overline{\text{FLTA2}}$ | RPINR13 | FLTA2R<4:0> |
| QEI1 Phase A | QEA | RPINR14 | QEA1R<4:0> |
| QEI1 Phase B | QEB | RPINR14 | QEB1R<4:0> |
| QEI1 Index | INDX | RPINR15 | INDX1R<4:0> |
| UART1 Receive | U1RX | RPINR18 | U1RXR<4:0> |
| UART1 Clear To Send | $\overline{\text{U1CTS}}$ | RPINR18 | U1CTSR<4:0> |
| SPI1 Data Input | SDI1 | RPINR20 | SDI1R<4:0> |
| SPI1 Clock Input | SCK1 | RPINR20 | SCK1R<4:0> |
| SPI1 Slave Select Input | $\overline{\text{SS1}}$ | RPINR21 | SS1R<4:0> |

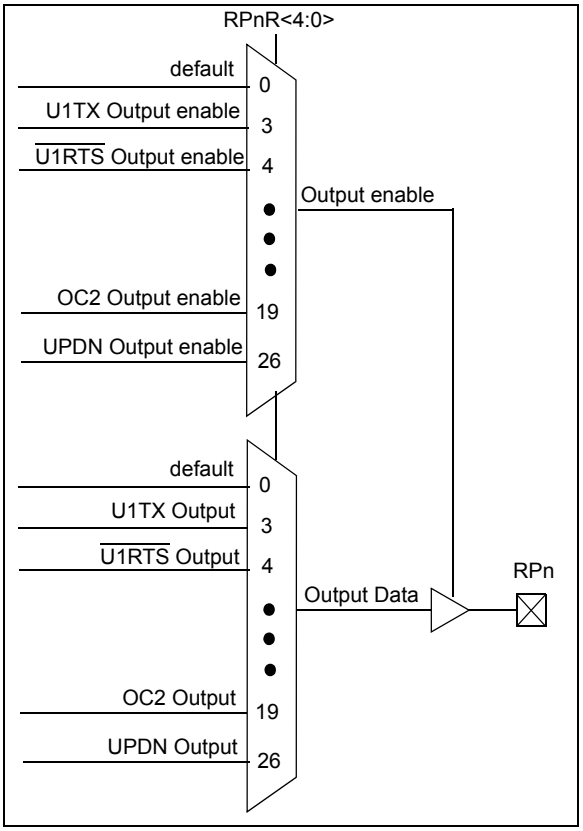
**Note 1:** Unless otherwise noted, all inputs use the Schmitt input buffers.

### 10.4.2.2 Output Mapping

In contrast to inputs, the outputs of the peripheral pin select options are mapped on the basis of the pin. In this case, a control register associated with a particular pin dictates the peripheral output to be mapped. The RPORx registers are used to control output mapping. Like the RPINRx registers, each register contains sets of 5-bit fields, with each set associated with one RPn pin (see Register 10-14 through Register 10-21). The value of the bit field corresponds to one of the peripherals, and that peripheral's output is mapped to the pin (see Table 10-2 and Figure 10-3).

The list of peripherals for output mapping also includes a null value of '00000' because of the mapping technique. This permits any given pin to remain unconnected from the output of any of the pin selectable peripherals.

**FIGURE 10-3: MULTIPLEXING OF REMAPPABLE OUTPUT FOR RPn**





© 2007-2011 Microchip Technology Inc.

**REGISTER 10-9: RPINR14: PERIPHERAL PIN SELECT INPUT REGISTER 14**

| U-0 | U-0 | U-0 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 |
|---|---|---|---|---|---|---|---|
| — | — | — | QEB1R<4:0> | | | | |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | U-0 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 |
|---|---|---|---|---|---|---|---|
| — | — | — | QEA1R<4:0> | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-13 **Unimplemented:** Read as '0'

bit 12-8 **QEB1R<4:0>:** Assign B (QEB) to the corresponding pin
11111 = Input tied Vss
01111 = Input tied to RP15
.
.
.
00001 = Input tied to RP1
00000 = Input tied to RP0

bit 7-5 **Unimplemented:** Read as '0'

bit 4-0 **QEA1R<4:0>:** Assign A (QEA) to the corresponding pin
11111 = Input tied Vss
01111 = Input tied to RP15
.
.
.
00001 = Input tied to RP1
00000 = Input tied to RP0

**REGISTER 10-10: RPINR15: PERIPHERAL PIN SELECT INPUT REGISTER 15**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | U-0 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 |
|---|---|---|---|---|---|---|---|
| — | — | — | INDX1R<4:0> | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-5 **Unimplemented:** Read as ‘0’

bit 4-0 **INDX1R<4:0>:** Assign QEI1 INDEX (INDX1) to the corresponding RPn pin

11111 = Input tied Vss
01111 = Input tied to RP15
.
.
.
00001 = Input tied to RP1
00000 = Input tied to RP0


© 2007-2011 Microchip Technology Inc.

**REGISTER 15-2: PxTMR: PWM TIMER COUNT VALUE REGISTER**

| R-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| PTDIR | PTMR<14:8> | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| PTMR<7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15 **PTDIR:** PWM Time Base Count Direction Status bit (read-only)
1 = PWM time base is counting down
0 = PWM time base is counting up

bit 14-0 **PTMR <14:0>:** PWM Time Base Register Count Value bits

**REGISTER 15-3: PxTPER: PWM TIME BASE PERIOD REGISTER**

| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | PTPER<14:8> | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| PTPER<7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15 **Unimplemented:** Read as ‘0’

bit 14-0 **PTPER<14:0>:** PWM Time Base Period Value bits

**REGISTER 15-7: PxDTCON1: DEAD-TIME CONTROL REGISTER 1**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| DTBPS<1:0> | | DTB<5:0> | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| DTAPS<1:0> | | DTA<5:0> | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-14 **DTBPS<1:0>:** Dead-Time Unit B Prescale Select bits
11 = Clock period for Dead-Time Unit B is 8 TCY
10 = Clock period for Dead-Time Unit B is 4 TCY
01 = Clock period for Dead-Time Unit B is 2 TCY
00 = Clock period for Dead-Time Unit B is TCY

bit 13-8 **DTB<5:0>:** Unsigned 6-bit Dead-Time Value for Dead-Time Unit B bits

bit 7-6 **DTAPS<1:0>:** Dead-Time Unit A Prescale Select bits
11 = Clock period for Dead-Time Unit A is 8 TCY
10 = Clock period for Dead-Time Unit A is 4 TCY
01 = Clock period for Dead-Time Unit A is 2 TCY
00 = Clock period for Dead-Time Unit A is TCY

bit 5-0 **DTA<5:0>:** Unsigned 6-bit Dead-Time Value for Dead-Time Unit A bits

**NOTES:**


© 2007-2011 Microchip Technology Inc.

**FIGURE 24-6: TIMERQ (QEI MODULE) EXTERNAL CLOCK TIMING CHARACTERISTICS**

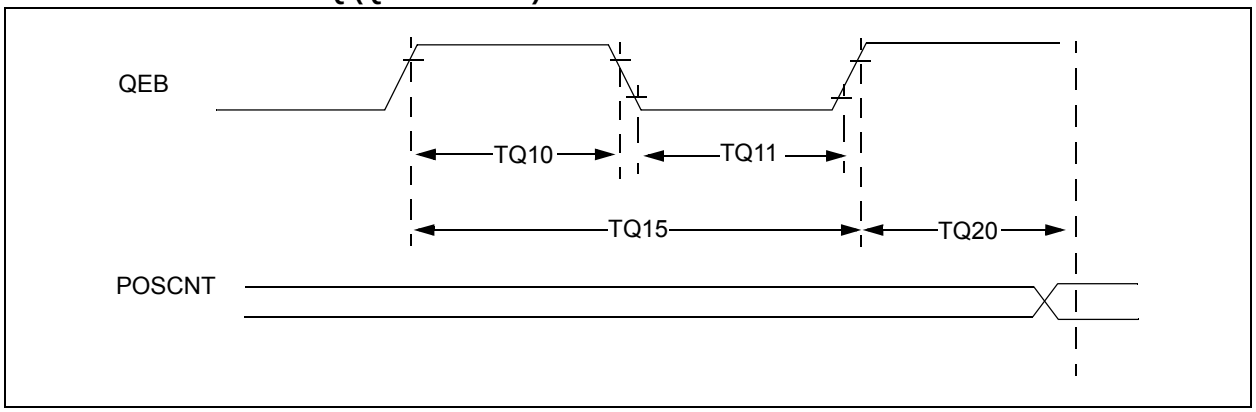
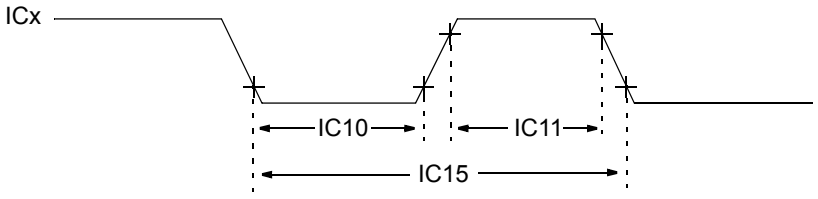



**TABLE 24-25: QEI MODULE EXTERNAL CLOCK TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic(1)** | | **Min** | **Typ** | **Max** | **Units** | **Conditions** |
| TQ10 | TtQH | TQCK High Time | Synchronous, with prescaler | TCY + 20 | | — | ns | Must also meet parameter TQ15 |
| TQ11 | TtQL | TQCK Low Time | Synchronous, with prescaler | TCY + 20 | | — | ns | Must also meet parameter TQ15 |
| TQ15 | TtQP | TQCP Input Period | Synchronous, with prescaler | 2 * TCY + 40 | | — | ns | — |
| TQ20 | TCKEXTMRL | Delay from External TxCK Clock Edge to Timer Increment | | 0.5 TCY | | 1.5 TCY | — | — |

**Note 1:** These parameters are characterized by similarity, but are not tested in manufacturing.

**FIGURE 24-7: INPUT CAPTURE (CAPx) TIMING CHARACTERISTICS**




**Note:** Refer to Figure 24-1 for load conditions.


© 2007-2011 Microchip Technology Inc.

**TABLE 24-30: QUADRATURE DECODER TIMING REQUIREMENTS**

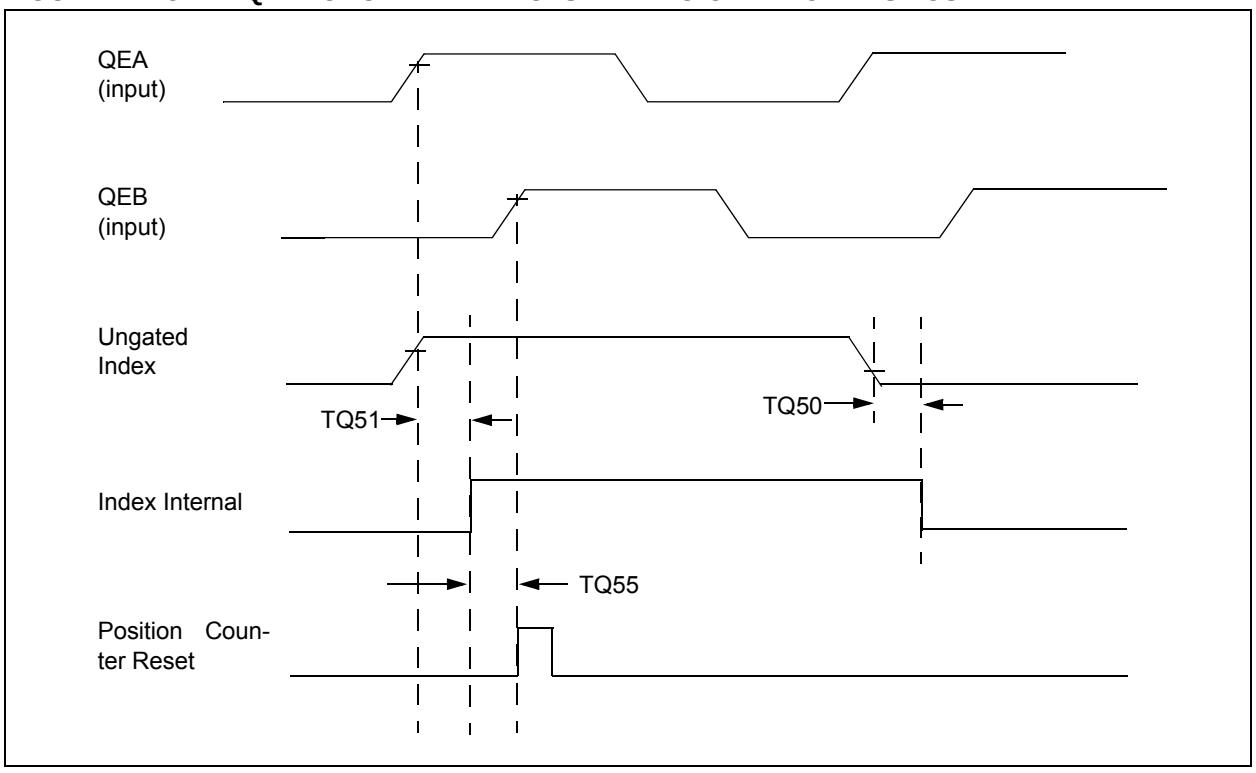
| AC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | |
|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic(1)** | **Typ(2)** | **Max** | **Units** | **Conditions** |
| TQ30 | TQUL | Quadrature Input Low Time | 6 TCY | — | ns | — |
| TQ31 | TQUH | Quadrature Input High Time | 6 TCY | — | ns | — |
| TQ35 | TQUIN | Quadrature Input Period | 12 TCY | — | ns | — |
| TQ36 | TQUP | Quadrature Phase Period | 3 TCY | — | ns | — |
| TQ40 | TQUFL | Filter Time to Recognize Low, with Digital Filter | 3 * N * TCY | — | ns | N = 1, 2, 4, 16, 32, 64, 128 and 256 **(Note 3)** |
| TQ41 | TQUFH | Filter Time to Recognize High, with Digital Filter | 3 * N * TCY | — | ns | N = 1, 2, 4, 16, 32, 64, 128 and 256 **(Note 3)** |

**Note 1:** These parameters are characterized by similarity, but are not tested in manufacturing.

**2:** Data in "Typ" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

**3:** N = Index Channel Digital Filter Clock Divide Select bits. Refer to **Section 15. "Quadrature Encoder Interface (QEI)"** (DS70208) in the *dsPIC33F/PIC24H Family Reference Manual*. Please see the Microchip (www.microchip.com) web site for the latest family reference manual chapters.

**FIGURE 24-13: QEI MODULE INDEX PULSE TIMING CHARACTERISTICS**





© 2007-2011 Microchip Technology Inc.

**TABLE 24-37: SPIx SLAVE MODE (FULL-DUPLEX, CKE = 1, CKP = 1, SMP = 0) TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤TA ≤+85°C for Industrial<br>-40°C ≤TA ≤+125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic(1)** | **Min** | **Typ(2)** | **Max** | **Units** | **Conditions** |
| SP70 | TscP | Maximum SCK Input Frequency | — | — | 11 | MHz | See **Note 3** |
| SP72 | TscF | SCKx Input Fall Time | — | — | — | ns | See parameter DO32 and **Note 4** |
| SP73 | TscR | SCKx Input Rise Time | — | — | — | ns | See parameter DO31 and **Note 4** |
| SP30 | TdoF | SDOx Data Output Fall Time | — | — | — | ns | See parameter DO32 and **Note 4** |
| SP31 | TdoR | SDOx Data Output Rise Time | — | — | — | ns | See parameter DO31 and **Note 4** |
| SP35 | TscH2doV, TscL2doV | SDOx Data Output Valid after SCKx Edge | — | 6 | 20 | ns | — |
| SP36 | TdoV2scH, TdoV2scL | SDOx Data Output Setup to First SCKx Edge | 30 | — | — | ns | — |
| SP40 | TdiV2scH, TdiV2scL | Setup Time of SDIx Data Input to SCKx Edge | 30 | — | — | ns | — |
| SP41 | TscH2diL, TscL2diL | Hold Time of SDIx Data Input to SCKx Edge | 30 | — | — | ns | — |
| SP50 | TssL2scH, TssL2scL | $\overline{SSx}$ ↓to SCKx ↑ or SCKx Input | 120 | — | — | ns | — |
| SP51 | TssH2doZ | $\overline{SSx}$ ↑ to SDOx Output High-Impedance(4) | 10 | — | 50 | ns | — |
| SP52 | TscH2ssH TscL2ssH | $\overline{SSx}$ after SCKx Edge | 1.5 TCY + 40 | — | — | ns | See **Note 4** |
| SP60 | TssL2doV | SDOx Data Output Valid after $\overline{SSx}$ Edge | — | — | 50 | ns | — |

**Note 1:** These parameters are characterized, but are not tested in manufacturing.

**2:** Data in "Typ" column is at 3.3V, 25°C unless otherwise stated.

**3:** The minimum clock period for SCKx is 91 ns. Therefore, the SCK clock generated by the Master must not violate this specification.

**4:** Assumes 50 pF load on all SPIx pins.

**TABLE 24-46: ADC CONVERSION (10-BIT MODE) TIMING REQUIREMENTS**

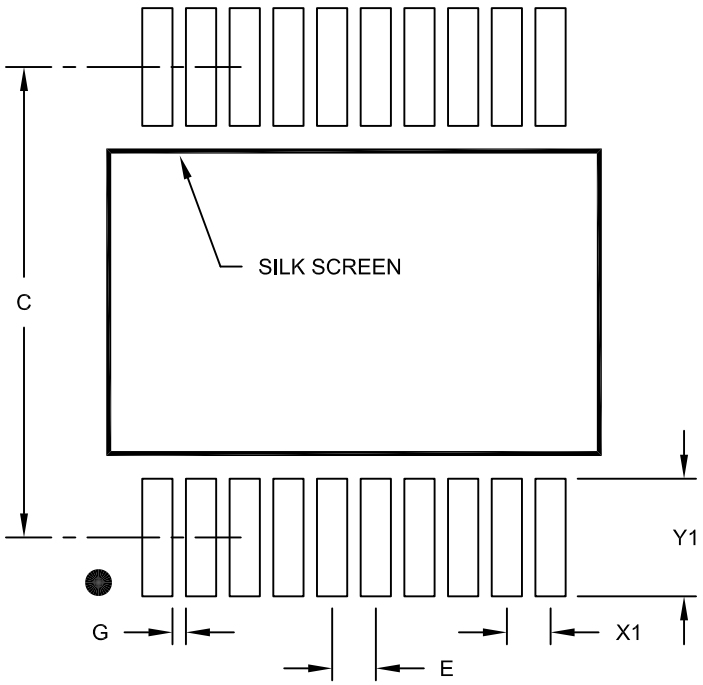
| AC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic** | **Min.** | **Typ(1)** | **Max.** | **Units** | **Conditions** |
| **Clock Parameters(2)** | | | | | | | |
| AD50 | TAD | ADC Clock Period | 76 | — | — | ns | — |
| AD51 | tRC | ADC Internal RC Oscillator Period | — | 250 | — | ns | — |
| **Conversion Rate** | | | | | | | |
| AD55 | tCONV | Conversion Time | — | 12 TAD | — | — | — |
| AD56 | FCNV | Throughput Rate | — | — | 1.1 | Msps | — |
| AD57 | TSAMP | Sample Time | 2.0 TAD | — | — | — | — |
| **Timing Parameters** | | | | | | | |
| AD60 | tPCS | Conversion Start from Sample Trigger(1) | 2.0 TAD | — | 3.0 TAD | — | Auto-Convert Trigger (SSRC<2:0> = 111) not selected |
| AD61 | tPSS | Sample Start from Setting Sample (SAMP) bit(1) | 2.0 TAD | — | 3.0 TAD | — | — |
| AD62 | tCSS | Conversion Completion to Sample Start (ASAM = 1)(1) | — | 0.5 TAD | — | — | — |
| AD63 | tDPU | Time to Stabilize Analog Stage from ADC Off to ADC On(1) | — | — | 20 | μs | — |

**Note 1:** These parameters are characterized but not tested in manufacturing.

**2:** Because the sample caps will eventually lose charge, clock rates below 10 kHz may affect linearity performance, especially at elevated temperatures.

20-Lead Plastic Shrink Small Outline (SS) - 5.30 mm Body [SSOP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E | 0.65 BSC | | |
| Contact Pad Spacing | C | | 7.20 | |
| Contact Pad Width (X20) | X1 | | | 0.45 |
| Contact Pad Length (X20) | Y1 | | | 1.75 |
| Distance Between Pads | G | 0.20 | | |

Notes:

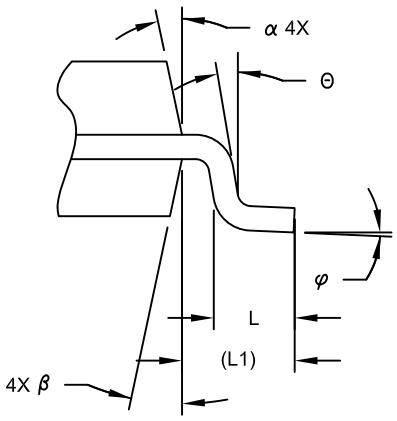
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

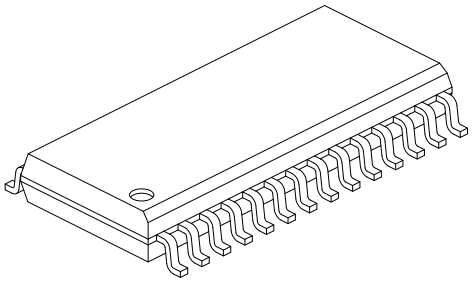
Microchip Technology Drawing No. C04-2072A

## 28-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




VIEW C



| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | | 28 | |
| Pitch | e | | 1.27 BSC | |
| Overall Height | A | - | - | 2.65 |
| Molded Package Thickness | A2 | 2.05 | - | - |
| Standoff § | A1 | 0.10 | - | 0.30 |
| Overall Width | E | | 10.30 BSC | |
| Molded Package Width | E1 | | 7.50 BSC | |
| Overall Length | D | | 17.90 BSC | |
| Chamfer (Optional) | h | 0.25 | - | 0.75 |
| Foot Length | L | 0.40 | - | 1.27 |
| Footprint | L1 | | 1.40 REF | |
| Lead Angle | Θ | 0° | - | - |
| Foot Angle | φ | 0° | - | 8° |
| Lead Thickness | c | 0.18 | - | 0.33 |
| Lead Width | b | 0.31 | - | 0.51 |
| Mold Draft Angle Top | α | 5° | - | 15° |
| Mold Draft Angle Bottom | β | 5° | - | 15° |

**Notes:**

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimension D does not include mold flash, protrusions or gate burrs, which shall not exceed 0.15 mm per end. Dimension E1 does not include interlead flash or protrusion, which shall not exceed 0.25 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M

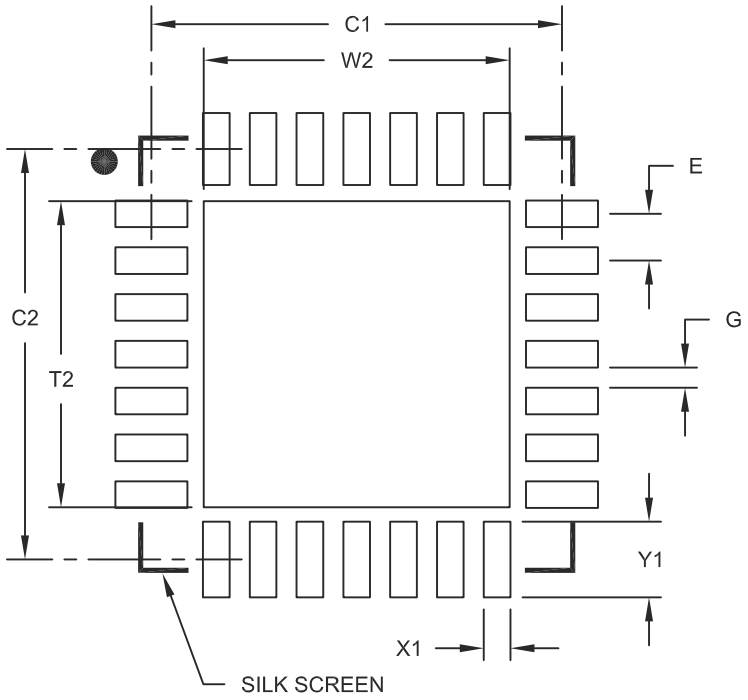
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing C04-052C Sheet 2 of 2

### 28-Lead Plastic Quad Flat, No Lead Package (ML) – 6x6 mm Body [QFN] with 0.55 mm Contact Length

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E | | 0.65 BSC | |
| Optional Center Pad Width | W2 | | | 4.25 |
| Optional Center Pad Length | T2 | | | 4.25 |
| Contact Pad Spacing | C1 | | 5.70 | |
| Contact Pad Spacing | C2 | | 5.70 | |
| Contact Pad Width (X28) | X1 | | | 0.37 |
| Contact Pad Length (X28) | Y1 | | | 1.00 |
| Distance Between Pads | G | 0.20 | | |

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2105A


© 2007-2011 Microchip Technology Inc.

**TABLE 25-1: MAJOR SECTION UPDATES**

| Section Name | Update Description |
|---|---|
| **Section 19.0 "10-bit/12-bit Analog-to-Digital Converter (ADC)"** | Updated ADC Conversion Clock Select bits in the AD1CON3 register from ADCS<**5**:0> to ADCS<**7**:0>. Any references to these bits have also been updated throughout this data sheet (Register 19-3).<br><br>Replaced Figure 19-1 (ADC1 Module Block Diagram for dsPIC33FJ12MC201) and added Figure 19-2 (ADC1 Block Diagram for dsPIC33FJ12MC202).<br><br>Removed Equation 19-1: ADC Conversion Clock Period and Figure 19-2: ADC Transfer Function (10-Bit Example).<br><br>Added Note 2 to Figure 19-2: ADC Conversion Clock Period Block Diagram.<br><br>Updated ADC1 Input Channel 1, 2, 3 Select Register (see Register 19-4) as follows:<br>• Changed bit 10-9 (CH123NB - dsPIC33FJ12MC201 devices only) description for bit value of `10` (if AD12B = `0`).<br>• Updated bit 8 (CH123SB) to reflect device-specific information.<br>• Updated bit 0 (CH123SA) to reflect device-specific information.<br>• Changed bit 2-1 (CH123NA - dsPIC33FJ12MC201 devices only) description for bit value of `10` (if AD12B = `0`).<br><br>Updated ADC1 Input Channel 0 Select Register (see Register 19-5) as follows:<br>• Changed bit value descriptions for bits 12-8<br>• Changed bit value descriptions for bits 4-0 (dsPIC33FJ12MC201 devices)<br><br>Modified Notes 1 and 2 in the ADC1 Input Scan Select Register Low (see Register 19-6)<br><br>Modified Notes 1 and 2 in the ADC1 Port Configuration Register Low (see Register 19-7) |
| **Section 20.0 "Special Features"** | Added FICD register information for address 0xF8000E in the Device Configuration Register Map (see Table 20-1).<br><br>Added FICD register content (BKBUG, COE, JTAGEN, and ICS<1:0> to the dsPIC33FJ12MC201/202 Configuration Bits Description (see Table 20-2).<br><br>Added a note regarding the placement of low-ESR capacitors, after the second paragraph of **Section 20.2 "On-Chip Voltage Regulator"** and to Figure 20-2.<br><br>Removed the words "if enabled" from the second sentence in the fifth paragraph of **Section 20.3 "BOR: Brown-out Reset"** |

## Revision E (July 2011)

This revision includes formatting changes and minor typographical throughout the data sheet text.

Global changes include:

- Removed Preliminary marking from the footer
- Updated all family reference manual information in the note boxes located at the beginning of most chapters
- Changed all instances of VCAP/VDDCORE to VCAP

All other major changes are referenced by their respective section in the following table.

**TABLE 25-3: MAJOR SECTION UPDATES**

| Section Name | Update Description |
|---|---|
| **Section 2.0 "Guidelines for Getting Started with 16-bit Digital Signal Controllers"** | Changed the title of section 2.3 to **Section 2.3 "CPU Logic Filter Capacitor Connection (VCAP)"**.<br><br>Updated the second paragraph in **Section 2.9 "Unused I/Os"**. |
| **Section 4.0 "Memory Organization"** | Revised the data memory implementation value in the third paragraph of **Section 4.2 "Data Address Space"**.<br><br>Updated the All Resets values for TMR1, TMR2, and TMR3 in the Timer Register Map (see Table 4-5). |
| **Section 8.0 "Oscillator Configuration"** | Added Note 3 to the Oscillator Control Register (see Register 8-1).<br><br>Added Note 2 to the Clock Divisor Register (see Register 8-2).<br><br>Added Note 1 to the PLL Feedback Divisor Register (see Register 8-3).<br><br>Added Note 2 to the FRC Oscillator Tuning Register (see Register 8-4). |
| **Section 10.0 "I/O Ports"** | Revised the second paragraph in **Section 10.1.1 "Open-Drain Configuration"**. |
| **Section 14.0 "Output Compare"** | Updated the Output Compare Module Block Diagram (see Figure 14-1). |
| **Section 19.0 "Universal Asynchronous Receiver Transmitter (UART)"** | Revised the UART module Baud Rate features, replacing both items with "Baud rates ranging from 10 Mbps to 38 bps at 40 MIPS". |
| **Section 21.0 "Special Features"** | Revised all paragraphs in **Section 21.1 "Configuration Bits"**.<br><br>Updated the Device Configuration Register Map (see Table 21-1).<br><br>Added the RTSP Effect column in the Configuration Bits Description (see Table 21-2). |


© 2007-2011 Microchip Technology Inc.