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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I ² C, IrDA, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I ² S, LVD, POR, PS2, PWM, WDT
Number of I/O	31
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 5.5V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/nuc120ld1bn



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- ADC
 - 12-bit SAR ADC with 600K SPS
 - Up to 8-ch single-end input or 4-ch differential input
 - Single scan/single cycle scan/continuous scan
 - Each channel with individual result register
 - Scan on enabled channels
 - Threshold voltage detection
 - Conversion start by software programming or external input
 - Support PDMA mode
- Analog Comparator
 - Up to two analog comparators
 - External input or internal bandgap voltage selectable at negative node
 - Interrupt when compare result change
 - Power down wake-up
- One built-in temperature sensor with 1°C resolution
- Brown-Out detector
 - With 4 levels: 4.5 V/3.8 V/2.7 V/2.2 V
 - Support Brown-Out Interrupt and Reset option
- Low Voltage Reset
 - Threshold voltage levels: 2.0 V
- Operating Temperature: -40°C~85°C
- Packages:
 - All Green package (RoHS)
 - LQFP 100-pin / 64-pin / 48-pin (100-pin for NuMicro™ NUC100/NUC120 Medium Density Only)



3 PARTS INFORMATION LIST AND PIN CONFIGURATION

3.1 NuMicro™ NUC120 Products Selection Guide

3.1.1 NuMicro™ NUC120 Medium Density USB Line Selection Guide

Part number	APROM	RAM	Data Flash	ISP Loader ROM	I/O	Timer	Connectivity						I ² S	Comp.	PWM	ADC	RTC	EBI	ISP ICP	Package
							UART	SPI	I ² C	USB	LIN	CAN								
NUC120LD3AN	64 KB	16 KB	4 KB	4 KB	up to 31	4x32-bit	2	1	2	1	-	-	1	1	4	8x12-bit	v	-	v	LQFP48
NUC120LE3AN	128 KB	16 KB	Definable	4 KB	up to 31	4x32-bit	2	1	2	1	-	-	1	1	4	8x12-bit	v	-	v	LQFP48
NUC120RD3AN	64 KB	16 KB	4 KB	4 KB	up to 45	4x32-bit	2	2	2	1	-	-	1	2	6	8x12-bit	v	-	v	LQFP64
NUC120RE3AN	128 KB	16 KB	Definable	4 KB	up to 45	4x32-bit	2	2	2	1	-	-	1	2	6	8x12-bit	v	-	v	LQFP64
NUC120VD2AN	64 KB	8 KB	4 KB	4 KB	up to 76	4x32-bit	3	4	2	1	-	-	1	2	8	8x12-bit	v	-	v	LQFP100
NUC120VD3AN	64 KB	16 KB	4 KB	4 KB	up to 76	4x32-bit	3	4	2	1	-	-	1	2	8	8x12-bit	v	-	v	LQFP100
NUC120VE3AN	128 KB	16 KB	Definable	4 KB	up to 76	4x32-bit	3	4	2	1	-	-	1	2	8	8x12-bit	v	-	v	LQFP100

3.1.2 NuMicro™ NUC120 Low Density USB Line Selection Guide

Part number	APROM	RAM	Data Flash	ISP Loader ROM	I/O	Timer	Connectivity						I ² S	Comp.	PWM	ADC	RTC	EBI	ISP ICP	Package
							UART	SPI	I ² C	USB	LIN	CAN								
NUC120LC1BN	32 KB	4 KB	4 KB	4 KB	up to 31	4x32-bit	2	1	2	1	-	-	1	1	4	8x12-bit	v	-	v	LQFP48
NUC120LD1BN	64 KB	4 KB	4 KB	4 KB	up to 31	4x32-bit	2	1	2	1	-	-	1	1	4	8x12-bit	v	-	v	LQFP48
NUC120LD2BN	64 KB	8 KB	4 KB	4 KB	up to 31	4x32-bit	2	1	2	1	-	-	1	1	4	8x12-bit	v	-	v	LQFP48
NUC120RC1BN	32 KB	4 KB	4 KB	4 KB	up to 45	4x32-bit	2	2	2	1	-	-	1	2	4	8x12-bit	v	v	v	LQFP64
NUC120RD1BN	64 KB	4 KB	4 KB	4 KB	up to 45	4x32-bit	2	2	2	1	-	-	1	2	4	8x12-bit	v	v	v	LQFP64
NUC120RD2BN	64 KB	8 KB	4 KB	4 KB	up to 45	4x32-bit	2	2	2	1	-	-	1	2	4	8x12-bit	v	v	v	LQFP64

3.2.1.3 NuMicro™ NUC120 Medium Density LQFP 48 pin

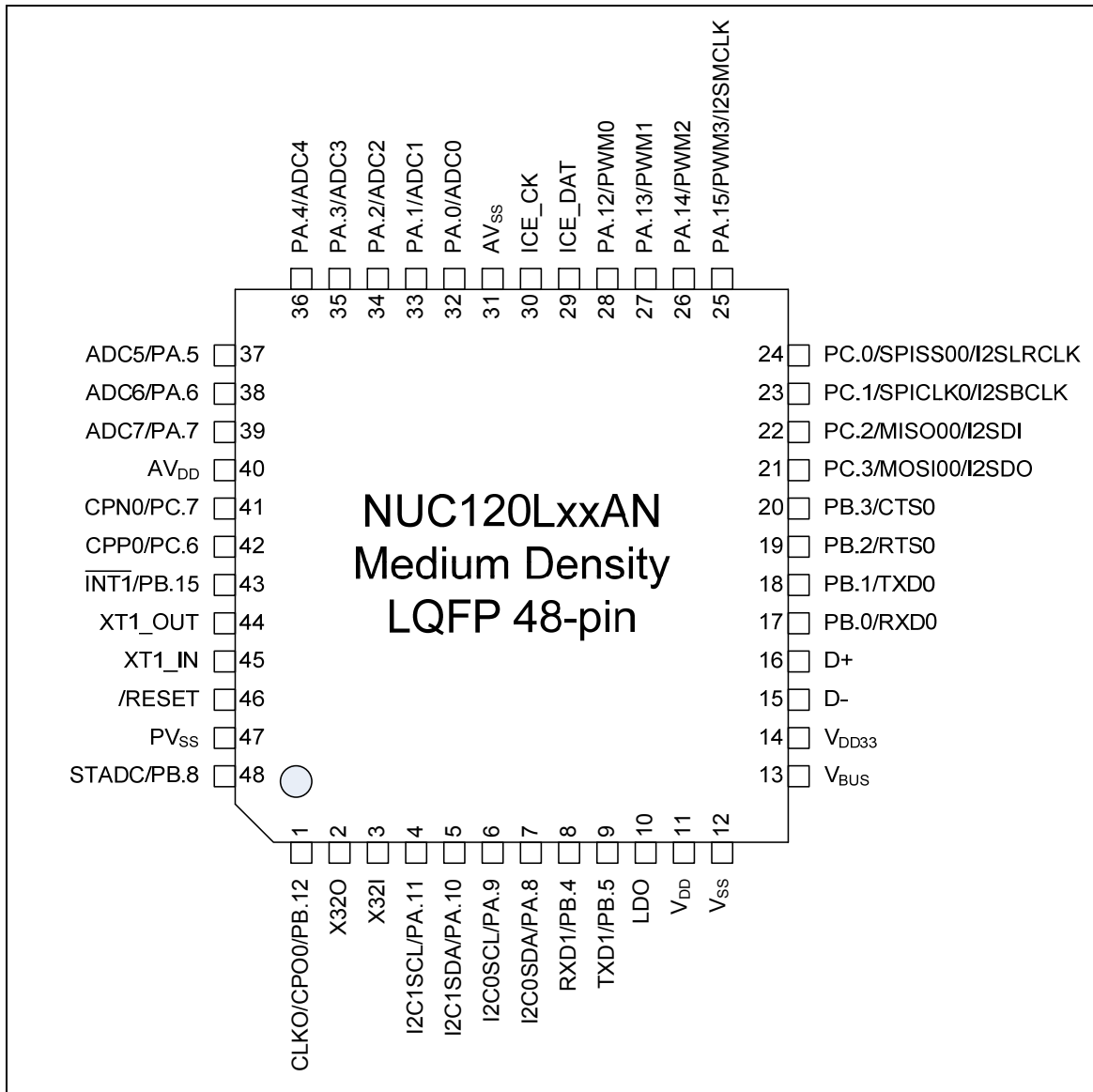


Figure 3-4 NuMicro™ NUC120 Medium Density LQFP 48-pin Pin Diagram

3.2.2.2 NuMicro™ NUC120 Low Density LQFP 48 pin

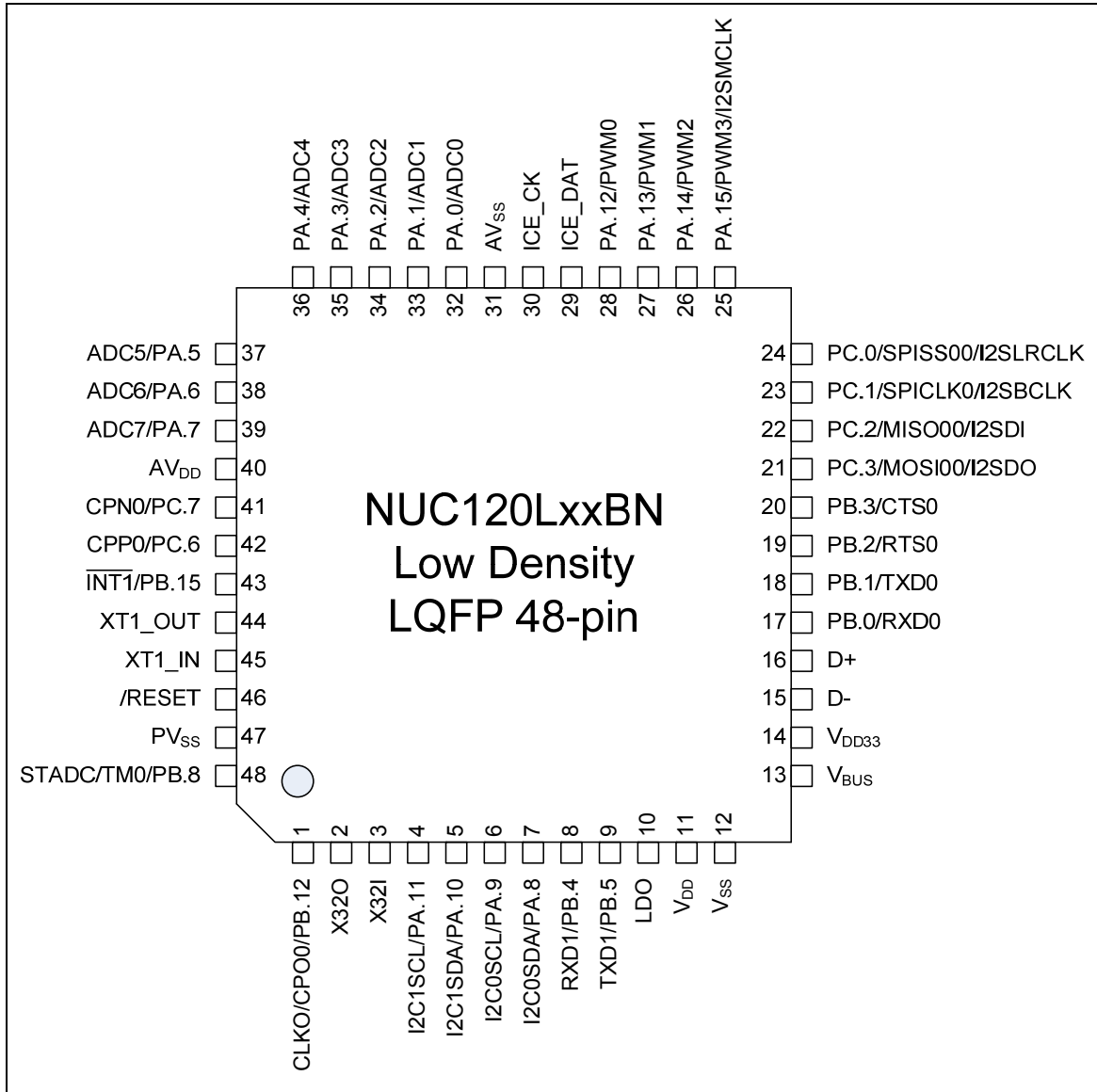


Figure 3-6 NuMicro™ NUC120 Low Density LQFP 48-pin Pin Diagram

4 BLOCK DIAGRAM

4.1 NuMicro™ NUC120 Medium Density Block Diagram

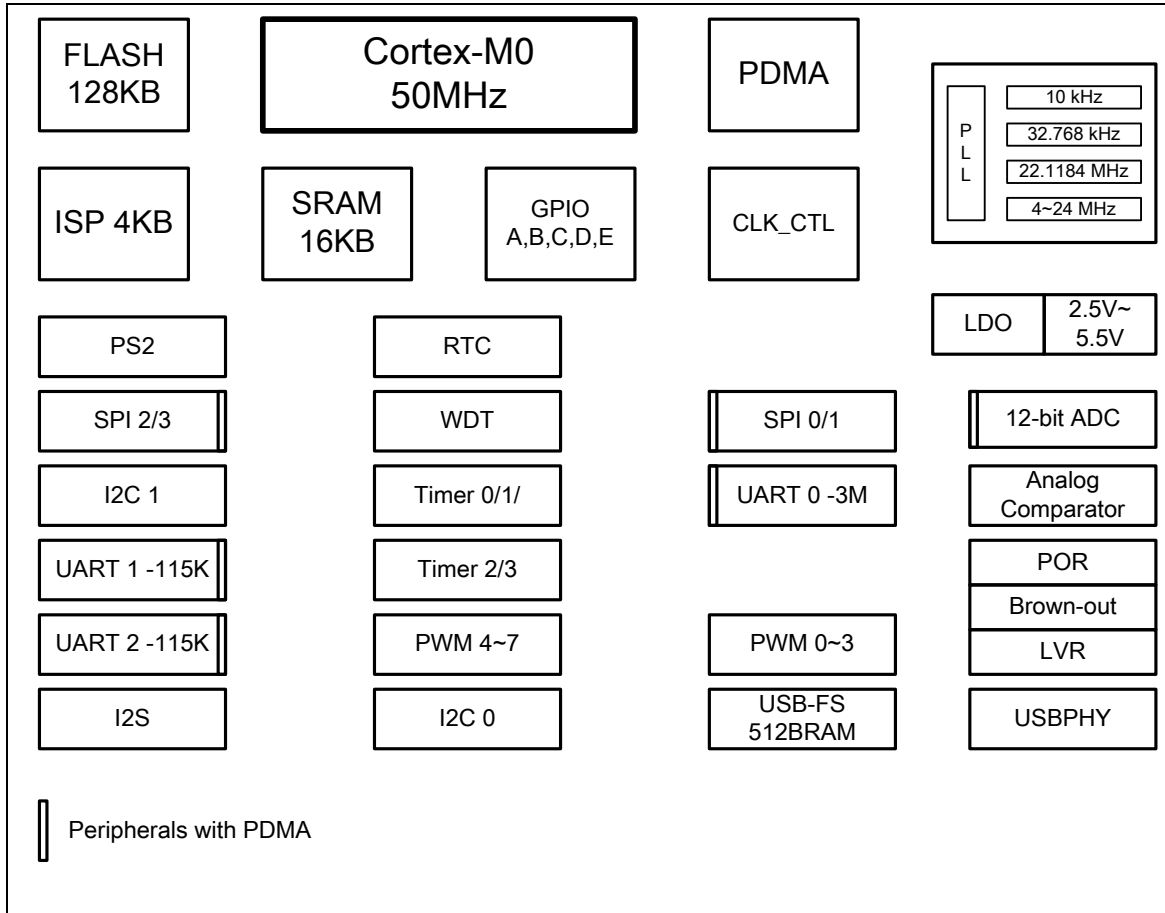


Figure 4-1 NuMicro™ NUC120 Medium Density Block Diagram

5.3.2 Clock Generator

The clock generator consists of 5 clock sources which are listed below:

- One external 32.768 kHz low speed crystal
- One external 4~24 MHz high speed crystal
- One programmable PLL FOUT(PLL source consists of external 4~24 MHz high speed crystal and internal 22.1184 MHz high speed oscillator)
- One internal 22.1184 MHz high speed oscillator
- One internal 10 kHz low speed oscillator

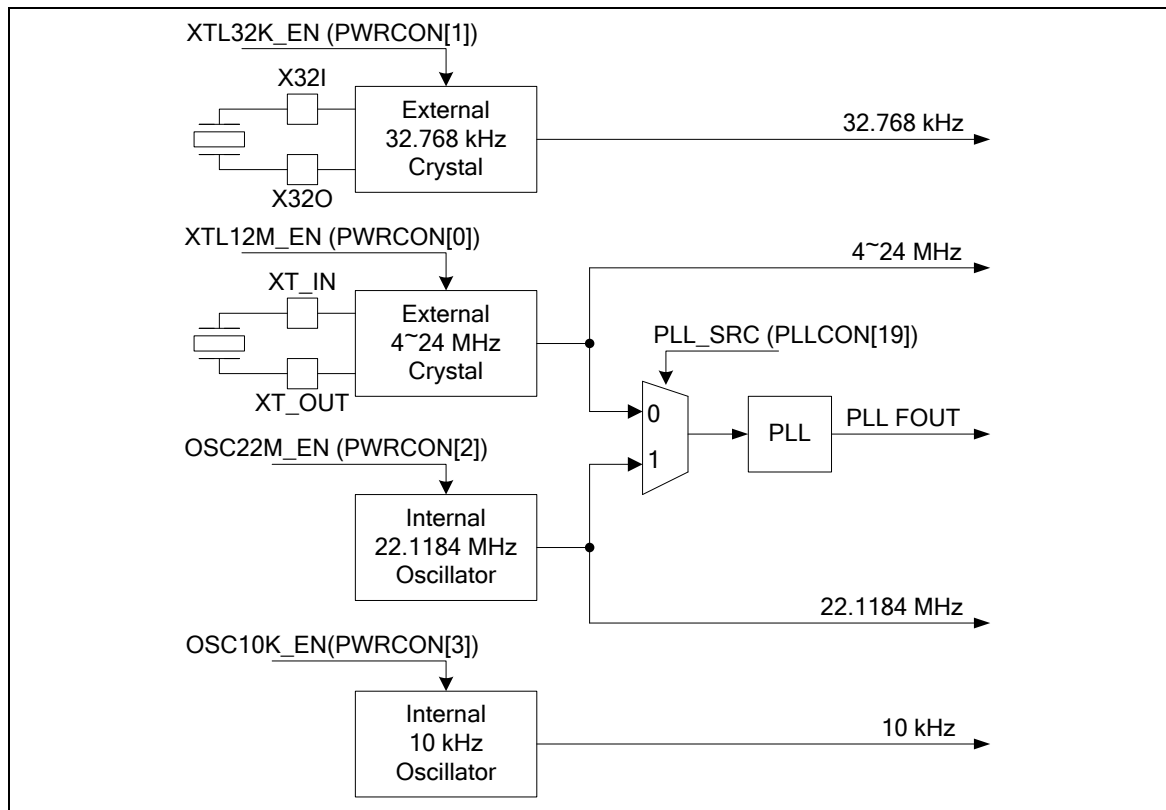


Figure 5-4 Clock generator block diagram

5.3.3 System Clock and SysTick Clock

The system clock has 5 clock sources which were generated from clock generator block. The clock source switch depends on the register HCLK_S (CLKSEL0[2:0]). The block diagram is showed in Figure 5-5.

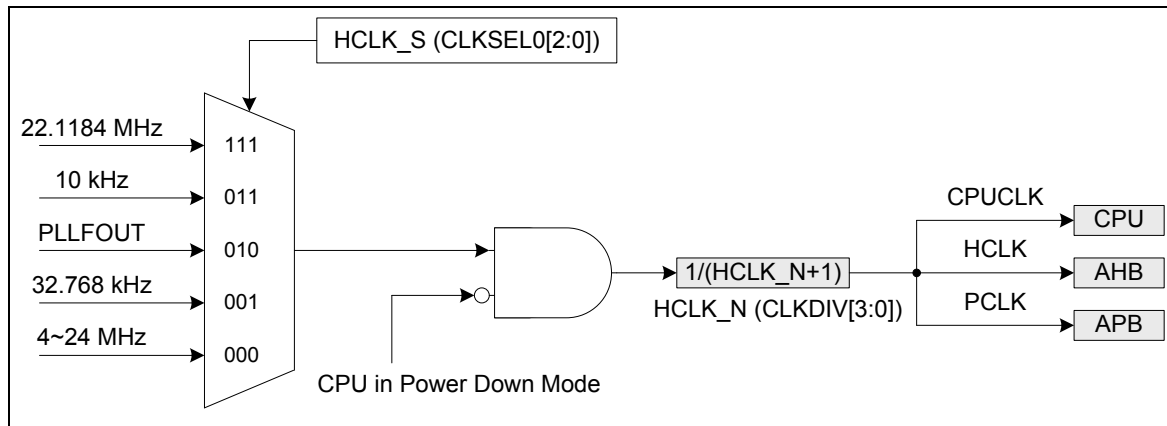


Figure 5-5 System Clock Block Diagram

The clock source of SysTick in Cortex-M0 core can use CPU clock or external clock (SYST_CSR[2]). If using external clock, the SysTick clock (STCLK) has 5 clock sources. The clock source switch depends on the setting of the register STCLK_S (CLKSEL0[5:3]). The block diagram is showed in Figure 5-6.

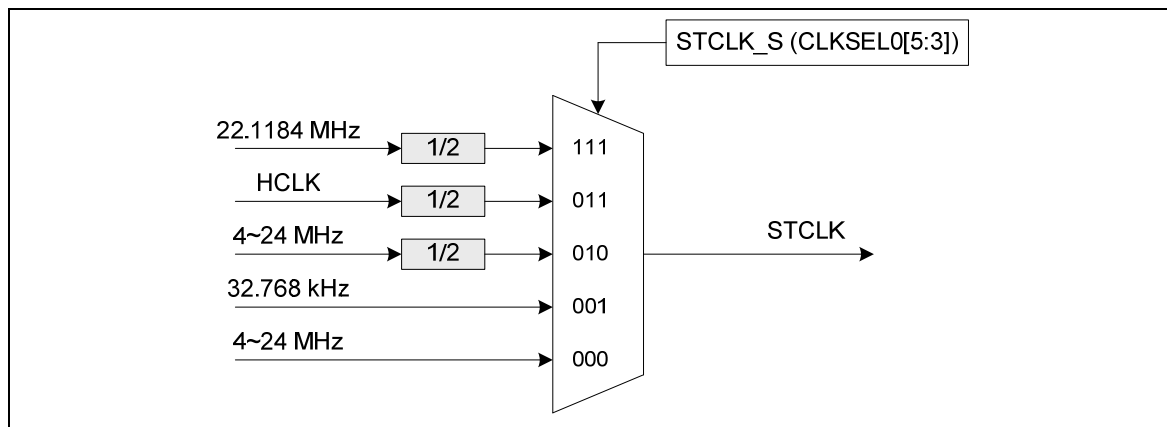


Figure 5-6 SysTick Clock Control Block Diagram

5.4 USB Device Controller (USB)

5.4.1 Overview

There is one set of USB 2.0 full-speed device controller and transceiver in this device. It is compliant with USB 2.0 full-speed device specification and support control/bulk/interrupt/isochronous transfer types.

In this device controller, there are two main interfaces: the APB bus and USB bus which comes from the USB PHY transceiver. For the APB bus, the CPU can program control registers through it. There are 512 bytes internal SRAM as data buffer in this controller. For IN or OUT transfer, it is necessary to write data to SRAM or read data from SRAM through the APB interface or SIE. Users need to set the effective starting address of SRAM for each endpoint buffer through “buffer segmentation register (USB_BUFSEGx)”.

There are 6 endpoints in this controller. Each of the endpoint can be configured as IN or OUT endpoint. All the operations including Control, Bulk, Interrupt and Isochronous transfer are implemented in this block. The block of ENDPOINT CONTROL is also used to manage the data sequential synchronization, endpoint states, current start address, transaction status, and data buffer status for each endpoint.

There are four different interrupt events in this controller. They are the wake-up function, device plug-in or plug-out event, USB events, like IN ACK, OUT ACK etc, and BUS events, like suspend and resume, etc. Any event will cause an interrupt, and users just need to check the related event flags in interrupt event status register (USB_INTSTS) to acknowledge what kind of interrupt occurring, and then check the related USB Endpoint Status Register (USB_EPSTS) to acknowledge what kind of event occurring in this endpoint.

A software-disable function is also supported for this USB controller. It is used to simulate the disconnection of this device from the host. If user enables DRVSE0 bit (USB_DRVSE0), the USB controller will force the output of USB_DP and USB_DM to level low and its function is disabled. After disable the DRVSE0 bit, host will enumerate the USB device again.

Reference: Universal Serial Bus Specification Revision 1.1

5.4.2 Features

This Universal Serial Bus (USB) performs a serial interface with a single connector type for attaching all USB peripherals to the host system. Following is the feature listing of this USB.

- Compliant with USB 2.0 Full-Speed specification
- Provide 1 interrupt vector with 4 different interrupt events (WAKEUP, FLDET, USB and BUS)
- Support Control/Bulk/Interrupt/Isochronous transfer type
- Support suspend function when no bus activity existing for 3 ms
- Provide 6 endpoints for configurable Control/Bulk/Interrupt/Isochronous transfer types and maximum 512 bytes buffer size
- Provide remote wake-up capability

5.6 I²C Serial Interface Controller (Master/Slave) (I²C)

5.6.1 Overview

I²C is a two-wire, bi-directional serial bus that provides a simple and efficient method of data exchange between devices. The I²C standard is a true multi-master bus including collision detection and arbitration that prevents data corruption if two or more masters attempt to control the bus simultaneously.

Data is transferred between a Master and a Slave synchronously to SCL on the SDA line on a byte-by-byte basis. Each data byte is 8-bit long. There is one SCL clock pulse for each data bit with the MSB being transmitted first. An acknowledge bit follows each transferred byte. Each bit is sampled during the high period of SCL; therefore, the SDA line may be changed only during the low period of SCL and must be held stable during the high period of SCL. A transition on the SDA line while SCL is high is interpreted as a command (START or STOP). Please refer to the Figure 5-9 for more detail I²C BUS Timing.

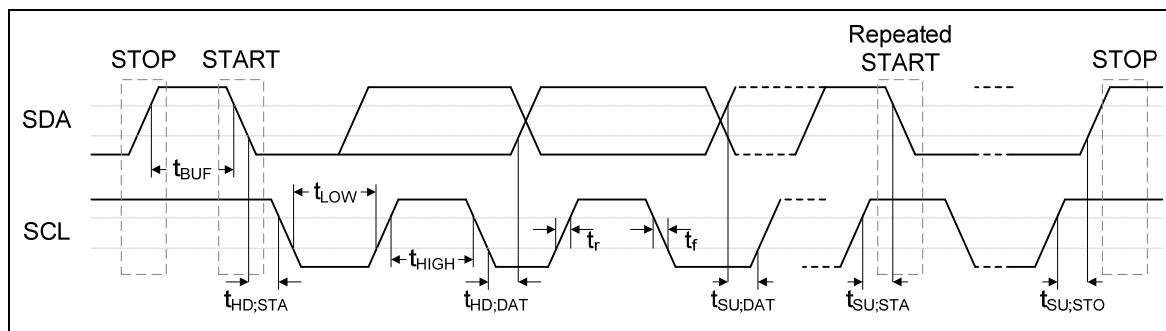


Figure 5-9 I²C Bus Timing

The device's on-chip I²C logic provides the serial interface that meets the I²C bus standard mode specification. The I²C port handles byte transfers autonomously. To enable this port, the bit ENS1 in I2CON should be set to '1'. The I²C H/W interfaces to the I²C bus via two pins: SDA and SCL. Pull up resistor is needed for I²C operation as these are open drain pins. When the I/O pins are used as I²C port, user must set the pins function to I²C in advance.

5.8 Real Time Clock (RTC)

5.8.1 Overview

Real Time Clock (RTC) controller provides user the real time and calendar message. The clock source of RTC is from an external 32.768 kHz low speed crystal connected at pins X32I and X32O (reference to pin descriptions) or from an external 32.768 kHz low speed oscillator output fed at pin X32I. The RTC controller provides the time message (second, minute, hour) in Time Loading Register (TLR) as well as calendar message (day, month, year) in Calendar Loading Register (CLR). The data message is expressed in BCD format. It also offers alarm function that user can preset the alarm time in Time Alarm Register (TAR) and alarm calendar in Calendar Alarm Register (CAR).

The RTC controller supports periodic Time Tick and Alarm Match interrupts. The periodic interrupt has 8 period options 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2 and 1 second which are selected by TTR (TTR[2:0]). When RTC counter in TLR and CLR is equal to alarm setting time registers TAR and CAR, the alarm interrupt flag (RIIR.AIF) is set and the alarm interrupt is requested if the alarm interrupt is enabled (RIER.AIER=1). Both RTC Time Tick and Alarm Match can cause chip wake-up from power down mode if wake-up function is enabled (TWKE (TTR[3])=1).

5.8.2 Features

- There is a time counter (second, minute, hour) and calendar counter (day, month, year) for user to check the time
- Alarm register (second, minute, hour, day, month, year)
- 12-hour or 24-hour mode is selectable
- Leap year compensation automatically
- Day of week counter
- Frequency compensate register (FCR)
- All time and calendar message is expressed in BCD code
- Support periodic time tick interrupt with 8 period options 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2 and 1 second
- Support RTC Time Tick and Alarm Match interrupt
- Support wake-up chip from power down mode

5.17 PDMA Controller (PDMA)

5.17.1 Overview

NuMicro™ NUC100/NUC120 Medium Density contains a peripheral direct memory access (PDMA) controller that transfers data to and from memory or transfer data to and from APB devices. The PDMA has nine channels of DMA (Peripheral-to-Memory or Memory-to-Peripheral or Memory-to-Memory). For each PDMA channel (PDMA CH0~CH8), there is one word buffer as transfer buffer between the Peripherals APB devices and Memory.

Software can stop the PDMA operation by disable PDMA [PDMACEN]. The CPU can recognize the completion of a PDMA operation by software polling or when it receives an internal PDMA interrupt. The PDMA controller can increase source or destination address or fixed them as well.

Notice: NuMicro™ NUC100/NUC120 Low Density only has 1 PDMA channel (channel 0).

5.17.2 Features

- Up to nine DMA channels. Each channel can support a unidirectional transfer (NuMicro™ NUC100/NUC120 Low Density only has 1 PDMA channel)
- AMBA AHB master/slave interface compatible, for data transfer and register read/write
- Support source and destination address increased mode or fixed mode
- Hardware channel priority. DMA channel 0 has the highest priority and channel 8 has the lowest priority

5.18 External Bus Interface (EBI)

5.18.1 Overview

The NuMicro™ NUC100/NUC120 Low Density LQFP-64 package equips an external bus interface (EBI) for external device used.

To save the connections between external device and this chip, EBI support address bus and data bus multiplex mode. And, address latch enable (ALE) signal supported differentiate the address and data cycle.

5.18.2 Features

External Bus Interface has the following functions:

- External devices with max. 64K-byte size (8-bit data width)/128K-byte (16-bit data width) supported
- Variable external bus base clock (MCLK) supported
- 8-bit or 16-bit data width supported
- Variable data access time (tACC), address latch enable time (tALE) and address hold time (tAHD) supported
- Address bus and data bus multiplex mode supported to save the address pins
- Configurable idle cycle supported for different access condition: Write command finish (W2X), Read-to-Read (R2R)

6 FLASH MEMORY CONTROLLER (FMC)

6.1 Overview

NuMicro™ NUC100 Series equips with 128/64/32K bytes on chip embedded Flash for application program memory (APROM) that can be updated through ISP procedure. In System Programming (ISP) function enables user to update program memory when chip is soldered on PCB. After chip power on, Cortex-M0 CPU fetches code from APROM or LDROM decided by boot select (CBS) in Config0. By the way, NuMicro™ NUC100 Series also provides additional DATA Flash for user, to store some application dependent data before chip power off. For 128K bytes APROM device, the data flash is shared with original 128K program memory and its start address is configurable and defined by user application request in Config1. For 64K/32K bytes APROM device, the data flash is fixed at 4K.

6.2 Features

- Run up to 50 MHz with zero wait state for continuous address read access
- 128/64/32KB application program memory (APROM) (NuMicro™ NUC100/NUC120 Low Density only support up to 64KB size)
- 4KB in system programming (ISP) loader program memory (LDROM)
- Configurable or fixed 4KB data flash with 512 bytes page erase unit
- Programmable data flash start address for 128K APROM device
- In System Program (ISP) to update on chip Flash

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Input High Voltage PA, PB, PC, PD, PE (Schmitt input)	V _{IH2}	0.4 V _{DD}	-	V _{DD} +0.5	V	
Hysteresis voltage of PA~PE (Schmitt input)	V _{HY}		0.2 V _{DD}		V	
Input Low Voltage XT1 ^[*2]	V _{IL3}	0	-	0.8	V	V _{DD} = 4.5 V
		0	-	0.4		V _{DD} = 3.0 V
Input High Voltage XT1 ^[*2]	V _{IH3}	3.5	-	V _{DD} +0.2	V	V _{DD} = 5.5 V
		2.4	-	V _{DD} +0.2		V _{DD} = 3.0 V
Input Low Voltage X32I ^[*2]	V _{IL4}	0	-	0.4	V	
Input High Voltage X32I ^[*2]	V _{IH4}	1.7		2.5	V	
Negative going threshold (Schmitt input), /RESET	V _{ILS}	-0.5	-	0.3 V _{DD}	V	
Positive going threshold (Schmitt input), /RESET	V _{IHS}	0.7 V _{DD}	-	V _{DD} +0.5	V	
Source Current PA, PB, PC, PD, PE (Quasi-bidirectional Mode)	I _{SR11}	-300	-370	-450	μA	V _{DD} = 4.5 V, V _S = 2.4 V
	I _{SR12}	-50	-70	-90	μA	V _{DD} = 2.7 V, V _S = 2.2 V
	I _{SR13}	-40	-60	-80	μA	V _{DD} = 2.5 V, V _S = 2.0 V
Source Current PA, PB, PC, PD, PE (Push-pull Mode)	I _{SR21}	-20	-24	-28	mA	V _{DD} = 4.5 V, V _S = 2.4 V
	I _{SR22}	-4	-6	-8	mA	V _{DD} = 2.7 V, V _S = 2.2 V
	I _{SR23}	-3	-5	-7	mA	V _{DD} = 2.5 V, V _S = 2.0 V
Sink Current PA, PB, PC, PD, PE (Quasi-bidirectional and Push-pull Mode)	I _{SK11}	10	16	20	mA	V _{DD} = 4.5 V, V _S = 0.45 V
	I _{SK12}	7	10	13	mA	V _{DD} = 2.7 V, V _S = 0.45 V
	I _{SK13}	6	9	12	mA	V _{DD} = 2.5 V, V _S = 0.45 V
Brown-Out voltage with BOV_VL [1:0] = 00b	V _{BO2.2}	2.1	2.2	2.3	V	
Brown-Out voltage with BOV_VL [1:0] = 01b	V _{BO2.7}	2.6	2.7	2.8	V	
Brown-Out voltage with BOV_VL [1:0] = 10b	V _{BO3.8}	3.6	3.8	4.0	V	
Brown-Out voltage with BOV_VL [1:0] = 11b	V _{BO4.5}	4.3	4.5	4.7	V	
Hysteresis range of BOD voltage	V _{BH}	30	-	150	mV	V _{DD} = 2.5 V~5.5 V

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
	I _{DD8}		11.5		mA	V _{DD} = 3 V@12 MHz, disable all IP and disable PLL, XTAL=12 MHz
Operating Current Normal Run Mode @ 4 MHz	I _{DD9}		13.5		mA	V _{DD} = 5 V@4 MHz, enable all IP and disable PLL, XTAL=4 MHz
	I _{DD10}		10		mA	V _{DD} = 5 V@4 MHz, disable all IP and disable PLL, XTAL=4 MHz
	I _{DD11}		12		mA	V _{DD} = 3 V@4 MHz, enable all IP and disable PLL, XTAL=4 MHz
	I _{DD12}		8		mA	V _{DD} = 3 V@4 MHz, disable all IP and disable PLL, XTAL=4 MHz
Operating Current Idle Mode @ 50 MHz	I _{IDLE1}		30		mA	V _{DD} = 5.5 V@50 MHz, enable all IP and PLL, XTAL=12 MHz
	I _{IDLE2}		13		mA	V _{DD} =5.5 V@50 MHz, disable all IP and enable PLL, XTAL=12 MHz
	I _{IDLE3}		28		mA	V _{DD} = 3 V@50 MHz, enable all IP and PLL, XTAL=12 MHz
	I _{IDLE4}		12		mA	V _{DD} = 3 V@50 MHz, disable all IP and enable PLL, XTAL=12 MHz
Operating Current Idle Mode @ 12 MHz	I _{IDLE5}		11		mA	V _{DD} = 5.5 V@12 MHz, enable all IP and disable PLL, XTAL=12 MHz
	I _{IDLE6}		5		mA	V _{DD} = 5.5 V@12 MHz, disable all IP and disable PLL, XTAL=12 MHz
	I _{IDLE7}		10		mA	V _{DD} = 3 V@12 MHz, enable all IP and disable PLL, XTAL=12 MHz

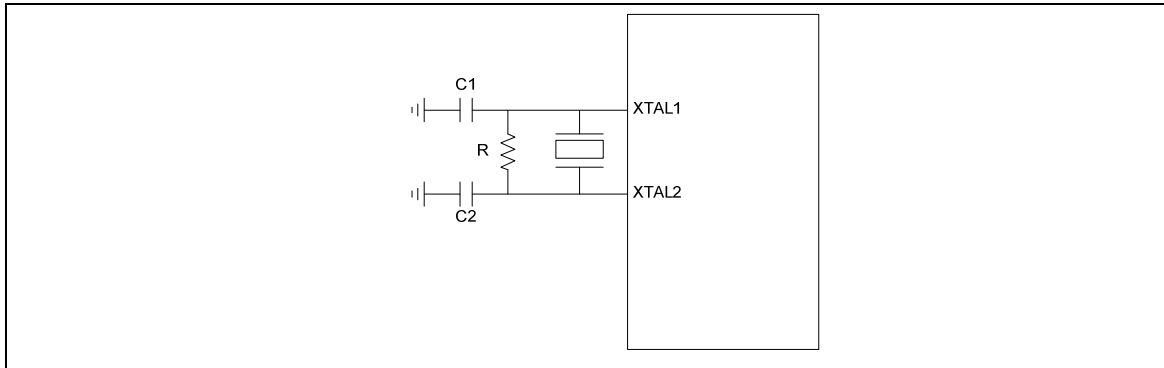


Figure 7-1 Typical Crystal Application Circuit

7.3.2 External 32.768 kHz Low Speed Crystal

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Input clock frequency	External crystal	-	32.768	-	kHz
Temperature	-	-40	-	85	°C
V _{DD}	-	2.5	-	5.5	V

7.3.3 Internal 22.1184 MHz High Speed Oscillator

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Supply voltage ^[1]	-	2.5	-	5.5	V
Center Frequency	-	-	22.1184	-	MHz
Calibrated Internal Oscillator Frequency	+25°C; V _{DD} = 5 V	-1	-	+1	%
	-40°C ~ +85°C; V _{DD} = 2.5 V ~ 5.5 V	-3	-	+3	%
Operation Current	V _{DD} = 5 V	-	500	-	uA

7.3.4 Internal 10 kHz Low Speed Oscillator

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Supply voltage ^[1]	-	2.5	-	5.5	V
Center Frequency	-	-	10	-	kHz
Calibrated Internal Oscillator Frequency	+25°C; V _{DD} = 5 V	-30	-	+30	%
	-40°C ~ +85°C; V _{DD} = 2.5 V ~ 5.5 V	-50	-	+50	%

Note: Internal operation voltage comes from LDO.

7.4.2 Specification of LDO and Power management

PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTE
Input Voltage	2.7	5	5.5	V	V _{DD} input voltage
Output Voltage	-10%	2.5	+10%	V	V _{DD} > 2.7 V
Temperature	-40	25	85	°C	
Cbp	-	1	-	uF	Resr=1ohm

Note:

1. It is recommended that a 10uF or higher capacitor and a 100nF bypass capacitor are connected between V_{DD} and the closest V_{SS} pin of the device.
2. For ensuring power stability, a 1uF or higher capacitor must be connected between LDO pin and the closest V_{SS} pin of the device.

7.6 SPI Dynamic Characteristics

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
SPI master mode ($V_{DD} = 4.5V \sim 5.5V$, 30pF loading Capacitor)					
t_{DS}	Data setup time	26	18	-	ns
t_{DH}	Data hold time	0	-	-	ns
t_V	Data output valid time	-	4	6	ns
SPI master mode ($V_{DD} = 3.0V \sim 3.6V$, 30pF loading Capacitor)					
t_{DS}	Data setup time	39	26	-	ns
t_{DH}	Data hold time	0	-	-	ns
t_V	Data output valid time	-	6	10	ns
SPI slave mode ($V_{DD} = 4.5V \sim 5.5V$, 30pF loading Capacitor)					
t_{DS}	Data setup time	0	-	-	ns
t_{DH}	Data hold time	$2 \cdot PCLK + 4$	-	-	ns
t_V	Data output valid time	-	$2 \cdot PCLK + 19$	$2 \cdot PCLK + 27$	ns
SPI slave mode ($V_{DD} = 3.0V \sim 3.6V$, 30pF loading Capacitor)					
t_{DS}	Data setup time	0	-	-	ns
t_{DH}	Data hold time	$2 \cdot PCLK + 8$	-	-	ns
t_V	Data output valid time	-	$2 \cdot PCLK + 27$	$2 \cdot PCLK + 40$	ns

8.3 48L LQFP (7x7x1.4mm footprint 2.0mm)

