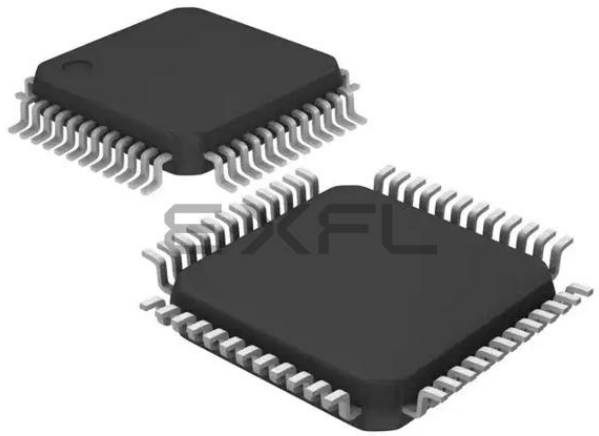

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Last Time Buy
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I²C, IrDA, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, LVD, POR, PS2, PWM, WDT
Number of I/O	31
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 5.5V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/nuc120ld2bn

- Full duplex synchronous serial data transfer
- Variable length of transfer data from 1 to 32 bits
- MSB or LSB first data transfer
- Rx and Tx on both rising or falling edge of serial clock independently
- 2 slave/device select lines when it is as the master, and 1 slave/device select line when it is as the slave
- Support byte suspend mode in 32-bit transmission
- Support PDMA mode

- I^2C
  - Up to two sets of I^2C device
  - Master/Slave mode
  - Bidirectional data transfer between masters and slaves
  - Multi-master bus (no central master)
  - Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
  - Serial clock synchronization allows devices with different bit rates to communicate via one serial bus
  - Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer
  - Programmable clocks allow versatile rate control
  - Support multiple address recognition (four slave address with mask option)
- I^2S
  - Interface with external audio CODEC
  - Operate as either master or slave mode
  - Capable of handling 8-, 16-, 24- and 32-bit word sizes
  - Mono and stereo audio data supported
  - I^2S and MSB justified data format supported
  - Two 8 word FIFO data buffers are provided, one for transmit and one for receive
  - Generates interrupt requests when buffer levels cross a programmable boundary
  - Support two DMA requests, one for transmit and one for receive
- PS/2 Device Controller
  - Host communication inhibit and request to send detection
  - Reception frame error detection
  - Programmable 1 to 16 bytes transmit buffer to reduce CPU intervention
  - Double buffer for data reception
  - S/W override bus
- USB 2.0 Full-Speed Device
  - One set of USB 2.0 FS Device 12Mbps
  - On-chip USB Transceiver
  - Provide 1 interrupt source with 4 interrupt events
  - Support Control, Bulk In/Out, Interrupt and Isochronous transfers
  - Auto suspend function when no bus signaling for 3 ms
  - Provide 6 programmable endpoints
  - Include 512 Bytes internal SRAM as USB buffer
  - Provide remote wake-up capability
- EBI (External bus interface) support (NuMicro™ NUC100/NUC120 Low Density 64-pin Package Only)
  - Accessible space: 64KB in 8-bit mode or 128KB in 16-bit mode
  - Support 8-/16-bit data width
  - Support byte write in 16-bit data width mode

3.2 Pin Configuration

3.2.1 NuMicro™ NUC120 Medium Density Pin Diagram

3.2.1.1 NuMicro™ NUC120 Medium Density LQFP 100 pin

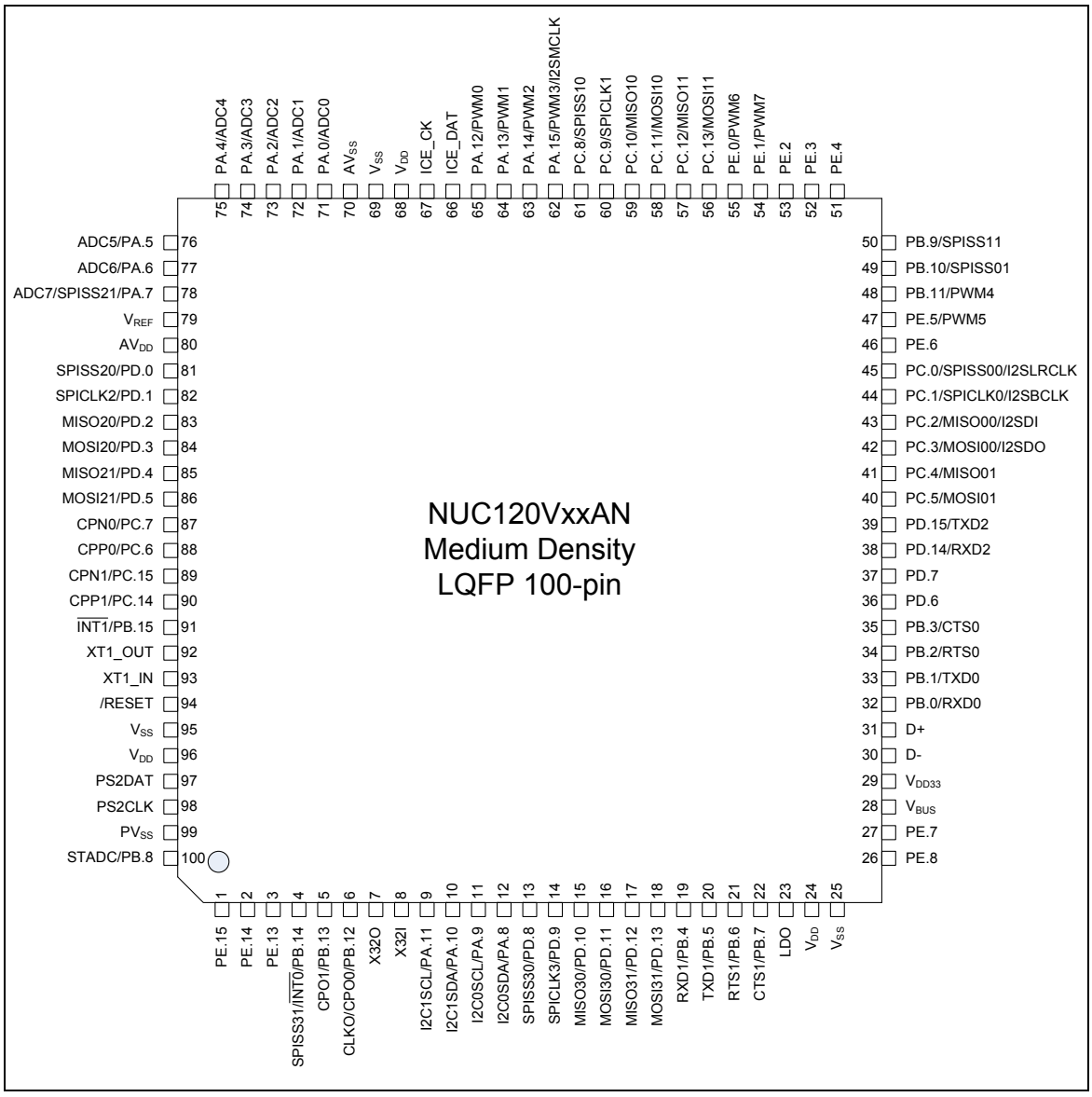


Figure 3-2 NuMicro™ NUC120 Medium Density LQFP 100-pin Pin Diagram

3.2.1.3 NuMicro™ NUC120 Medium Density LQFP 48 pin

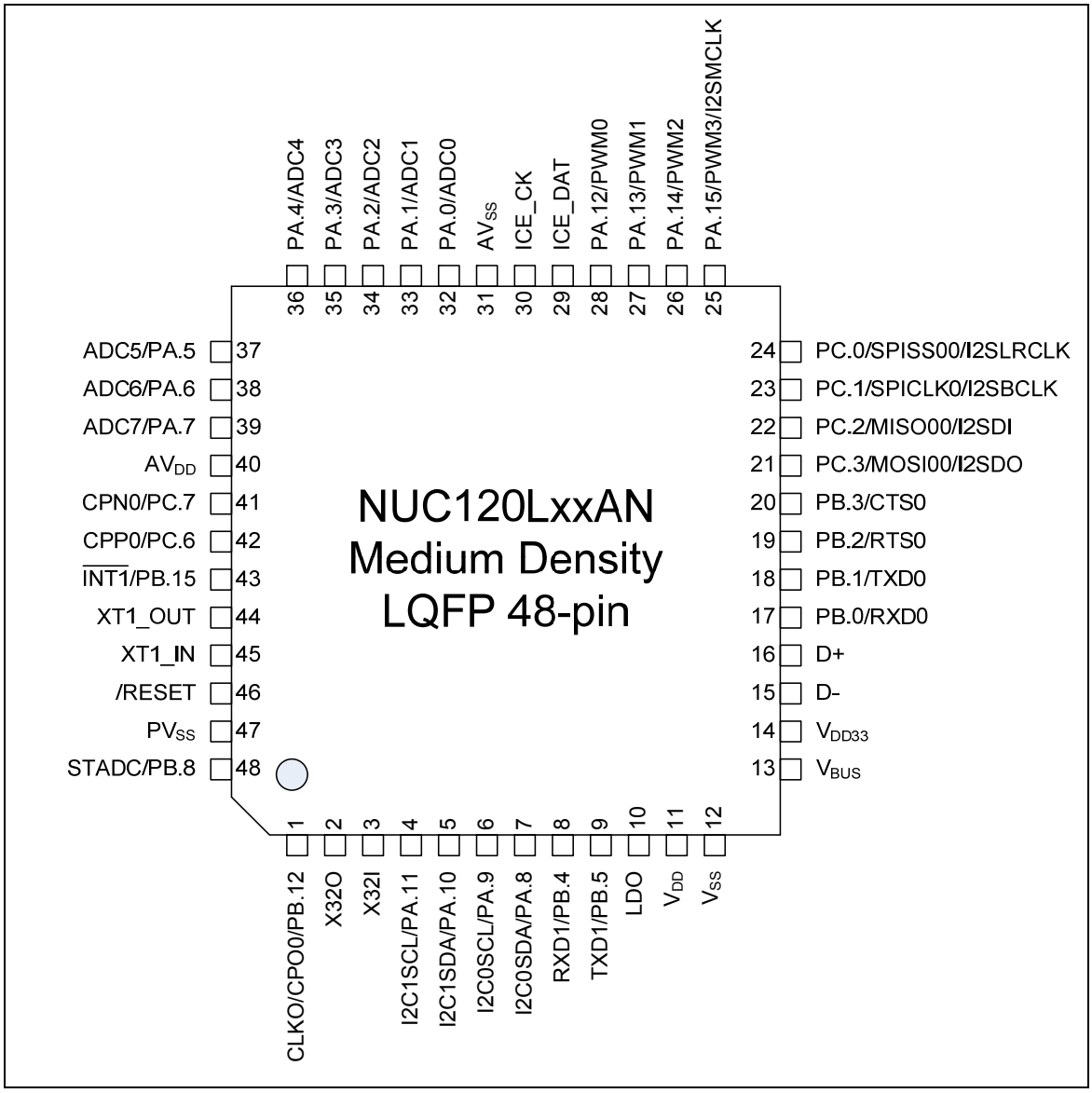


Figure 3-4 NuMicro™ NUC120 Medium Density LQFP 48-pin Pin Diagram

3.2.2 NuMicro™ NUC120 Low Density Pin Diagram

3.2.2.1 NuMicro™ NUC120 Low Density LQFP 64 pin

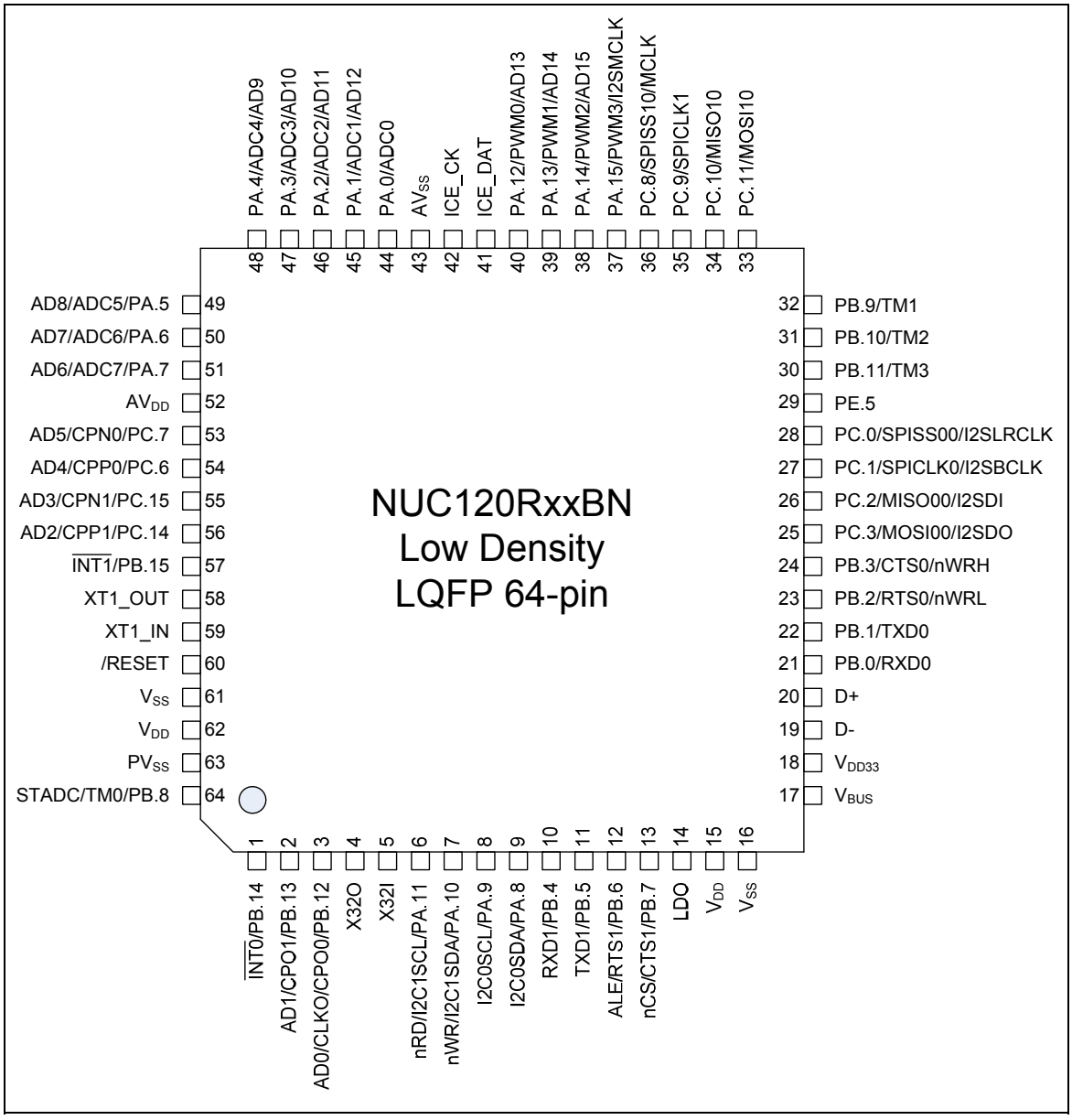


Figure 3-5 NuMicro™ NUC120 Low Density LQFP 64-pin Pin Diagram

Address Space	Token	Controllers
0x400E_0000 – 0x400E_FFFF	ADC_BA	Analog-Digital-Converter (ADC) Control Registers
APB2 Controllers Space (0x4010_0000 ~ 0x401F_FFFF)		
0x4010_0000 – 0x4010_3FFF	PS2_BA	PS/2 Interface Control Registers
0x4011_0000 – 0x4011_3FFF	TMR23_BA	Timer2/Timer3 Control Registers
0x4012_0000 – 0x4012_3FFF	I2C1_BA	I^2C1 Interface Control Registers
0x4013_0000 – 0x4013_3FFF	SPI2_BA	SPI2 with master/slave function Control Registers (NuMicro™ NUC100/NUC120 Medium Density Only)
0x4013_4000 – 0x4013_7FFF	SPI3_BA	SPI3 with master/slave function Control Registers (NuMicro™ NUC100/NUC120 Medium Density Only)
0x4014_0000 – 0x4014_3FFF	PWMB_BA	PWM4/5/6/7 Control Registers (NuMicro™ NUC100/NUC120 Medium Density Only)
0x4015_0000 – 0x4015_3FFF	UART1_BA	UART1 Control Registers
0x4015_4000 – 0x4015_7FFF	UART2_BA	UART2 Control Registers (NuMicro™ NUC100/NUC120 Medium Density Only)
0x401A_0000 – 0x401A_3FFF	I2S_BA	I^2S Interface Control Registers
System Controllers Space (0xE000_E000 ~ 0xE000_EFFF)		
0xE000_E010 – 0xE000_E0FF	SCS_BA	System Timer Control Registers
0xE000_E100 – 0xE000_ECFF	SCS_BA	External Interrupt Controller Control Registers
0xE000_ED00 – 0xE000_ED8F	SCS_BA	System Control Registers

Table 5-1 Address Space Assignments for On-Chip Controllers

5.2.6.1 Exception Model and System Interrupt Map

Table 5-2 lists the exception model supported by NuMicro™ NUC100 Series. Software can set four levels of priority on some of these exceptions as well as on all interrupts. The highest user-configurable priority is denoted as "0" and the lowest priority is denoted as "3". The default priority of all the user-configurable interrupts is "0". Note that priority "0" is treated as the fourth priority on the system, after three system exceptions "Reset", "NMI" and "Hard Fault".

Exception Name	Vector Number	Priority
Reset	1	-3
NMI	2	-2
Hard Fault	3	-1
Reserved	4 ~ 10	Reserved
SVCall	11	Configurable
Reserved	12 ~ 13	Reserved
PendSV	14	Configurable
SysTick	15	Configurable
Interrupt (IRQ0 ~ IRQ31)	16 ~ 47	Configurable

Table 5-2 Exception Model

Vector Number	Interrupt Number (Bit in Interrupt Registers)	Interrupt Name	Source IP	Interrupt description
0 ~ 15	-	-	-	System exceptions
16	0	**BOD_OUT**	Brown-Out	Brown-Out low voltage detected interrupt
17	1	**WDT_INT**	WDT	Watchdog Timer interrupt
18	2	**EINT0**	GPIO	External signal interrupt from PB.14 pin
19	3	**EINT1**	GPIO	External signal interrupt from PB.15 pin
20	4	**GPAB_INT**	GPIO	External signal interrupt from PA[15:0]/PB[13:0]
21	5	**GPCDE_INT**	GPIO	External interrupt from PC[15:0]/PD[15:0]/PE[15:0]
22	6	**PWMA_INT**	PWM0~3	PWM0, PWM1, PWM2 and PWM3 interrupt
23	7	**PWMB_INT**	PWM4~7	PWM4, PWM5, PWM6 and PWM7 interrupt
24	8	**TMR0_INT**	TMR0	Timer 0 interrupt
25	9	**TMR1_INT**	TMR1	Timer 1 interrupt

5.3.3 System Clock and SysTick Clock

The system clock has 5 clock sources which were generated from clock generator block. The clock source switch depends on the register HCLK_S (CLKSEL0[2:0]). The block diagram is showed in Figure 5-5.

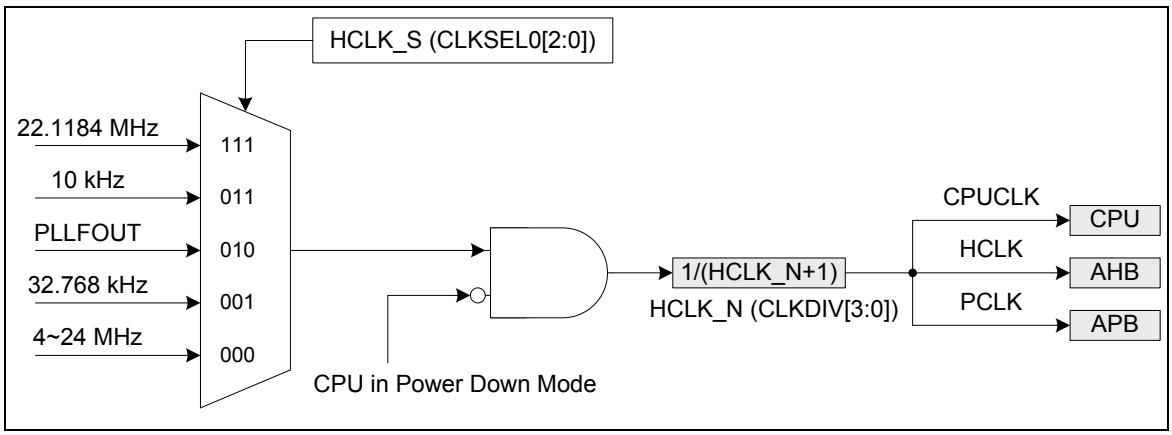


Figure 5-5 System Clock Block Diagram

The clock source of SysTick in Cortex-M0 core can use CPU clock or external clock (SYST_CSR[2]). If using external clock, the SysTick clock (STCLK) has 5 clock sources. The clock source switch depends on the setting of the register STCLK_S (CLKSEL0[5:3]). The block diagram is showed in Figure 5-6.

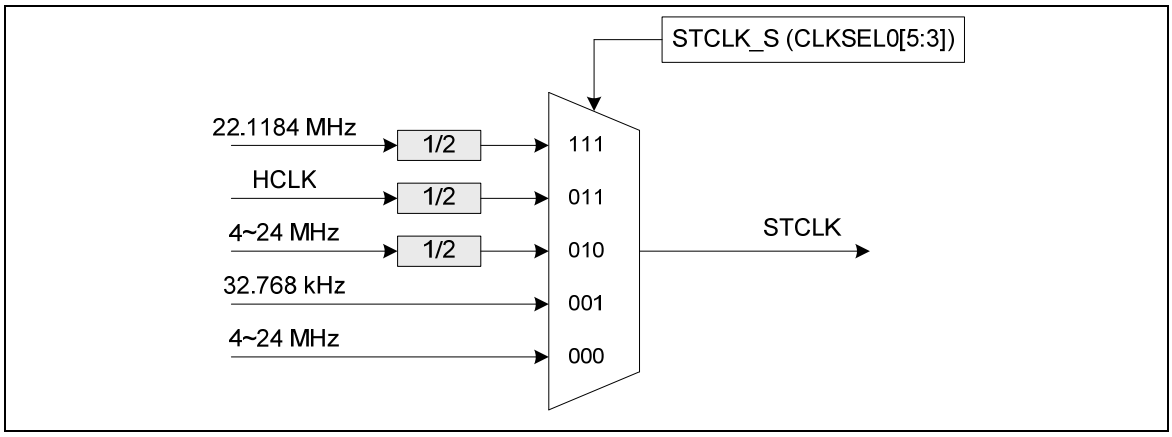


Figure 5-6 SysTick Clock Control Block Diagram

5.6 I²C Serial Interface Controller (Master/Slave) (I²C)

5.6.1 Overview

I²C is a two-wire, bi-directional serial bus that provides a simple and efficient method of data exchange between devices. The I²C standard is a true multi-master bus including collision detection and arbitration that prevents data corruption if two or more masters attempt to control the bus simultaneously.

Data is transferred between a Master and a Slave synchronously to SCL on the SDA line on a byte-by-byte basis. Each data byte is 8-bit long. There is one SCL clock pulse for each data bit with the MSB being transmitted first. An acknowledge bit follows each transferred byte. Each bit is sampled during the high period of SCL; therefore, the SDA line may be changed only during the low period of SCL and must be held stable during the high period of SCL. A transition on the SDA line while SCL is high is interpreted as a command (START or STOP). Please refer to the Figure 5-9 for more detail I²C BUS Timing.

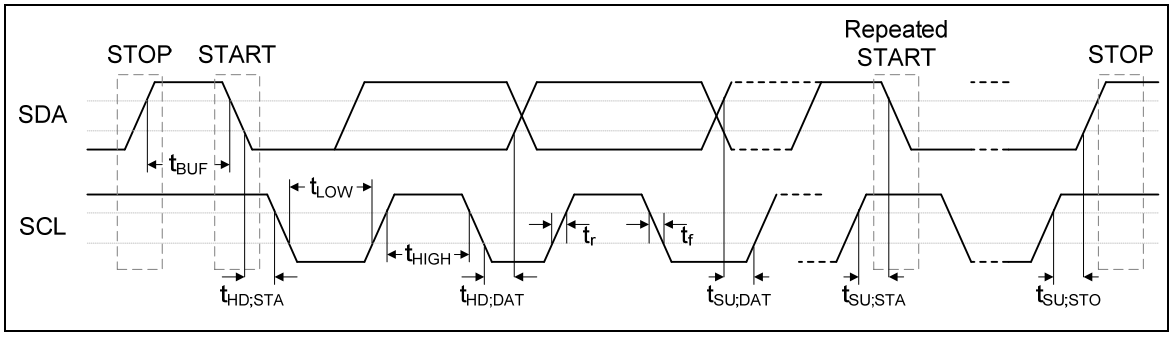


Figure 5-9 I²C Bus Timing

The device's on-chip I²C logic provides the serial interface that meets the I²C bus standard mode specification. The I²C port handles byte transfers autonomously. To enable this port, the bit ENS1 in I2CON should be set to '1'. The I²C H/W interfaces to the I²C bus via two pins: SDA and SCL. Pull up resistor is needed for I²C operation as these are open drain pins. When the I/O pins are used as I²C port, user must set the pins function to I²C in advance.

System clock = Internal 22.1184 MHz high speed oscillator						
Baud rate	Mode0		Mode1		Mode2	
	Parameter	Register	Parameter	Register	Parameter	Register
921600	x	x	A=0,B=11	0x2B00_0000	A=22	0x3000_0016
460800	A=1	0x0000_0001	A=1,B=15 A=2,B=11	0x2F00_0001 0x2B00_0002	A=46	0x3000_002E
230400	A=4	0x0000_0004	A=4,B=15 A=6,B=11	0x2F00_0004 0x2B00_0006	A=94	0x3000_005E
115200	A=10	0x0000_000A	A=10,B=15 A=14,B=11	0x2F00_000A 0x2B00_000E	A=190	0x3000_00BE
57600	A=22	0x0000_0016	A=22,B=15 A=30,B=11	0x2F00_0016 0x2B00_001E	A=382	0x3000_017E
38400	A=34	0x0000_0022	A=62,B=8 A=46,B=11 A=34,B=15	0x2800_003E 0x2B00_002E 0x2F00_0022	A=574	0x3000_023E
19200	A=70	0x0000_0046	A=126,B=8 A=94,B=11 A=70,B=15	0x2800_007E 0x2B00_005E 0x2F00_0046	A=1150	0x3000_047E
9600	A=142	0x0000_008E	A=254,B=8 A=190,B=11 A=142,B=15	0x2800_00FE 0x2B00_00BE 0x2F00_008E	A=2302	0x3000_08FE
4800	A=286	0x0000_011E	A=510,B=8 A=382,B=11 A=286,B=15	0x2800_01FE 0x2B00_017E 0x2F00_011E	A=4606	0x3000_11FE

Table 5-7 UART Baud Rate Setting Table

The UART0 and UART1 controllers support auto-flow control function that uses two low-level signals, /CTS (clear-to-send) and /RTS (request-to-send), to control the flow of data transfer between the UART and external devices (ex: Modem). When auto-flow is enabled, the UART is not allowed to receive data until the UART asserts /RTS to external device. When the number of bytes in the RX FIFO equals the value of RTS_TRI_LEV (UA_FCR [19:16]), the /RTS is de-asserted. The UART sends data out when UART controller detects /CTS is asserted from external device. If a valid asserted /CTS is not detected the UART controller will not send data out.

The UART controllers also provides Serial IrDA (SIR, Serial Infrared) function (User must set IrDA_EN (UA_FUN_SEL [1]) to enable IrDA function). The SIR specification defines a short-range infrared asynchronous serial transmission mode with one start bit, 8 data bits, and 1 stop bit. The maximum data rate is 115.2 Kbps (half duplex). The IrDA SIR block contains an IrDA SIR Protocol encoder/decoder. The IrDA SIR protocol is half-duplex only. So it cannot transmit and receive data at the same time. The IrDA SIR physical layer specifies a minimum 10ms transfer delay between transmission and reception. This delay feature must be implemented by software.

For NuMicro™ NUC100/NUC120 Low Density, another alternate function of UART controllers is RS-485 9-bit mode function, and direction control provided by RTS pin or can program GPIO (PB.2 for RTS0 and PB.6 for RTS1) to implement the function by software. The RS-485 mode is selected by setting the UA_FUN_SEL register to select RS-485 function. The RS-485 driver control is implemented using the RTS control signal from an asynchronous serial port to enable the RS-485 driver. In RS-485 mode, many characteristics of the RX and TX are same as UART.

5.14 I²S Controller (I²S)

5.14.1 Overview

The I²S controller consists of IIS protocol to interface with external audio CODEC. Two 8 word deep FIFO for read path and write path respectively and is capable of handling 8 ~ 32 bit word sizes. DMA controller handles the data movement between FIFO and memory.

5.14.2 Features

- I²S can operate as either master or slave
- Capable of handling 8-, 16-, 24- and 32-bit word sizes
- Mono and stereo audio data supported
- I²S and MSB justified data format supported
- Two 8 word FIFO data buffers are provided, one for transmit and one for receive
- Generates interrupt requests when buffer levels cross a programmable boundary
- Two DMA requests, one for transmit and one for receive

7.2 DC Electrical Characteristics

7.2.1 NuMicro™ NUC100/NUC120 Medium Density DC Electrical Characteristics

(V_{DD}-V_{SS}=3.3 V, TA = 25°C, FOSC = 50 MHz unless otherwise specified.)

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Operation voltage	V_{DD}	2.5		5.5	V	V_{DD} =2.5 V ~ 5.5 V up to 50 MHz
Power Ground	V_{SS} AV_{SS}	-0.3			V	
LDO Output Voltage	V_{LDO}	-10%	2.5	+10%	V	V_{DD} > 2.7 V
Analog Operating Voltage	AV_{DD}	0		V_{DD}	V	
Analog Reference Voltage	Vref	0		AV_{DD}	V	
Operating Current Normal Run Mode @ 50 MHz	I_{DD1}		54		mA	V_{DD} = 5.5 V@50 MHz, enable all IP and PLL, XTAL=12 MHz
	I_{DD2}		31		mA	V_{DD} = 5.5 V@ 50 MHz, disable all IP and enable PLL, XTAL=12 MHz
	I_{DD3}		51		mA	V_{DD} = 3 V@50 MHz, enable all IP and PLL, XTAL=12 MHz
	I_{DD4}		28		mA	V_{DD} = 3 V@50 MHz, disable all IP and enable PLL, XTAL=12 MHz
Operating Current Normal Run Mode @ 12 MHz	I_{DD5}		22		mA	V_{DD} = 5.5 V@12 MHz, enable all IP and disable PLL, XTAL=12 MHz
	I_{DD6}		14		mA	V_{DD} = 5.5 V@12 MHz, disable all IP and disable PLL, XTAL=12 MHz
	I_{DD7}		20		mA	V_{DD} = 3 V@12MHz, enable all IP and disable PLL, XTAL=12 MHz

Note:

1. /RESET pin is a Schmitt trigger input.

2. Crystal Input is a CMOS input.

3. Pins of PA, PB, PC, PD and PE can source a transition current when they are being externally driven from 1 to 0. In the condition of V_{DD}=5.5 V, 5he transition current reaches its maximum value when V_{IN} approximates to 2 V.

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
	I_{DD8}		11.5		mA	V_{DD} = 3 V@12 MHz, disable all IP and disable PLL, XTAL=12 MHz
Operating Current Normal Run Mode @ 4 MHz	I_{DD9}		13.5		mA	V_{DD} = 5 V@4 MHz, enable all IP and disable PLL, XTAL=4 MHz
	I_{DD10}		10		mA	V_{DD} = 5 V@4 MHz, disable all IP and disable PLL, XTAL=4 MHz
	I_{DD11}		12		mA	V_{DD} = 3 V@4 MHz, enable all IP and disable PLL, XTAL=4 MHz
	I_{DD12}		8		mA	V_{DD} = 3 V@4 MHz, disable all IP and disable PLL, XTAL=4 MHz
Operating Current Idle Mode @ 50 MHz	I_{IDLE1}		30		mA	V_{DD}= 5.5 V@50 MHz, enable all IP and PLL, XTAL=12 MHz
	I_{IDLE2}		13		mA	VDD=5.5 V@50 MHz, disable all IP and enable PLL, XTAL=12 MHz
	I_{IDLE3}		28		mA	V_{DD} = 3 V@50 MHz, enable all IP and PLL, XTAL=12 MHz
	I_{IDLE4}		12		mA	V_{DD} = 3 V@50 MHz, disable all IP and enable PLL, XTAL=12 MHz
Operating Current Idle Mode @ 12 MHz	I_{IDLE5}		11		mA	V_{DD} = 5.5 V@12 MHz, enable all IP and disable PLL, XTAL=12 MHz
	I_{IDLE6}		5		mA	V_{DD} = 5.5 V@12 MHz, disable all IP and disable PLL, XTAL=12 MHz
	I_{IDLE7}		10		mA	V_{DD} = 3 V@12 MHz, enable all IP and disable PLL, XTAL=12 MHz

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Bandgap voltage	V_{BG}	1.20	1.26	1.32	V	V_{DD} = 2.5 V~5.5 V

Note:

1. /RESET pin is a Schmitt trigger input.

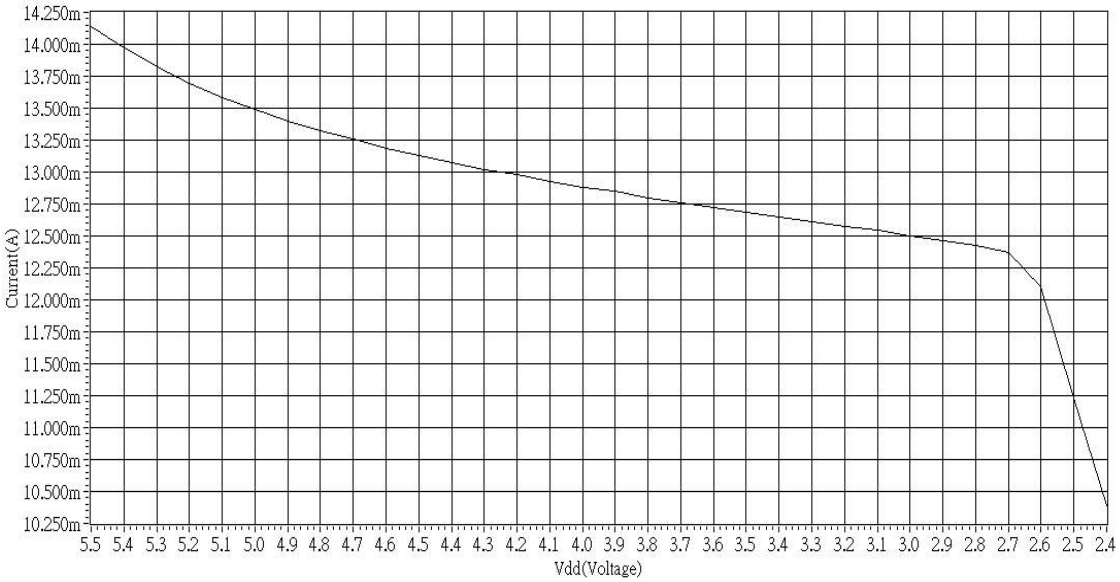
2. Crystal Input is a CMOS input.

3. Pins of PA, PB, PC, PD and PE can source a transition current when they are being externally driven from 1 to 0. In the condition of V_{DD}=5.5 V, 5he transition current reaches its maximum value when V_{IN} approximates to 2 V.

7.2.3 Operating Current Curve (Test condition: run NOP)

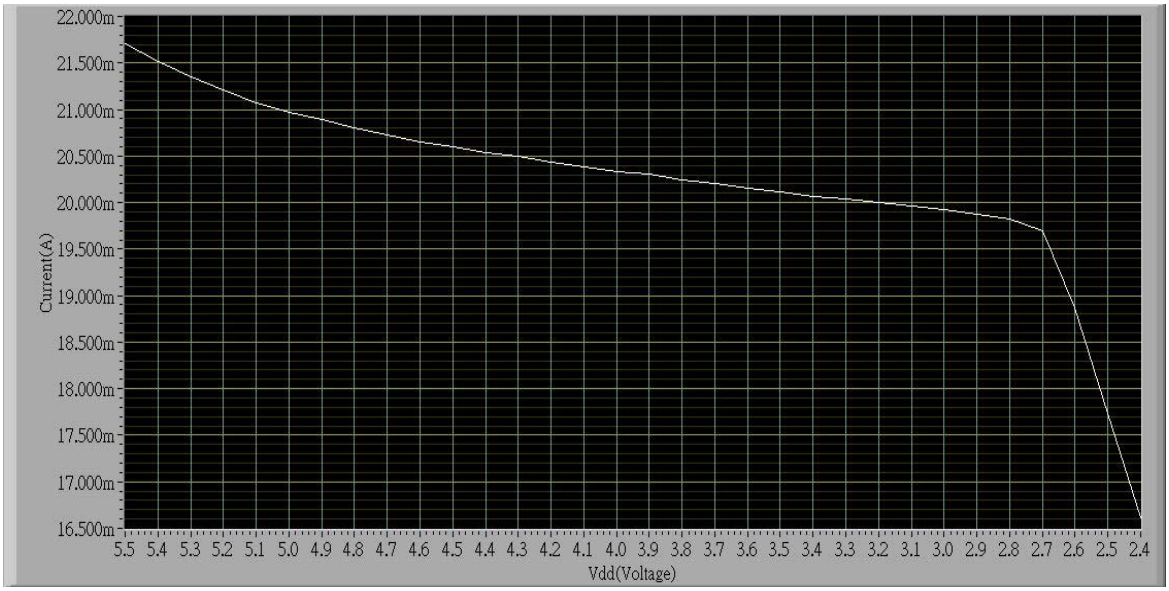
1. XTAL clock = 12 MHz, PLL disable, all-IP disable:

Unit: mA



2. XTAL clock = 12 MHz, PLL disable, all-IP enable

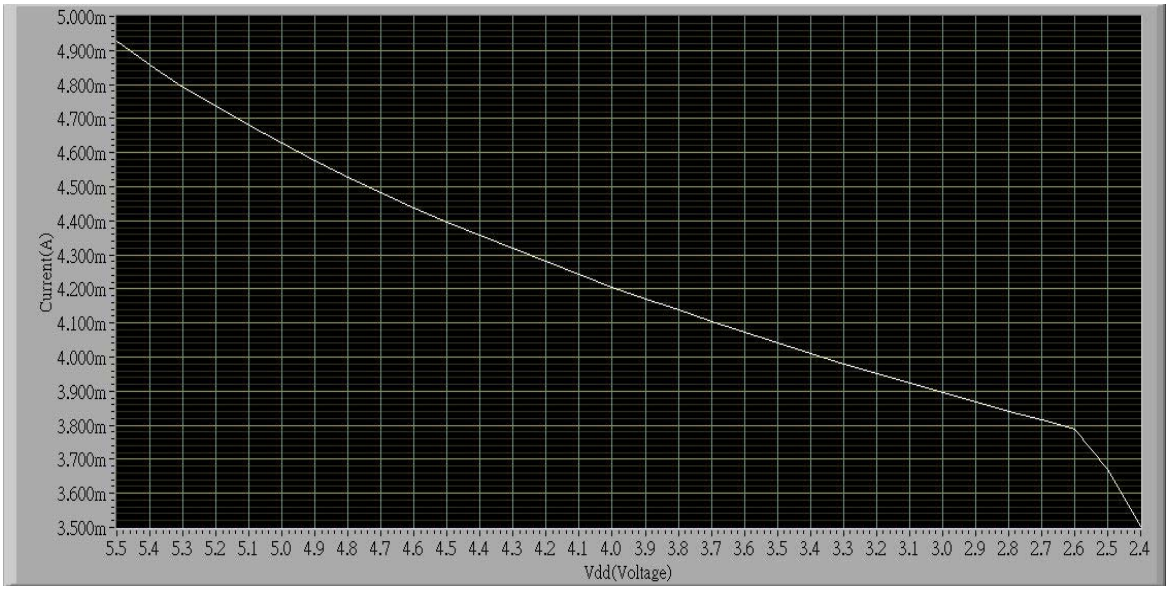
Unit: mA



7.2.4 Idle Current Curve

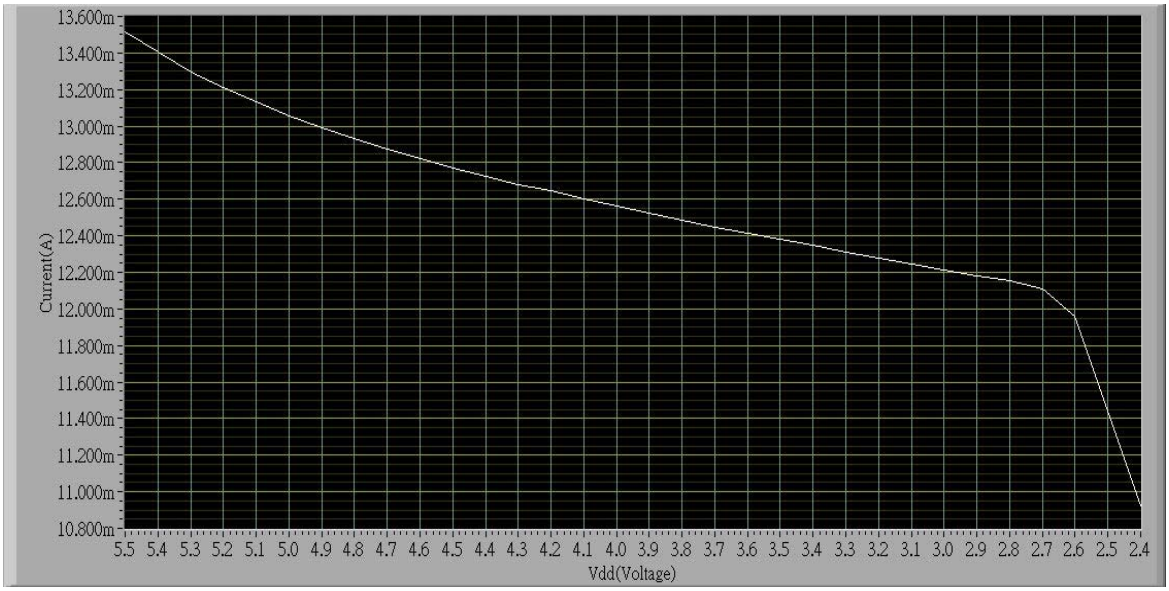
1. XTAL clock = 12 MHz, PLL disable, all-IP disable

Unit: mA



2. XTAL clock = 12 MHz, PLL disable, all-IP enable

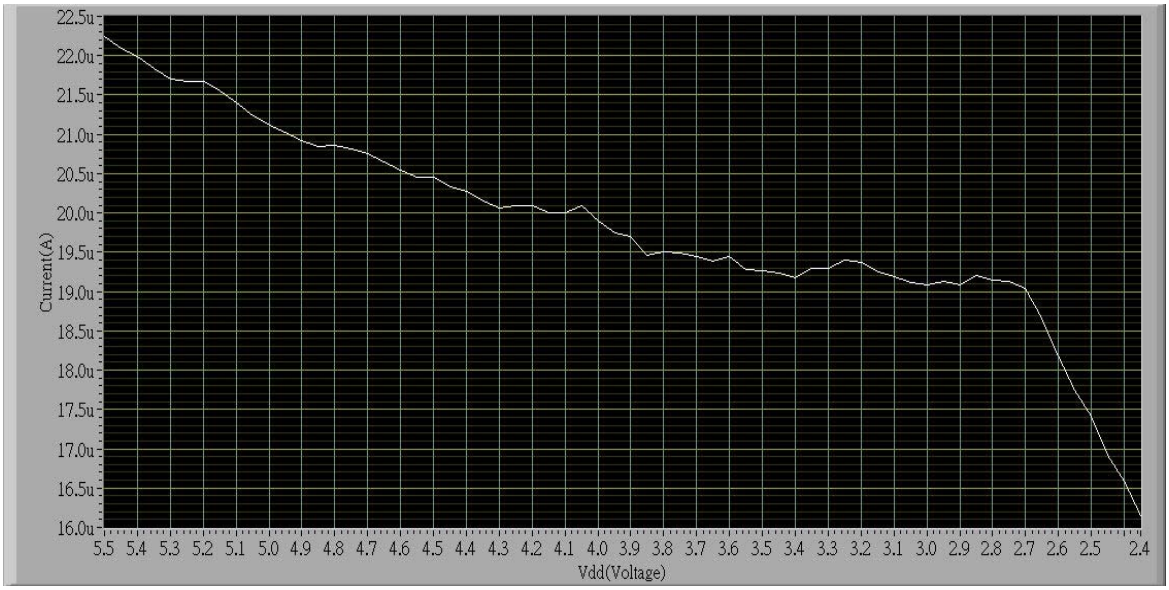
Unit: mA



7.2.5 Power Down Current Curve

XTAL clock = 12 MHz, PLL Disable

Unit: mA



7.4.8 Specification of USB PHY

7.4.8.1 USB DC Electrical Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input high (driven)		2.0			V
V_{IL}	Input low				0.8	V
V_{DI}	Differential input sensitivity	|PADP-PADM|	0.2			V
V_{CM}	Differential common-mode range	Includes V_{DI} range	0.8		2.5	V
V_{SE}	Single-ended receiver threshold		0.8		2.0	V
	Receiver hysteresis			200		mV
V_{OL}	Output low (driven)		0		0.3	V
V_{OH}	Output high (driven)		2.8		3.6	V
V_{CRS}	Output signal cross voltage		1.3		2.0	V
R_{PU}	Pull-up resistor		1.425		1.575	kΩ
V_{TRM}	Termination Voltage for upstream port pull up (RPU)		3.0		3.6	V
Z_{DRV}	Driver output resistance	Steady state drive*		10		Ω
C_{IN}	Transceiver capacitance	Pin to GND			20	pF

*Driver output resistance doesn't include series resistor resistance.

7.4.8.2 USB Full-Speed Driver Electrical Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
T_{FR}	Rise Time	C_L=50p	4		20	ns
T_{FF}	Fall Time	C_L=50p	4		20	ns
T_{FRFF}	Rise and fall time matching	$T_{FRFF}=T_{FR}/T_{FF}$	90		111.11	%

7.4.8.3 USB Power Dissipation

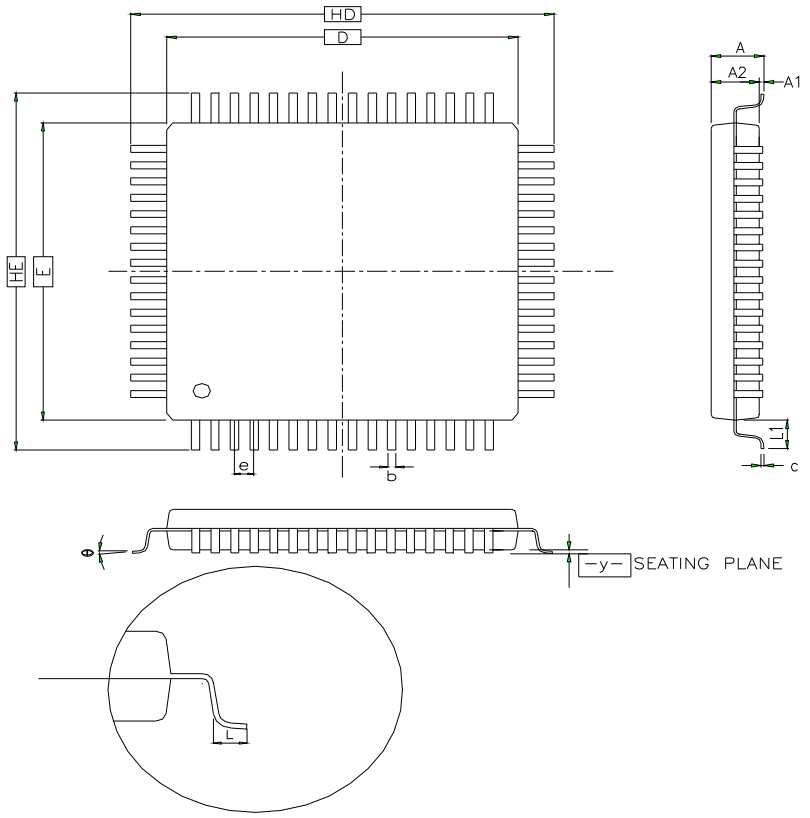
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{VDDREG} (Full Speed)	VDDD and VDDREG Supply Current (Steady State)	Standby		50		uA
		Input mode				uA
		Output mode				uA

7.5 Flash DC Electrical Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
N_{endu}	Endurance		10000			cycles[1]
T_{ret}	Retention time	Temp=25 ℃	100			year
T_{erase}	Page erase time		20		40	ms
T_{mass}	Mass erase time		40	50	60	ms
T_{prog}	Program time		35	40	55	us
V_{dd}	Supply voltage		2.25	2.5	2.75	V[2]
I_{dd1}	Read current				14	mA
I_{dd2}	Program/Erase current				7	mA
I_{pd}	Power down current				10	uA

1. Number of program/erase cycles.
2. V_{dd} is source from chip LDO output voltage.
3. This table is guaranteed by design, not test in production.

8.2 64L LQFP (10x10x1.4mm footprint 2.0 mm)



Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	—	—	0.063	—	—	1.60
A_1	0.002	—	0.006	0.05	—	0.15
A_2	0.053	0.055	0.057	1.35	1.40	1.45
b	0.007	0.008	0.011	0.17	0.20	0.27
c	0.004	—	0.008	0.09	—	0.20
D	—	0.393	—	—	10.00	—
E	—	0.393	—	—	10.00	—
e	—	0.020	—	—	0.50	—
H_D	—	0.472	—	—	12.00	—
H_E	—	0.472	—	—	12.00	—
L	0.018	0.024	0.030	0.45	0.60	0.75
L_1	—	0.039	—	—	1.00	—
y	—	0.004	—	—	0.10	—
θ	0°	3.5°	7°	0°	3.5°	7°