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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	EBI/EMI, I ² C, IrDA, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I ² S, LVD, POR, PS2, PWM, WDT
Number of I/O	45
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 5.5V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/nuc120rd3an

Contents

1	GENERAL DESCRIPTION	7
2	FEATURES	8
2.1	NuMicro™ NUC120 Features – USB Line	8
3	PARTS INFORMATION LIST AND PIN CONFIGURATION	12
3.1	NuMicro™ NUC120 Products Selection Guide	12
3.1.1	NuMicro™ NUC120 Medium Density USB Line Selection Guide.....	12
3.1.2	NuMicro™ NUC120 Low Density USB Line Selection Guide.....	12
3.2	Pin Configuration	14
3.2.1	NuMicro™ NUC120 Medium Density Pin Diagram	14
3.2.2	NuMicro™ NUC120 Low Density Pin Diagram	17
4	BLOCK DIAGRAM	19
4.1	NuMicro™ NUC120 Medium Density Block Diagram	19
4.2	NuMicro™ NUC120 Low Density Block Diagram.....	20
5	FUNCTIONAL DESCRIPTION.....	21
5.1	ARM® Cortex™-M0 Core	21
5.2	System Manager.....	23
5.2.1	Overview	23
5.2.2	System Reset	23
5.2.3	System Power Distribution	24
5.2.4	System Memory Map.....	25
5.2.5	System Timer (SysTick)	27
5.2.6	Nested Vectored Interrupt Controller (NVIC).....	28
5.3	Clock Controller	32
5.3.1	Overview	32
5.3.2	Clock Generator	34
5.3.3	System Clock and SysTick Clock	35
5.3.4	Peripherals Clock	36
5.3.5	Power Down Mode Clock	36
5.3.6	Frequency Divider Output.....	37
5.4	USB Device Controller (USB).....	38
5.4.1	Overview	38
5.4.2	Features	38
5.5	General Purpose I/O (GPIO)	39
5.5.1	Overview	39
5.5.2	Features	39
5.6	I ² C Serial Interface Controller (Master/Slave) (I ² C)	40
5.6.1	Overview	40
5.6.2	Features	41
5.7	PWM Generator and Capture Timer (PWM)	42
5.7.1	Overview	42

	5.7.2 Features	43
5.8	Real Time Clock (RTC).....	44
	5.8.1 Overview	44
	5.8.2 Features	44
5.9	Serial Peripheral Interface (SPI).....	45
	5.9.1 Overview	45
	5.9.2 Features	45
5.10	Timer Controller (TMR).....	46
	5.10.1 Overview	46
	5.10.2 Features	46
5.11	Watchdog Timer (WDT).....	47
	5.11.1 Overview	47
	5.11.2 Features	49
5.12	UART Interface Controller (UART)	49
	5.12.1 Overview	49
	5.12.2 Features	51
5.13	PS/2 Device Controller (PS2D).....	52
	5.13.1 Overview	52
	5.13.2 Features	52
5.14	I ² S Controller (I ² S).....	53
	5.14.1 Overview	53
	5.14.2 Features	53
5.15	Analog-to-Digital Converter (ADC)	54
	5.15.1 Overview	54
	5.15.2 Features	54
5.16	Analog Comparator (CMP)	55
	5.16.1 Overview	55
	5.16.2 Features	55
5.17	PDMA Controller (PDMA).....	56
	5.17.1 Overview	56
	5.17.2 Features	56
5.18	External Bus Interface (EBI)	57
	5.18.1 Overview	57
	5.18.2 Features	57
6	FLASH MEMORY CONTROLLER (FMC)	58
	6.1 Overview	58
	6.2 Features	58
7	ELECTRICAL CHARACTERISTICS	59
	7.1 Absolute Maximum Ratings	59
	7.2 DC Electrical Characteristics	60
	7.2.1 NuMicro™ NUC100/NUC120 Medium Density DC Electrical Characteristics	60
	7.2.2 NuMicro™ NUC100/NUC120 Low Density DC Electrical Characteristics	65

Figures

Figure 3-1 NuMicro™ NUC100 Series selection code	13
Figure 3-2 NuMicro™ NUC120 Medium Density LQFP 100-pin Pin Diagram	14
Figure 3-3 NuMicro™ NUC120 Medium Density LQFP 64-pin Pin Diagram	15
Figure 3-4 NuMicro™ NUC120 Medium Density LQFP 48-pin Pin Diagram	16
Figure 3-5 NuMicro™ NUC120 Low Density LQFP 64-pin Pin Diagram.....	17
Figure 3-6 NuMicro™ NUC120 Low Density LQFP 48-pin Pin Diagram.....	18
Figure 4-1 NuMicro™ NUC120 Medium Density Block Diagram	19
Figure 4-2 NuMicro™ NUC120 Low Density Block Diagram	20
Figure 5-1 Functional Controller Diagram	21
Figure 5-2 NuMicro™ NUC120 Power Distribution Diagram.....	24
Figure 5-4 Clock generator global view diagram	33
Figure 5-5 Clock generator block diagram	34
Figure 5-6 System Clock Block Diagram	35
Figure 5-7 SysTick Clock Control Block Diagram	35
Figure 5-8 Clock Source of Frequency Divider	37
Figure 5-9 Block Diagram of Frequency Divider	37
Figure 5-10 I ² C Bus Timing	40
Figure 5-11 Timing of Interrupt and Reset Signal	48
Figure 7-1 Typical Crystal Application Circuit	76
Figure 7-2 SPI Master dynamic characteristics timing.....	84
Figure 7-3 SPI Slave dynamic characteristics timing.....	84



- ADC

- 12-bit SAR ADC with 600K SPS
- Up to 8-ch single-end input or 4-ch differential input
- Single scan/single cycle scan/continuous scan
- Each channel with individual result register
- Scan on enabled channels
- Threshold voltage detection
- Conversion start by software programming or external input
- Support PDMA mode

- Analog Comparator

- Up to two analog comparators
- External input or internal bandgap voltage selectable at negative node
- Interrupt when compare result change
- Power down wake-up

- One built-in temperature sensor with 1°C resolution

- Brown-Out detector

- With 4 levels: 4.5 V/3.8 V/2.7 V/2.2 V
- Support Brown-Out Interrupt and Reset option

- Low Voltage Reset

- Threshold voltage levels: 2.0 V

- Operating Temperature: -40°C~85°C

- Packages:

- All Green package (RoHS)
- LQFP 100-pin / 64-pin / 48-pin (100-pin for NuMicro™ NUC100/NUC120 Medium Density Only)

3.2.2 NuMicro™ NUC120 Low Density Pin Diagram

3.2.2.1 NuMicro™ NUC120 Low Density LQFP 64 pin

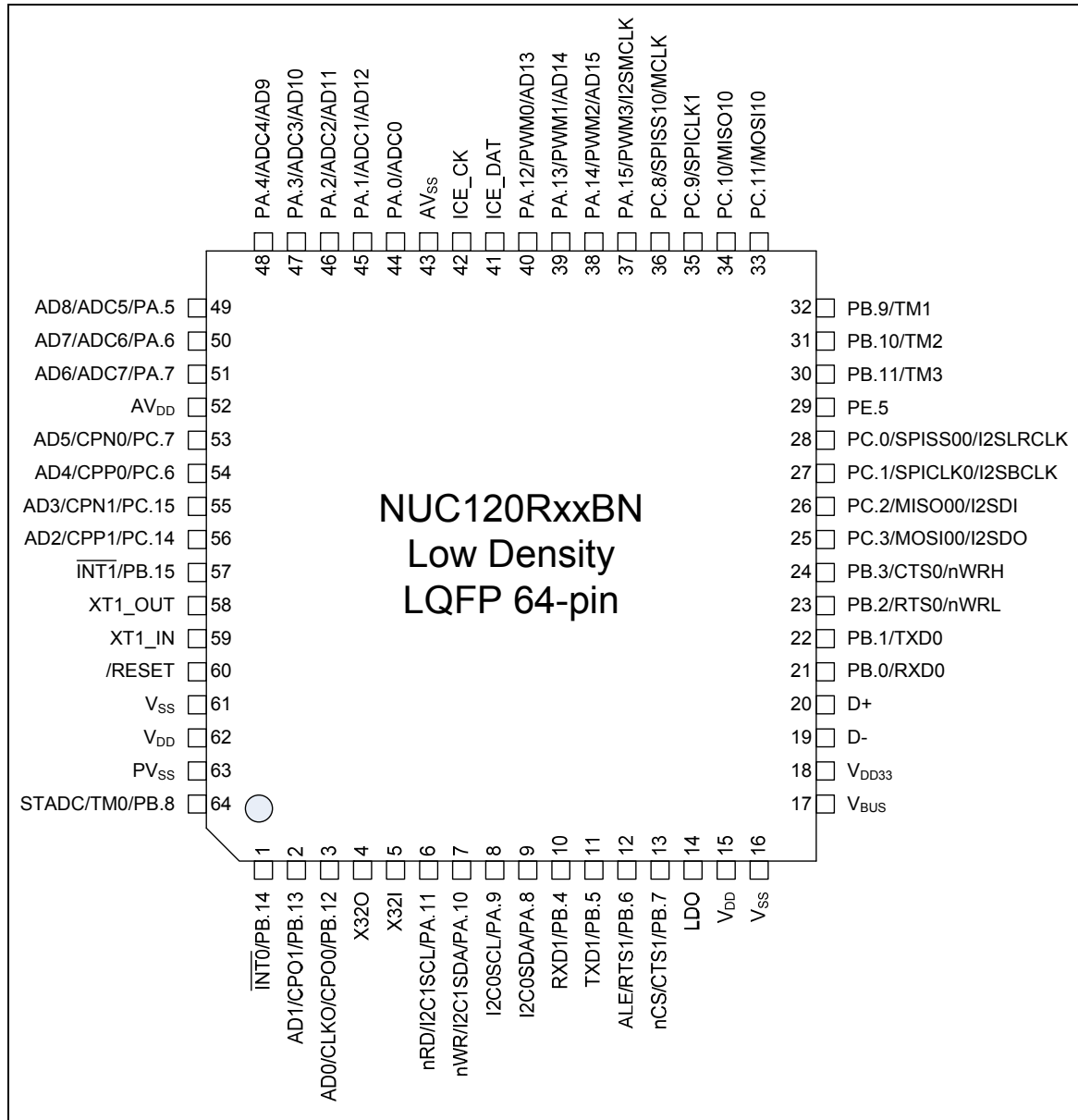


Figure 3-5 NuMicro™ NUC120 Low Density LQFP 64-pin Pin Diagram

- ◆ Low power sleep mode entry using Wait For Interrupt (WFI), Wait For Event (WFE) instructions, or the return from interrupt sleep-on-exit feature
- NVIC that features:
 - ◆ 32 external interrupt inputs, each with four levels of priority
 - ◆ Dedicated Non-Maskable Interrupt (NMI) input.
 - ◆ Support for both level-sensitive and pulse-sensitive interrupt lines
 - ◆ Wake-up Interrupt Controller (WIC), providing ultra-low power sleep mode support.
- Debug support
 - ◆ Four hardware breakpoints.
 - ◆ Two watchpoints.
 - ◆ Program Counter Sampling Register (PCSR) for non-intrusive code profiling.
 - ◆ Single step and vector catch capabilities.
- Bus interfaces:
 - ◆ Single 32-bit AMBA-3 AHB-Lite system interface that provides simple integration to all system peripherals and memory.
 - ◆ Single 32-bit slave port that supports the DAP (Debug Access Port).

Address Space	Token	Controllers
0x400E_0000 – 0x400E_FFFF	ADC_BA	Analog-Digital-Converter (ADC) Control Registers
APB2 Controllers Space (0x4010_0000 ~ 0x401F_FFFF)		
0x4010_0000 – 0x4010_3FFF	PS2_BA	PS/2 Interface Control Registers
0x4011_0000 – 0x4011_3FFF	TMR23_BA	Timer2/Timer3 Control Registers
0x4012_0000 – 0x4012_3FFF	I2C1_BA	I ² C1 Interface Control Registers
0x4013_0000 – 0x4013_3FFF	SPI2_BA	SPI2 with master/slave function Control Registers (NuMicro™ NUC100/NUC120 Medium Density Only)
0x4013_4000 – 0x4013_7FFF	SPI3_BA	SPI3 with master/slave function Control Registers (NuMicro™ NUC100/NUC120 Medium Density Only)
0x4014_0000 – 0x4014_3FFF	PWMB_BA	PWM4/5/6/7 Control Registers (NuMicro™ NUC100/NUC120 Medium Density Only)
0x4015_0000 – 0x4015_3FFF	UART1_BA	UART1 Control Registers
0x4015_4000 – 0x4015_7FFF	UART2_BA	UART2 Control Registers (NuMicro™ NUC100/NUC120 Medium Density Only)
0x401A_0000 – 0x401A_3FFF	I2S_BA	I ² S Interface Control Registers
System Controllers Space (0xE000_E000 ~ 0xE000_EFFF)		
0xE000_E010 – 0xE000_E0FF	SCS_BA	System Timer Control Registers
0xE000_E100 – 0xE000_ECFF	SCS_BA	External Interrupt Controller Control Registers
0xE000_ED00 – 0xE000_ED8F	SCS_BA	System Control Registers

Table 5-1 Address Space Assignments for On-Chip Controllers

5.2.6 Nested Vectored Interrupt Controller (NVIC)

Cortex-M0 provides an interrupt controller as an integral part of the exception mode, named as “Nested Vectored Interrupt Controller (NVIC)”. It is closely coupled to the processor kernel and provides following features:

- Nested and Vectored interrupt support
- Automatic processor state saving and restoration
- Reduced and deterministic interrupt latency

The NVIC prioritizes and handles all supported exceptions. All exceptions are handled in “Handler Mode”. This NVIC architecture supports 32 (IRQ[31:0]) discrete interrupts with 4 levels of priority. All of the interrupts and most of the system exceptions can be configured to different priority levels. When an interrupt occurs, the NVIC will compare the priority of the new interrupt to the current running one’s priority. If the priority of the new interrupt is higher than the current one, the new interrupt handler will override the current handler.

When any interrupts is accepted, the starting address of the interrupt service routine (ISR) is fetched from a vector table in memory. There is no need to determine which interrupt is accepted and branch to the starting address of the correlated ISR by software. While the starting address is fetched, NVIC will also automatically save processor state including the registers “PC, PSR, LR, R0~R3, R12” to the stack. At the end of the ISR, the NVIC will restore the mentioned registers from stack and resume the normal execution. Thus it will take less and deterministic time to process the interrupt request.

The NVIC supports “Tail Chaining” which handles back-to-back interrupts efficiently without the overhead of states saving and restoration and therefore reduces delay time in switching to pending ISR at the end of current ISR. The NVIC also supports “Late Arrival” which improves the efficiency of concurrent ISRs. When a higher priority interrupt request occurs before the current ISR starts to execute (at the stage of state saving and starting address fetching), the NVIC will give priority to the higher one without delay penalty. Thus it advances the real-time capability.

For more detailed information, please refer to the documents “ARM® Cortex™-M0 Technical Reference Manual” and “ARM® v6-M Architecture Reference Manual”.

Vector Number	Interrupt Number (Bit in Interrupt Registers)	Interrupt Name	Source IP	Interrupt description
26	10	TMR2_INT	TMR2	Timer 2 interrupt
27	11	TMR3_INT	TMR3	Timer 3 interrupt
28	12	UART02_INT	UART0/2	UART0 and UART2 interrupt
29	13	UART1_INT	UART1	UART1 interrupt
30	14	SPI0_INT	SPI0	SPI0 interrupt
31	15	SPI1_INT	SPI1	SPI1 interrupt
32	16	SPI2_INT	SPI2	SPI2 interrupt
33	17	SPI3_INT	SPI3	SPI3 interrupt
34	18	I2C0_INT	I ² C0	I ² C0 interrupt
35	19	I2C1_INT	I ² C1	I ² C1 interrupt
36	20	Reserved	Reserved	Reserved
37	21	Reserved	Reserved	Reserved
38	22	Reserved	Reserved	Reserved
39	23	USB_INT	USBD	USB 2.0 FS Device interrupt
40	24	PS2_INT	PS/2	PS/2 interrupt
41	25	ACMP_INT	ACMP	Analog Comparator-0 or Comaprator-1 interrupt
42	26	PDMA_INT	PDMA	PDMA interrupt
43	27	I2S_INT	I ² S	I ² S interrupt
44	28	PWRWU_INT	CLKC	Clock controller interrupt for chip wake-up from power down state
45	29	ADC_INT	ADC	ADC interrupt
46	30	Reserved	Reserved	Reserved
47	31	RTC_INT	RTC	Real time clock interrupt

Table 5-3 System Interrupt Map

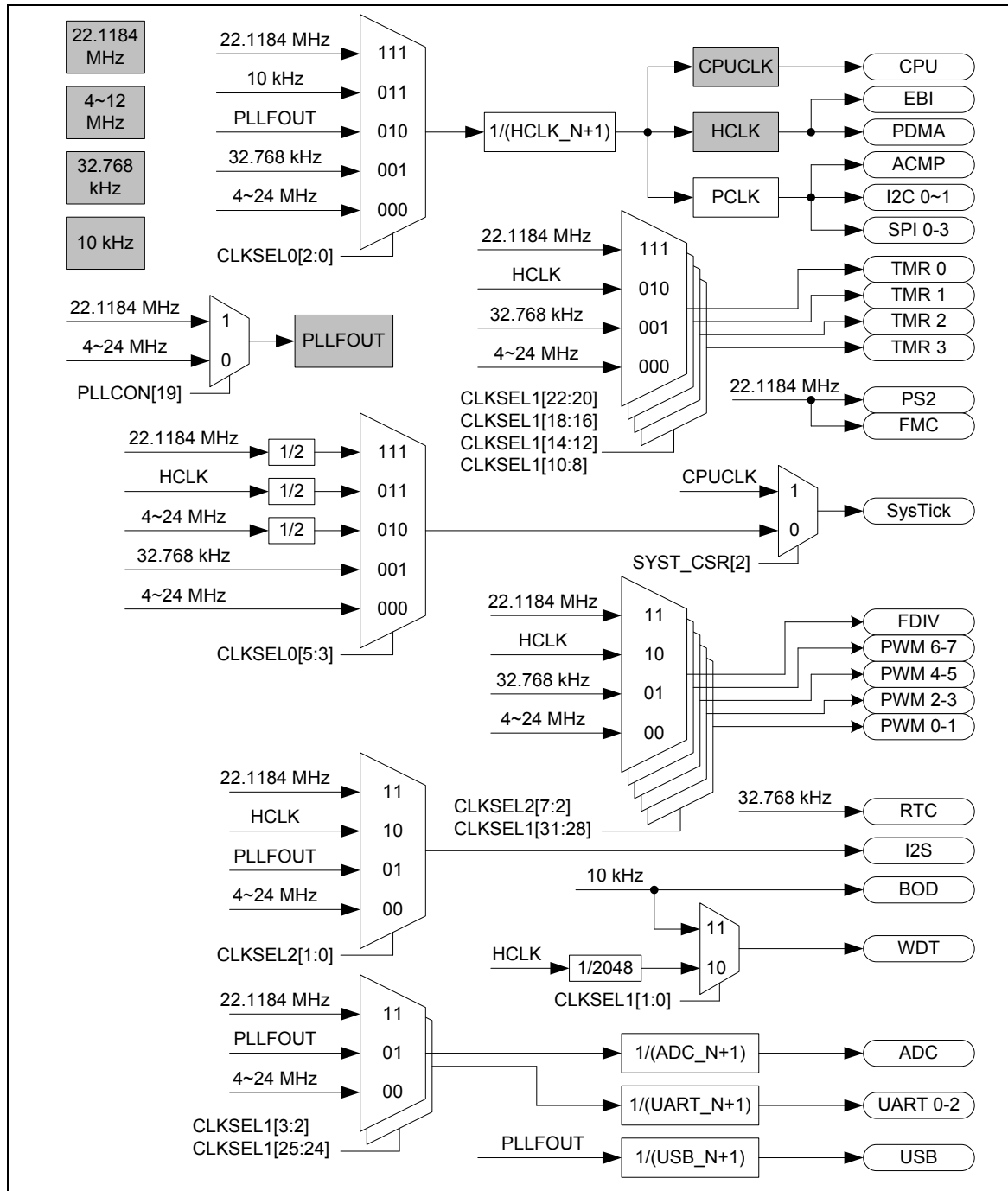


Figure 5-3 Clock generator global view diagram

5.3.3 System Clock and SysTick Clock

The system clock has 5 clock sources which were generated from clock generator block. The clock source switch depends on the register HCLK_S (CLKSEL0[2:0]). The block diagram is showed in Figure 5-5.

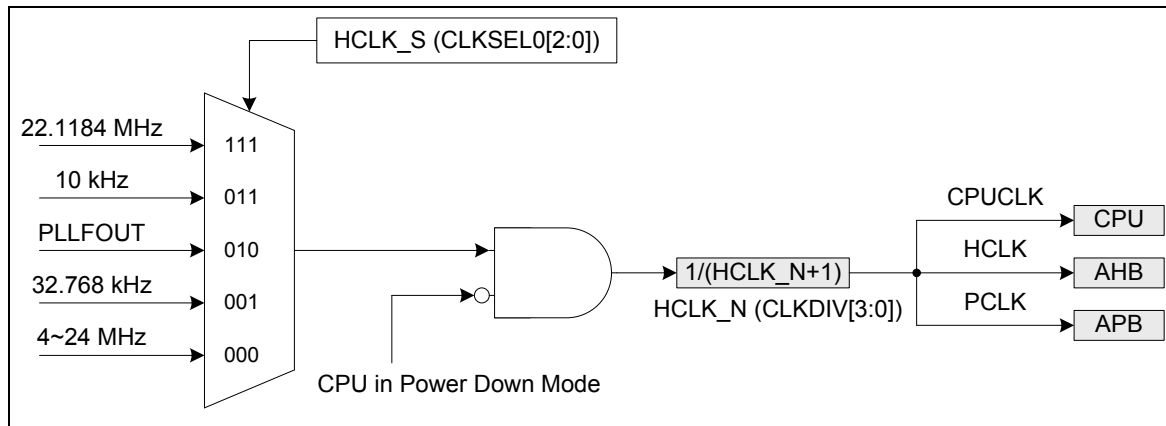


Figure 5-5 System Clock Block Diagram

The clock source of SysTick in Cortex-M0 core can use CPU clock or external clock (SYST_CSR[2]). If using external clock, the SysTick clock (STCLK) has 5 clock sources. The clock source switch depends on the setting of the register STCLK_S (CLKSEL0[5:3]). The block diagram is showed in Figure 5-6.

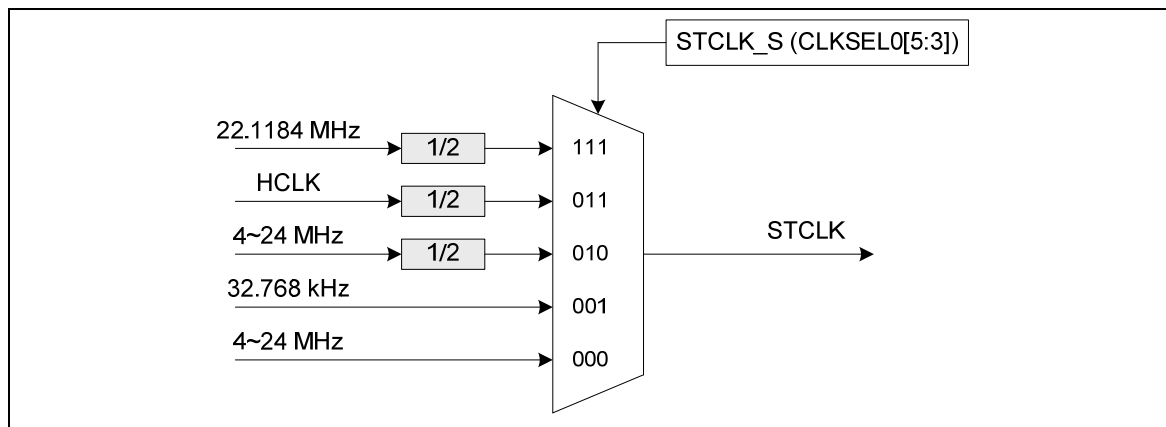


Figure 5-6 SysTick Clock Control Block Diagram

5.10 Timer Controller (TMR)

5.10.1 Overview

The timer controller includes four 32-bit timers, TIMER0~TIMER3, which allows user to easily implement a timer control for applications. The timer can perform functions like frequency measurement, event counting, interval measurement, clock generation, delay timing, and so on. The timer can generate an interrupt signal upon timeout, or provide the current value during operation. Note: toggle mode, continuous counting mode and event counting function only support in NuMicro™ NUC100/NUC120 Low Density.

5.10.2 Features

- 4 sets of 32-bit timers with 24-bit up-timer and one 8-bit pre-scale counter
- Independent clock source for each timer
- Provides one-shot, periodic, toggle and continuous counting operation modes (NuMicro™ NUC100/NUC120 Medium Density only support one-shot and periodic mode)
- Time out period = (Period of timer clock input) * (8-bit pre-scale counter + 1) * (24-bit TCMP)
- Maximum counting cycle time = $(1 / T \text{ MHz}) * (2^8) * (2^{24})$, T is the period of timer clock
- 24-bit timer value is readable through TDR (Timer Data Register)
- Support event counting function to count the event from external pin (NuMicro™ NUC100/NUC120 Low Density only)

5.11.2 Features

- 18-bit free running counter to avoid chip from Watchdog timer reset before the delay time expires.
- Selectable time-out interval ($2^4 \sim 2^{18}$) and the time out interval is 104 ms $\sim$ 26.3168 s (if WDT_CLK = 10 kHz).
- Reset period = (1 / 10 kHz) * 63, if WDT_CLK = 10 kHz.

5.12 UART Interface Controller (UART)

NuMicro™ NUC100/NUC120 Medium Density provides up to three channels of Universal Asynchronous Receiver/Transmitters (UART). UART0 supports High Speed UART and UART1~2 perform Normal Speed UART, besides, only UART0 and UART1 support flow control function. NuMicro™ NUC100/NUC120 Low Density only supports UART0 and UART1.

5.12.1 Overview

The Universal Asynchronous Receiver/Transmitter (UART) performs a serial-to-parallel conversion on data received from the peripheral, and a parallel-to-serial conversion on data transmitted from the CPU. The UART controller also supports IrDA SIR Function and RS-485 mode functions. Each UART channel supports seven types of interrupts including transmitter FIFO empty interrupt (INT_THRE), receiver threshold level reaching interrupt (INT_RDA), line status interrupt (parity error or framing error or break interrupt) (INT_RLS), receiver buffer time out interrupt (INT_TOUT), MODEM/Wake-up status interrupt (INT_MODEM) and Buffer error interrupt (INT_BUF_ERR). Interrupts of UART0 and UART2 share the interrupt number 12 (vector number is 28); Interrupt number 13 (vector number is 29) only supports UART1 interrupt. Refer to Nested Vectored Interrupt Controller chapter for System Interrupt Map.

The UART0 is built-in with a 64-byte transmitter FIFO (TX_FIFO) and a 64-byte receiver FIFO (RX_FIFO) that reduces the number of interrupts presented to the CPU and the UART1~2 are equipped 16-byte transmitter FIFO (TX_FIFO) and 16-byte receiver FIFO (RX_FIFO). The CPU can read the status of the UART at any time during the operation. The reported status information includes the type and condition of the transfer operations being performed by the UART, as well as 4 error conditions (parity error, framing error, break interrupt and buffer error) probably occur while receiving data. The UART includes a programmable baud rate generator that is capable of dividing clock input by divisors to produce the serial clock that transmitter and receiver need. The baud rate equation is Baud Rate = UART_CLK / M * [BRD + 2], where M and BRD are defined in Baud Rate Divider Register (UA_BAUD). Table 5-6 lists the equations in the various conditions and Table 5-7 list the UART baud rate setting table.

Mode	DIV_X_EN	DIV_X_ONE	Divider X	BRD	Baud rate equation
0	0	0	B	A	$\text{UART_CLK} / [16 * (A+2)]$
1	1	0	B	A	$\text{UART_CLK} / [(B+1) * (A+2)]$, B must ≥ 8
2	1	1	Don't care	A	$\text{UART_CLK} / (A+2)$, A must ≥ 3

Table 5-6 UART Baud Rate Equation

5.13 PS/2 Device Controller (PS2D)

5.13.1 Overview

PS/2 device controller provides basic timing control for PS/2 communication. All communication between the device and the host is managed through the CLK and DATA pins. Unlike PS/2 keyboard or mouse device controller, the received/transmit code needs to be translated as meaningful code by firmware. The device controller generates the CLK signal after receiving a request to send, but host has ultimate control over communication. DATA sent from the host to the device is read on the rising edge and DATA sent from device to the host is change after rising edge. A 16 bytes FIFO is used to reduce CPU intervention. S/W can select 1 to 16 bytes for a continuous transmission.

5.13.2 Features

- Host communication inhibit and request to send detection
- Reception frame error detection
- Programmable 1 to 16 bytes transmit buffer to reduce CPU intervention
- Double buffer for data reception
- S/W override bus

5.18 External Bus Interface (EBI)

5.18.1 Overview

The NuMicro™ NUC100/NUC120 Low Density LQFP-64 package equips an external bus interface (EBI) for external device used.

To save the connections between external device and this chip, EBI support address bus and data bus multiplex mode. And, address latch enable (ALE) signal supported differentiate the address and data cycle.

5.18.2 Features

External Bus Interface has the following functions:

- External devices with max. 64K-byte size (8-bit data width)/128K-byte (16-bit data width) supported
- Variable external bus base clock (MCLK) supported
- 8-bit or 16-bit data width supported
- Variable data access time (tACC), address latch enable time (tALE) and address hold time (tAHD) supported
- Address bus and data bus multiplex mode supported to save the address pins
- Configurable idle cycle supported for different access condition: Write command finish (W2X), Read-to-Read (R2R)



7.2 DC Electrical Characteristics

7.2.1 NuMicro™ NUC100/NUC120 Medium Density DC Electrical Characteristics

($V_{DD}-V_{SS}=3.3\text{ V}$, $T_A = 25^\circ\text{C}$, $F_{OSC} = 50\text{ MHz}$ unless otherwise specified.)

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Operation voltage	V_{DD}	2.5		5.5	V	$V_{DD} = 2.5\text{ V} \sim 5.5\text{ V}$ up to 50 MHz
Power Ground	V_{SS} AV_{SS}	-0.3			V	
LDO Output Voltage	V_{LDO}	-10%	2.5	+10%	V	$V_{DD} > 2.7\text{ V}$
Analog Operating Voltage	AV_{DD}	0		V_{DD}	V	
Analog Reference Voltage	V_{ref}	0		AV_{DD}	V	
Operating Current Normal Run Mode @ 50 MHz	I_{DD1}		54		mA	$V_{DD} = 5.5\text{ V}@50\text{ MHz}$, enable all IP and PLL, XTAL=12 MHz
	I_{DD2}		31		mA	$V_{DD} = 5.5\text{ V}@50\text{ MHz}$, disable all IP and enable PLL, XTAL=12 MHz
	I_{DD3}		51		mA	$V_{DD} = 3\text{ V}@50\text{ MHz}$, enable all IP and PLL, XTAL=12 MHz
	I_{DD4}		28		mA	$V_{DD} = 3\text{ V}@50\text{ MHz}$, disable all IP and enable PLL, XTAL=12 MHz
Operating Current Normal Run Mode @ 12 MHz	I_{DD5}		22		mA	$V_{DD} = 5.5\text{ V}@12\text{ MHz}$, enable all IP and disable PLL, XTAL=12 MHz
	I_{DD6}		14		mA	$V_{DD} = 5.5\text{ V}@12\text{ MHz}$, disable all IP and disable PLL, XTAL=12 MHz
	I_{DD7}		20		mA	$V_{DD} = 3\text{ V}@12\text{ MHz}$, enable all IP and disable PLL, XTAL=12 MHz

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Input High Voltage PA, PB, PC, PD, PE (Schmitt input)	V _{IH2}	0.4 V _{DD}	-	V _{DD} +0.5	V	
Hysteresis voltage of PA~PE (Schmitt input)	V _{HY}		0.2 V _{DD}		V	
Input Low Voltage XT1 ^[*2]	V _{IL3}	0	-	0.8	V	V _{DD} = 4.5 V
		0	-	0.4		V _{DD} = 3.0 V
Input High Voltage XT1 ^[*2]	V _{IH3}	3.5	-	V _{DD} +0.2	V	V _{DD} = 5.5 V
		2.4	-	V _{DD} +0.2		V _{DD} = 3.0 V
Input Low Voltage X32I ^[*2]	V _{IL4}	0	-	0.4	V	
Input High Voltage X32I ^[*2]	V _{IH4}	1.7		2.5	V	
Negative going threshold (Schmitt input), /RESET	V _{ILS}	-0.5	-	0.3 V _{DD}	V	
Positive going threshold (Schmitt input), /RESET	V _{IHS}	0.7 V _{DD}	-	V _{DD} +0.5	V	
Source Current PA, PB, PC, PD, PE (Quasi-bidirectional Mode)	I _{SR11}	-300	-370	-450	μA	V _{DD} = 4.5 V, V _S = 2.4 V
	I _{SR12}	-50	-70	-90	μA	V _{DD} = 2.7 V, V _S = 2.2 V
	I _{SR13}	-40	-60	-80	μA	V _{DD} = 2.5 V, V _S = 2.0 V
Source Current PA, PB, PC, PD, PE (Push-pull Mode)	I _{SR21}	-20	-24	-28	mA	V _{DD} = 4.5 V, V _S = 2.4 V
	I _{SR22}	-4	-6	-8	mA	V _{DD} = 2.7 V, V _S = 2.2 V
	I _{SR23}	-3	-5	-7	mA	V _{DD} = 2.5 V, V _S = 2.0 V
Sink Current PA, PB, PC, PD, PE (Quasi-bidirectional and Push-pull Mode)	I _{SK11}	10	16	20	mA	V _{DD} = 4.5 V, V _S = 0.45 V
	I _{SK12}	7	10	13	mA	V _{DD} = 2.7 V, V _S = 0.45 V
	I _{SK13}	6	9	12	mA	V _{DD} = 2.5 V, V _S = 0.45 V
Brown-Out voltage with BOV_VL [1:0] = 00b	V _{BO2.2}	2.1	2.2	2.3	V	
Brown-Out voltage with BOV_VL [1:0] = 01b	V _{BO2.7}	2.6	2.7	2.8	V	
Brown-Out voltage with BOV_VL [1:0] = 10b	V _{BO3.8}	3.6	3.8	4.0	V	
Brown-Out voltage with BOV_VL [1:0] = 11b	V _{BO4.5}	4.3	4.5	4.7	V	
Hysteresis range of BOD voltage	V _{BH}	30	-	150	mV	V _{DD} = 2.5 V~5.5 V



PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Bandgap voltage	V _{BG}	1.20	1.26	1.32	V	V _{DD} = 2.5 V~5.5 V

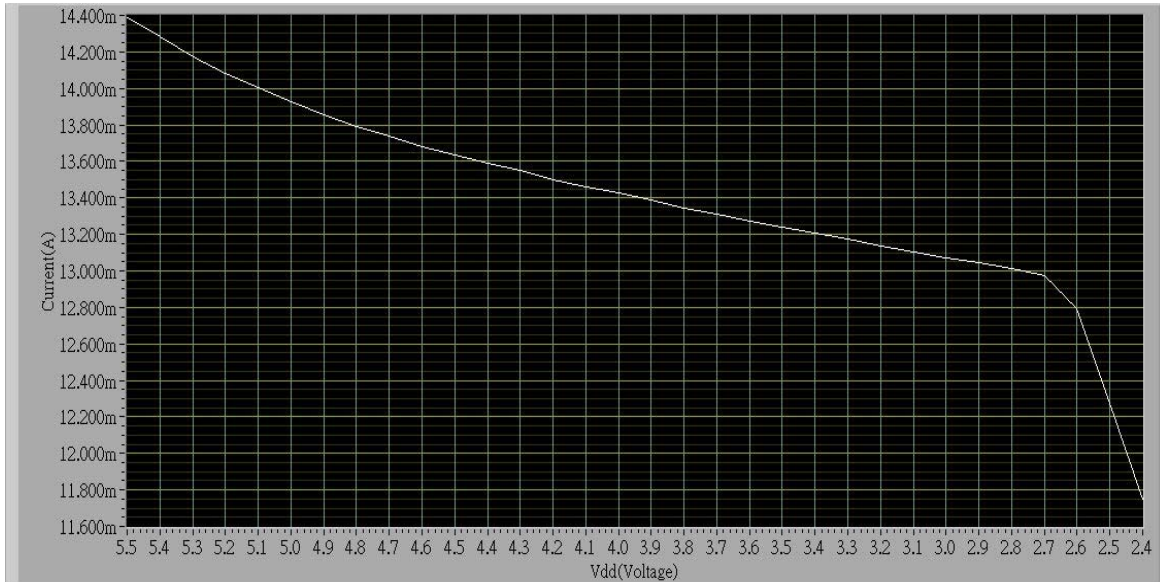
Note:

1. /RESET pin is a Schmitt trigger input.
2. Crystal Input is a CMOS input.
3. Pins of PA, PB, PC, PD and PE can source a transition current when they are being externally driven from 1 to 0. In the condition of V_{DD}=5.5 V, the transition current reaches its maximum value when V_{IN} approximates to 2 V.



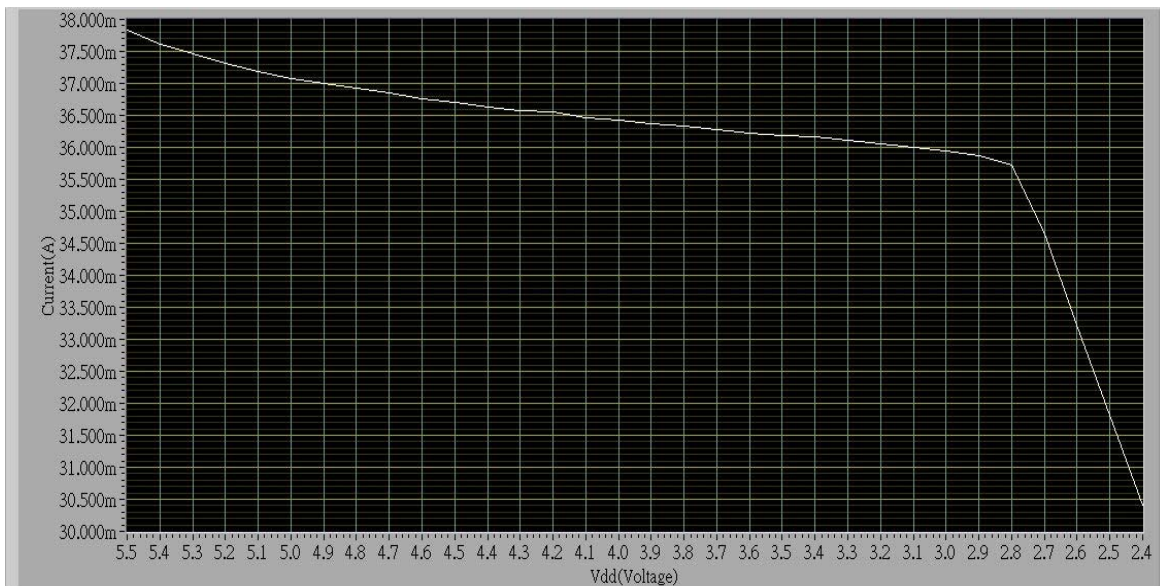
3. XTAL clock = 12 MHz, PLL enable, all-IP disable

Unit: mA



4. XTAL clock = 12 MHz, PLL enable, all-IP enable

Unit: mA



7.4.3 Specification of Low Voltage Reset

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Operation voltage	-	1.7	-	5.5	V
Quiescent current	V _{DD} =5.5 V	-	-	5	μA
Temperature	-	-40	25	85	°C
Threshold voltage	Temperature=25°C	1.7	2.0	2.3	V
	Temperature=-40°C	-	2.4	-	V
	Temperature=85°C	-	1.6	-	V
Hysteresis	-	0	0	0	V

7.4.4 Specification of Brown-Out Detector

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Operation voltage	-	2.5	-	5.5	V
Quiescent current	AV _{DD} =5.5 V	-	-	125	μA
Temperature	-	-40	25	85	°C
Brown-Out voltage	BOV_VL[1:0]=11	4.3	4.5	4.7	V
	BOV_VL [1:0]=10	3.6	3.8	4.0	V
	BOV_VL [1:0]=01	2.6	2.7	2.8	V
	BOV_VL [1:0]=00	2.1	2.2	2.3	V
Hysteresis	-	30	-	150	mV

7.4.5 Specification of Power-On Reset (5 V)

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Temperature	-	-40	25	85	°C
Reset voltage	V+	-	2	-	V
Quiescent current	V _{in} >reset voltage	-	1	-	nA