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Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I ² C, IrDA, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I ² S, LVD, POR, PS2, PWM, WDT
Number of I/O	76
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 5.5V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/nuc120vd3an



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3 PARTS INFORMATION LIST AND PIN CONFIGURATION

3.1 NuMicro™ NUC120 Products Selection Guide

3.1.1 NuMicro™ NUC120 Medium Density USB Line Selection Guide

Part number	APROM	RAM	Data Flash	ISP Loader ROM	I/O	Timer	Connectivity						I ² S	Comp.	PWM	ADC	RTC	EBI	ISP ICP	Package
							UART	SPI	I ² C	USB	LIN	CAN								
NUC120LD3AN	64 KB	16 KB	4 KB	4 KB	up to 31	4x32-bit	2	1	2	1	-	-	1	1	4	8x12-bit	v	-	v	LQFP48
NUC120LE3AN	128 KB	16 KB	Definable	4 KB	up to 31	4x32-bit	2	1	2	1	-	-	1	1	4	8x12-bit	v	-	v	LQFP48
NUC120RD3AN	64 KB	16 KB	4 KB	4 KB	up to 45	4x32-bit	2	2	2	1	-	-	1	2	6	8x12-bit	v	-	v	LQFP64
NUC120RE3AN	128 KB	16 KB	Definable	4 KB	up to 45	4x32-bit	2	2	2	1	-	-	1	2	6	8x12-bit	v	-	v	LQFP64
NUC120VD2AN	64 KB	8 KB	4 KB	4 KB	up to 76	4x32-bit	3	4	2	1	-	-	1	2	8	8x12-bit	v	-	v	LQFP100
NUC120VD3AN	64 KB	16 KB	4 KB	4 KB	up to 76	4x32-bit	3	4	2	1	-	-	1	2	8	8x12-bit	v	-	v	LQFP100
NUC120VE3AN	128 KB	16 KB	Definable	4 KB	up to 76	4x32-bit	3	4	2	1	-	-	1	2	8	8x12-bit	v	-	v	LQFP100

3.1.2 NuMicro™ NUC120 Low Density USB Line Selection Guide

Part number	APROM	RAM	Data Flash	ISP Loader ROM	I/O	Timer	Connectivity						I ² S	Comp.	PWM	ADC	RTC	EBI	ISP ICP	Package
							UART	SPI	I ² C	USB	LIN	CAN								
NUC120LC1BN	32 KB	4 KB	4 KB	4 KB	up to 31	4x32-bit	2	1	2	1	-	-	1	1	4	8x12-bit	v	-	v	LQFP48
NUC120LD1BN	64 KB	4 KB	4 KB	4 KB	up to 31	4x32-bit	2	1	2	1	-	-	1	1	4	8x12-bit	v	-	v	LQFP48
NUC120LD2BN	64 KB	8 KB	4 KB	4 KB	up to 31	4x32-bit	2	1	2	1	-	-	1	1	4	8x12-bit	v	-	v	LQFP48
NUC120RC1BN	32 KB	4 KB	4 KB	4 KB	up to 45	4x32-bit	2	2	2	1	-	-	1	2	4	8x12-bit	v	v	v	LQFP64
NUC120RD1BN	64 KB	4 KB	4 KB	4 KB	up to 45	4x32-bit	2	2	2	1	-	-	1	2	4	8x12-bit	v	v	v	LQFP64
NUC120RD2BN	64 KB	8 KB	4 KB	4 KB	up to 45	4x32-bit	2	2	2	1	-	-	1	2	4	8x12-bit	v	v	v	LQFP64

3.2.2.2 NuMicro™ NUC120 Low Density LQFP 48 pin

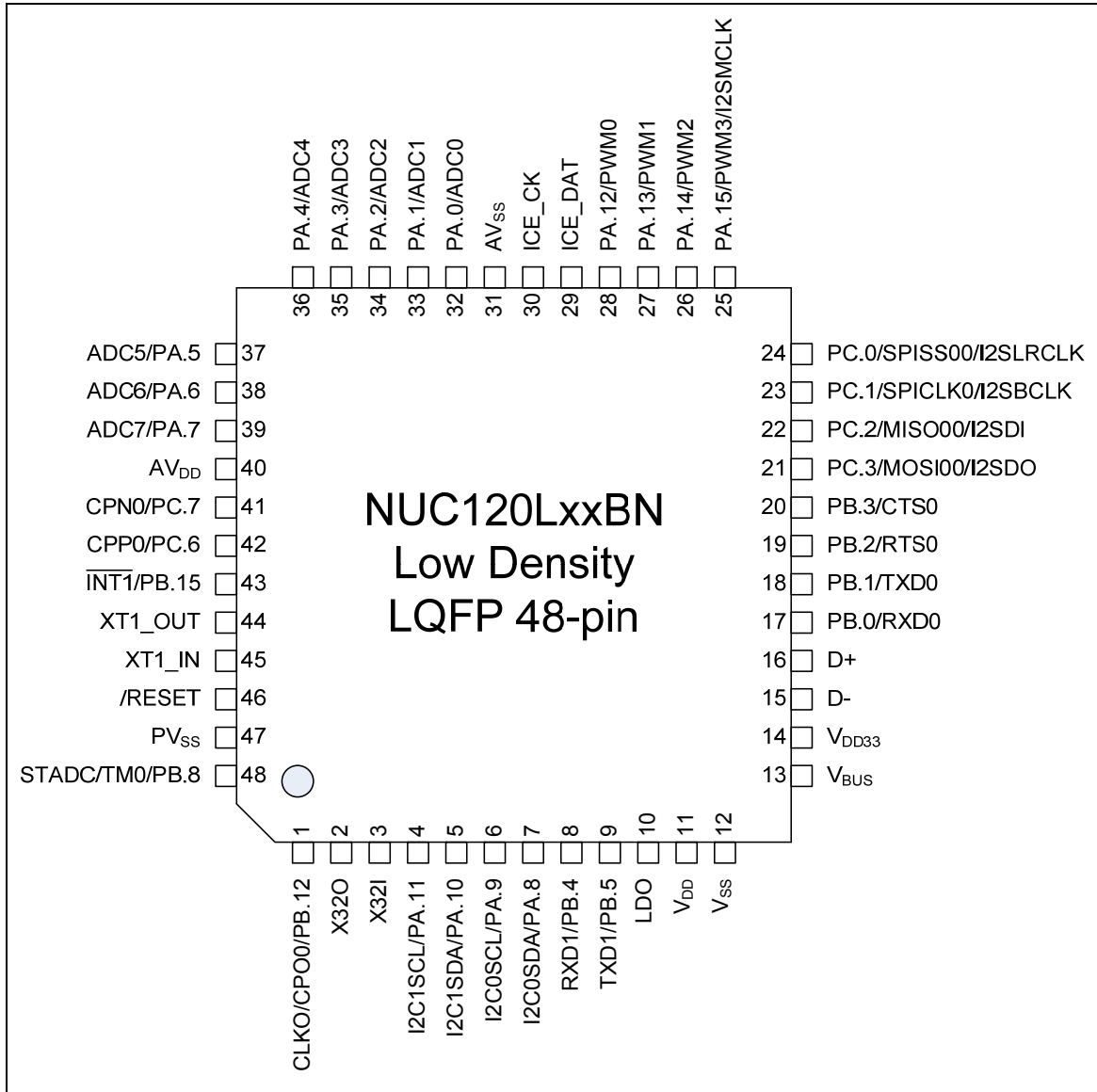


Figure 3-6 NuMicro™ NUC120 Low Density LQFP 48-pin Pin Diagram

- ◆ Low power sleep mode entry using Wait For Interrupt (WFI), Wait For Event (WFE) instructions, or the return from interrupt sleep-on-exit feature
- NVIC that features:
 - ◆ 32 external interrupt inputs, each with four levels of priority
 - ◆ Dedicated Non-Maskable Interrupt (NMI) input.
 - ◆ Support for both level-sensitive and pulse-sensitive interrupt lines
 - ◆ Wake-up Interrupt Controller (WIC), providing ultra-low power sleep mode support.
- Debug support
 - ◆ Four hardware breakpoints.
 - ◆ Two watchpoints.
 - ◆ Program Counter Sampling Register (PCSR) for non-intrusive code profiling.
 - ◆ Single step and vector catch capabilities.
- Bus interfaces:
 - ◆ Single 32-bit AMBA-3 AHB-Lite system interface that provides simple integration to all system peripherals and memory.
 - ◆ Single 32-bit slave port that supports the DAP (Debug Access Port).

5.2 System Manager

5.2.1 Overview

System management includes these following sections:

- System Resets
- System Memory Map
- System management registers for Part Number ID, chip reset and on-chip controllers reset , multi-functional pin control
- System Timer (SysTick)
- Nested Vectored Interrupt Controller (NVIC)
- System Control registers

5.2.2 System Reset

The system reset can be issued by one of the below listed events. For these reset event flags can be read by RSTSRC register.

- The Power-On Reset
- The low level on the /RESET pin
- Watchdog Time Out Reset
- Low Voltage Reset
- Brown-Out Detector Reset
- CPU Reset
- System Reset

System Reset and Power-On Reset all reset the whole chip including all peripherals. The difference between System Reset and Power-On Reset is external crystal circuit and ISPCON.BS bit. System Reset doesn't reset external crystal circuit and ISPCON.BS bit, but Power-On Reset does.



5.2.4 System Memory Map

NuMicro™ NUC100 Series provides 4G-byte addressing space. The memory locations assigned to each on-chip controllers are shown in the following table. The detailed register definition, memory space, and programming detailed will be described in the following sections for each on-chip peripherals. NuMicro™ NUC100 Series only supports little-endian data format.

Address Space	Token	Controllers
Flash and SRAM Memory Space		
0x0000_0000 – 0x0001_FFFF	FLASH_BA	FLASH Memory Space (128KB)
0x2000_0000 – 0x2000_3FFF	SRAM_BA	SRAM Memory Space (16KB)
0x6000_0000 – 0x6001_FFFF	EXTMEM_BA	External Memory Space (128KB) (NuMicro™ NUC100/NUC120 Low Density 64-pin Only)
AHB Controllers Space (0x5000_0000 – 0x501F_FFFF)		
0x5000_0000 – 0x5000_01FF	GCR_BA	System Global Control Registers
0x5000_0200 – 0x5000_02FF	CLK_BA	Clock Control Registers
0x5000_0300 – 0x5000_03FF	INT_BA	Interrupt Multiplexer Control Registers
0x5000_4000 – 0x5000_7FFF	GPIO_BA	GPIO Control Registers
0x5000_8000 – 0x5000_BFFF	PDMA_BA	Peripheral DMA Control Registers
0x5000_C000 – 0x5000_FFFF	FMC_BA	Flash Memory Control Registers
0x5001_0000 – 0x5001_03FF	EBI_BA	External Bus Interface Control Registers (NuMicro™ NUC100/NUC120 Low Density 64-pin Only)
APB1 Controllers Space (0x4000_0000 ~ 0x400F_FFFF)		
0x4000_4000 – 0x4000_7FFF	WDT_BA	Watchdog Timer Control Registers
0x4000_8000 – 0x4000_BFFF	RTC_BA	Real Time Clock (RTC) Control Register
0x4001_0000 – 0x4001_3FFF	TMR01_BA	Timer0/Timer1 Control Registers
0x4002_0000 – 0x4002_3FFF	I2C0_BA	I ² C0 Interface Control Registers
0x4003_0000 – 0x4003_3FFF	SPI0_BA	SPI0 with master/slave function Control Registers
0x4003_4000 – 0x4003_7FFF	SPI1_BA	SPI1 with master/slave function Control Registers
0x4004_0000 – 0x4004_3FFF	PWMA_BA	PWM0/1/2/3 Control Registers
0x4005_0000 – 0x4005_3FFF	UART0_BA	UART0 Control Registers
0x4006_0000 – 0x4006_3FFF	USBD_BA	USB 2.0 FS device Controller Registers
0x400D_0000 – 0x400D_3FFF	ACMP_BA	Analog Comparator Control Registers

Address Space	Token	Controllers
0x400E_0000 – 0x400E_FFFF	ADC_BA	Analog-Digital-Converter (ADC) Control Registers
APB2 Controllers Space (0x4010_0000 ~ 0x401F_FFFF)		
0x4010_0000 – 0x4010_3FFF	PS2_BA	PS/2 Interface Control Registers
0x4011_0000 – 0x4011_3FFF	TMR23_BA	Timer2/Timer3 Control Registers
0x4012_0000 – 0x4012_3FFF	I2C1_BA	I ² C1 Interface Control Registers
0x4013_0000 – 0x4013_3FFF	SPI2_BA	SPI2 with master/slave function Control Registers (NuMicro™ NUC100/NUC120 Medium Density Only)
0x4013_4000 – 0x4013_7FFF	SPI3_BA	SPI3 with master/slave function Control Registers (NuMicro™ NUC100/NUC120 Medium Density Only)
0x4014_0000 – 0x4014_3FFF	PWMB_BA	PWM4/5/6/7 Control Registers (NuMicro™ NUC100/NUC120 Medium Density Only)
0x4015_0000 – 0x4015_3FFF	UART1_BA	UART1 Control Registers
0x4015_4000 – 0x4015_7FFF	UART2_BA	UART2 Control Registers (NuMicro™ NUC100/NUC120 Medium Density Only)
0x401A_0000 – 0x401A_3FFF	I2S_BA	I ² S Interface Control Registers
System Controllers Space (0xE000_E000 ~ 0xE000_EFFF)		
0xE000_E010 – 0xE000_E0FF	SCS_BA	System Timer Control Registers
0xE000_E100 – 0xE000_ECFF	SCS_BA	External Interrupt Controller Control Registers
0xE000_ED00 – 0xE000_ED8F	SCS_BA	System Control Registers

Table 5-1 Address Space Assignments for On-Chip Controllers

5.2.6.1 Exception Model and System Interrupt Map

Table 5-2 lists the exception model supported by NuMicro™ NUC100 Series. Software can set four levels of priority on some of these exceptions as well as on all interrupts. The highest user-configurable priority is denoted as “0” and the lowest priority is denoted as “3”. The default priority of all the user-configurable interrupts is “0”. Note that priority “0” is treated as the fourth priority on the system, after three system exceptions “Reset”, “NMI” and “Hard Fault”.

Exception Name	Vector Number	Priority
Reset	1	-3
NMI	2	-2
Hard Fault	3	-1
Reserved	4 ~ 10	Reserved
SVCall	11	Configurable
Reserved	12 ~ 13	Reserved
PendSV	14	Configurable
SysTick	15	Configurable
Interrupt (IRQ0 ~ IRQ31)	16 ~ 47	Configurable

Table 5-2 Exception Model

Vector Number	Interrupt Number (Bit in Interrupt Registers)	Interrupt Name	Source IP	Interrupt description
0 ~ 15	-	-	-	System exceptions
16	0	BOD_OUT	Brown-Out	Brown-Out low voltage detected interrupt
17	1	WDT_INT	WDT	Watchdog Timer interrupt
18	2	EINT0	GPIO	External signal interrupt from PB.14 pin
19	3	EINT1	GPIO	External signal interrupt from PB.15 pin
20	4	GPAB_INT	GPIO	External signal interrupt from PA[15:0]/PB[13:0]
21	5	GPCDE_INT	GPIO	External interrupt from PC[15:0]/PD[15:0]/PE[15:0]
22	6	PWMA_INT	PWM0~3	PWM0, PWM1, PWM2 and PWM3 interrupt
23	7	PWMB_INT	PWM4~7	PWM4, PWM5, PWM6 and PWM7 interrupt
24	8	TMR0_INT	TMR0	Timer 0 interrupt
25	9	TMR1_INT	TMR1	Timer 1 interrupt

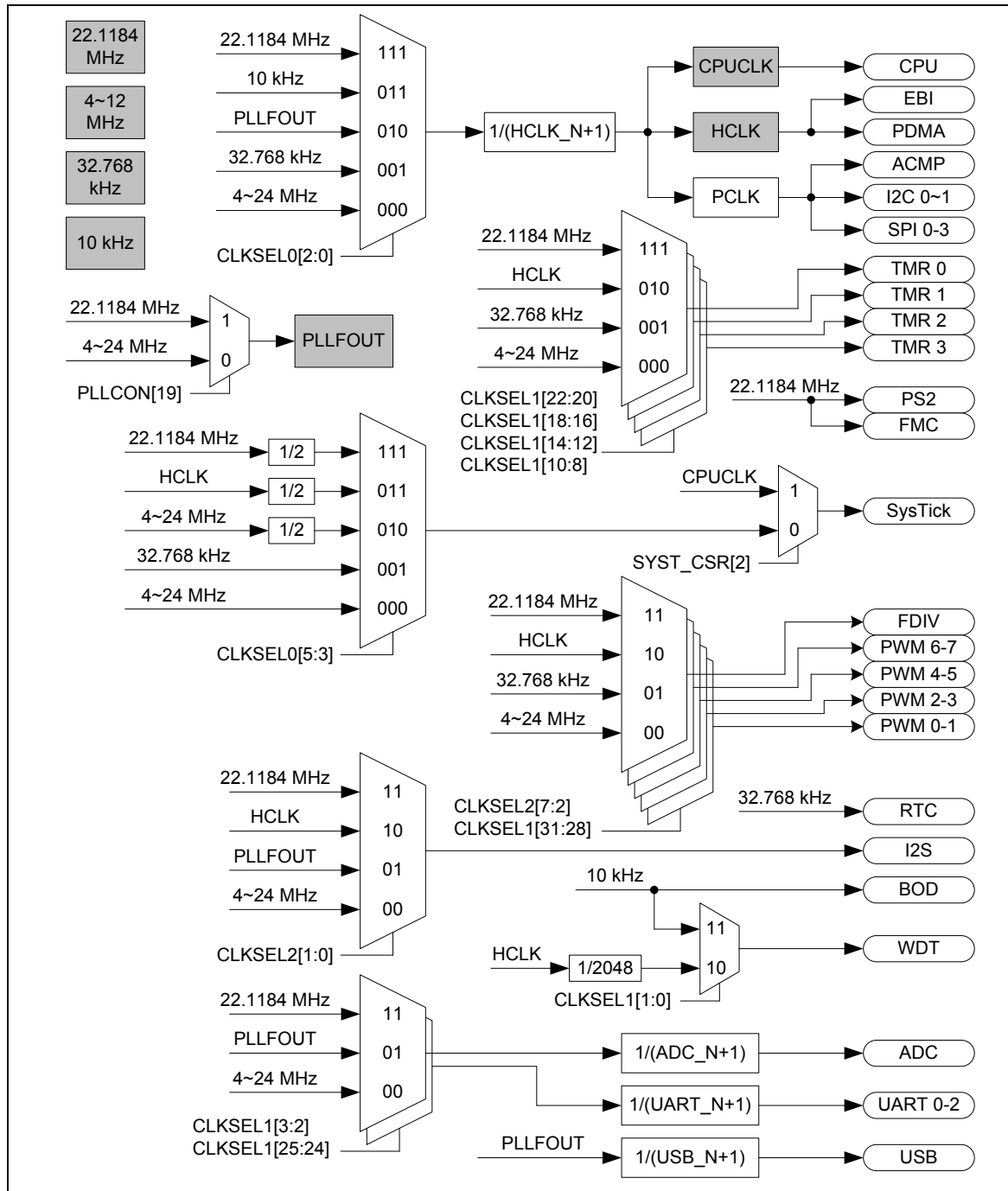


Figure 5-3 Clock generator global view diagram

5.6 I²C Serial Interface Controller (Master/Slave) (I²C)

5.6.1 Overview

I²C is a two-wire, bi-directional serial bus that provides a simple and efficient method of data exchange between devices. The I²C standard is a true multi-master bus including collision detection and arbitration that prevents data corruption if two or more masters attempt to control the bus simultaneously.

Data is transferred between a Master and a Slave synchronously to SCL on the SDA line on a byte-by-byte basis. Each data byte is 8-bit long. There is one SCL clock pulse for each data bit with the MSB being transmitted first. An acknowledge bit follows each transferred byte. Each bit is sampled during the high period of SCL; therefore, the SDA line may be changed only during the low period of SCL and must be held stable during the high period of SCL. A transition on the SDA line while SCL is high is interpreted as a command (START or STOP). Please refer to the Figure 5-9 for more detail I²C BUS Timing.

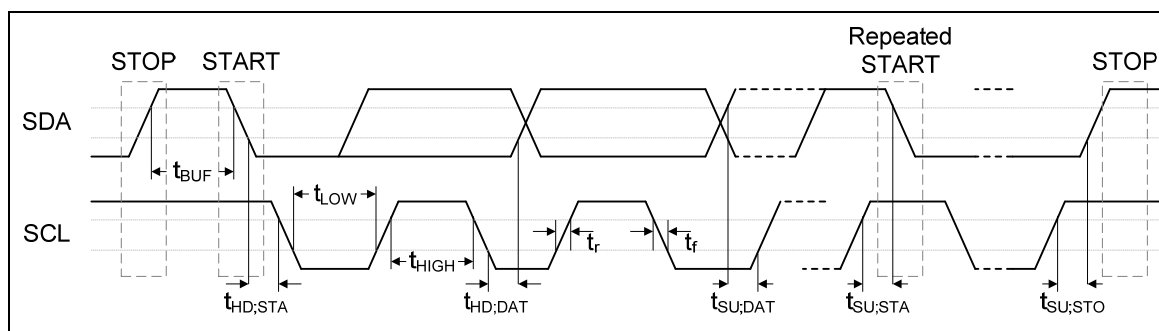


Figure 5-9 I²C Bus Timing

The device's on-chip I²C logic provides the serial interface that meets the I²C bus standard mode specification. The I²C port handles byte transfers autonomously. To enable this port, the bit ENS1 in I2CON should be set to '1'. The I²C H/W interfaces to the I²C bus via two pins: SDA and SCL. Pull up resistor is needed for I²C operation as these are open drain pins. When the I/O pins are used as I²C port, user must set the pins function to I²C in advance.

5.9 Serial Peripheral Interface (SPI)

5.9.1 Overview

The Serial Peripheral Interface (SPI) is a synchronous serial data communication protocol which operates in full duplex mode. Devices communicate in master/slave mode with 4-wire bi-direction interface. The NuMicro™ NUC100/NUC120 Medium Density contains up to four sets of SPI controller performing a serial-to-parallel conversion on data received from a peripheral device, and a parallel-to-serial conversion on data transmitted to a peripheral device. Each set of SPI controller can be set as a master that can drive up to 2 external peripheral slave devices; it also can be configured as a slave device controlled by an off-chip master device. NuMicro™ NUC100/NUC120 Low Density contains two sets of SPI controller only.

This controller supports a variable serial clock for special application and it also supports 2-bit transfer mode to connect 2 off-chip slave devices at the same time. The SPI controller also supports PDMA function to access the data buffer.

5.9.2 Features

- Up to four sets of SPI controller for NuMicro™ NUC100/NUC120 Medium Density
- Up to two sets of SPI controller for NuMicro™ NUC100/NUC120 Low Density
- Support master or slave mode operation
- Support 1-bit or 2-bit transfer mode
- Configurable bit length up to 32-bit of a transfer word and configurable word numbers up to 2 of a transaction, so the maximum bit length is 64-bit for each data transfer
- Provide burst mode operation, transmit/receive can be transferred up to two times word transaction in one transfer
- Support MSB or LSB first transfer
- 2 device/slave select lines in master mode, but 1 device/slave select line in slave mode
- Support byte reorder function
- Support byte or word suspend mode
- Variable output serial clock frequency in master mode
- Support two programmable serial clock frequencies in master mode
- Support two channel PDMA request, one for transmitter and another for receiver

5.12.2 Features

- Full duplex, asynchronous communications
- Separate receive / transmit 64/16/16 bytes (UART0/UART1/UART2) entry FIFO for data payloads
- Support hardware auto flow control/flow control function (CTS, RTS) and programmable RTS flow control trigger level (UART0 and UART1 support)
- Programmable receiver buffer trigger level
- Support programmable baud-rate generator for each channel individually
- Support CTS wake-up function (UART0 and UART1 support)
- Support 7-bit receiver buffer time out detection function
- UART0/UART1 can be served by the DMA controller
- Programmable transmitting data delay time between the last stop and the next start bit by setting UA_TOR [DLY] register
- Support break error, frame error, parity error and receive / transmit buffer overflow detect function
- Fully programmable serial-interface characteristics
 - Programmable number of data bit, 5-, 6-, 7-, 8-bit character
 - Programmable parity bit, even, odd, no parity or stick parity bit generation and detection
 - Programmable stop bit, 1, 1.5, or 2 stop bit generation
- Support IrDA SIR function mode
 - Support for 3-/16-bit duration for normal mode
- Support RS-485 function mode. (NuMicro™ NUC100/NUC120 Low Density only)
 - Support RS-485 9-bit mode
 - Support hardware or software direct enable control provided by RTS pin

7 ELECTRICAL CHARACTERISTICS

7.1 Absolute Maximum Ratings

SYMBOL	PARAMETER	MIN	MAX	UNIT
DC Power Supply	$V_{DD}-V_{SS}$	-0.3	+7.0	V
Input Voltage	V_{IN}	$V_{SS}-0.3$	$V_{DD}+0.3$	V
Oscillator Frequency	$1/t_{CLCL}$	4	24	MHz
Operating Temperature	TA	-40	+85	°C
Storage Temperature	TST	-55	+150	°C
Maximum Current into V_{DD}		-	120	mA
Maximum Current out of V_{SS}			120	mA
Maximum Current sunk by a I/O pin			35	mA
Maximum Current sourced by a I/O pin			35	mA
Maximum Current sunk by total I/O pins			100	mA
Maximum Current sourced by total I/O pins			100	mA

Note: Exposure to conditions beyond those listed under absolute maximum ratings may adversely affects the life and reliability of the device.

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
	I _{IDLE8}		4		mA	V _{DD} = 3 V@12 MHz, disable all IP and disable PLL, XTAL=12 MHz
Operating Current Idle Mode @ 4 MHz	I _{IDLE9}		8.5		mA	V _{DD} = 5 V@4 MHz, enable all IP and disable PLL, XTAL=4 MHz
	I _{IDLE10}		3.5		mA	V _{DD} = 5 V@4 MHz, disable all IP and disable PLL, XTAL=4 MHz
	I _{IDLE11}		7		mA	V _{DD} = 3 V@4 MHz, enable all IP and disable PLL, XTAL=4 MHz
	I _{IDLE12}		2.5		mA	V _{DD} = 3 V@4 MHz, disable all IP and disable PLL, XTAL=4 MHz
Standby Current Power down Mode	I _{PWD1}		23		μA	V _{DD} = 5.5 V, RTC OFF, No load @ Disable BOV function
	I _{PWD2}		18		μA	V _{DD} = 3.3 V, RTC OFF, No load @ Disable BOV function
	I _{PWD3}		28		μA	V _{DD} = 5.5 V, RTC run , No load @ Disable BOV function
	I _{PWD4}		22		μA	V _{DD} = 3.3 V, RTC run , No load @ Disable BOV function
Input Current PA, PB, PC, PD, PE (Quasi-bidirectional mode)	I _{IN1}		-50	-60	μA	V _{DD} = 5.5 V, V _{IN} = 0 V or V _{IN} =V _{DD}
Input Current at /RESET ^[1]	I _{IN2}	-55	-45	-30	μA	V _{DD} = 3.3 V, V _{IN} = 0.45 V
Input Leakage Current PA, PB, PC, PD, PE	I _{LK}	-2	-	+2	μA	V _{DD} = 5.5 V, 0<V _{IN} <V _{DD}
Logic 1 to 0 Transition Current PA~PE (Quasi-bidirectional mode)	I _{TL} ^[3]	-650	-	-200	μA	V _{DD} = 5.5 V, V _{IN} <2.0 V
Input Low Voltage PA, PB, PC, PD, PE (TTL input)	V _{IL1}	-0.3	-	0.8	V	V _{DD} = 4.5 V
		-0.3	-	0.6		V _{DD} = 2.5 V
Input High Voltage PA, PB, PC, PD, PE (TTL input)	V _{IH1}	2.0	-	V _{DD} +0.2	V	V _{DD} = 5.5 V
		1.5	-	V _{DD} +0.2		V _{DD} = 3.0 V
Input Low Voltage PA, PB, PC, PD, PE (Schmitt input)	V _{IL2}	-0.5	-	0.2 V _{DD}	V	

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Bandgap voltage	V _{BG}	1.20	1.26	1.32	V	V _{DD} = 2.5 V~5.5 V

Note:

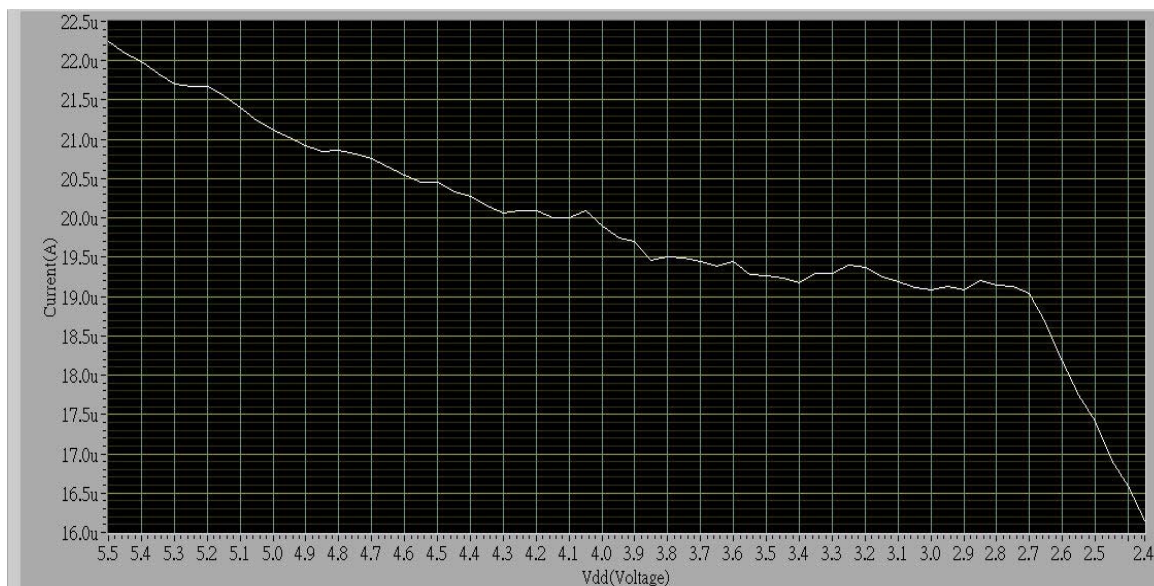
1. /RESET pin is a Schmitt trigger input.
2. Crystal Input is a CMOS input.
3. Pins of PA, PB, PC, PD and PE can source a transition current when they are being externally driven from 1 to 0. In the condition of V_{DD}=5.5 V, the transition current reaches its maximum value when V_{IN} approximates to 2 V.



7.2.5 Power Down Current Curve

XTAL clock = 12 MHz, PLL Disable

Unit: mA





7.4.8 Specification of USB PHY

7.4.8.1 USB DC Electrical Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V _{IH}	Input high (driven)		2.0			V
V _{IL}	Input low				0.8	V
V _{DI}	Differential input sensitivity	PADP-PADM	0.2			V
V _{CM}	Differential common-mode range	Includes V _{DI} range	0.8		2.5	V
V _{SE}	Single-ended receiver threshold		0.8		2.0	V
	Receiver hysteresis			200		mV
V _{OL}	Output low (driven)		0		0.3	V
V _{OH}	Output high (driven)		2.8		3.6	V
V _{CRS}	Output signal cross voltage		1.3		2.0	V
R _{PU}	Pull-up resistor		1.425		1.575	kΩ
V _{TRM}	Termination Voltage for upstream port pull up (RPU)		3.0		3.6	V
Z _{DRV}	Driver output resistance	Steady state drive*		10		Ω
C _{IN}	Transceiver capacitance	Pin to GND			20	pF

*Driver output resistance doesn't include series resistor resistance.

7.4.8.2 USB Full-Speed Driver Electrical Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
T _{FR}	Rise Time	C _L =50p	4		20	ns
T _{FF}	Fall Time	C _L =50p	4		20	ns
T _{FRFF}	Rise and fall time matching	T _{FRFF} =T _{FR} /T _{FF}	90		111.11	%

7.4.8.3 USB Power Dissipation

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I _{VDDREG} (Full Speed)	V _{DDD} and V _{DDREG} Supply Current (Steady State)	Standby		50		uA
		Input mode				uA
		Output mode				uA

7.5 Flash DC Electrical Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
N _{endu}	Endurance		10000			cycles ^[1]
T _{ret}	Retention time	Temp=25 °C	100			year
T _{erase}	Page erase time		20		40	ms
T _{mass}	Mass erase time		40	50	60	ms
T _{prog}	Program time		35	40	55	us
V _{dd}	Supply voltage		2.25	2.5	2.75	V ^[2]
I _{dd1}	Read current				14	mA
I _{dd2}	Program/Erase current				7	mA
I _{pd}	Power down current				10	uA

1. Number of program/erase cycles.
2. V_{dd} is source from chip LDO output voltage.
3. This table is guaranteed by design, not test in production.

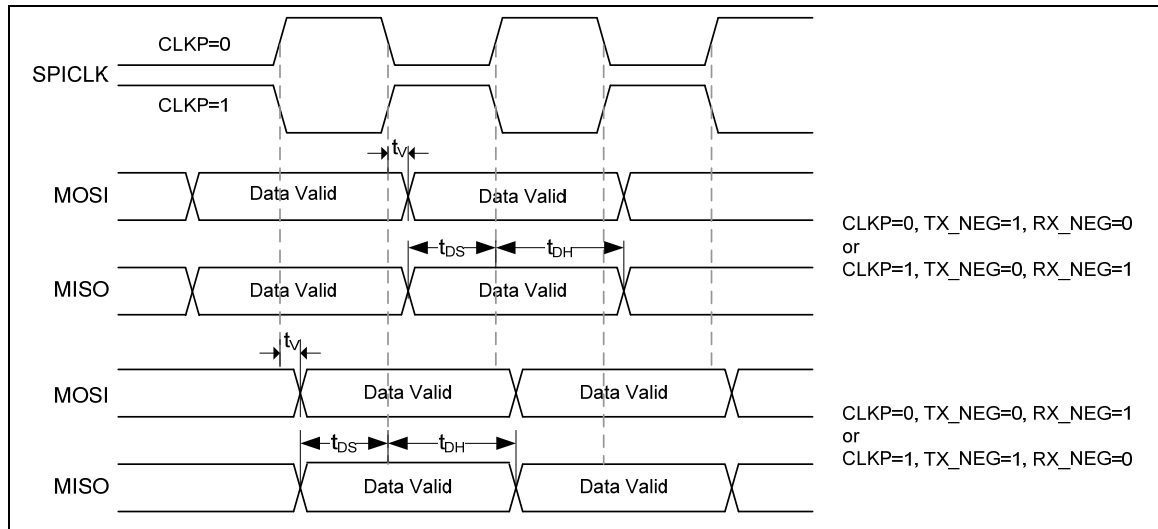


Figure 7-2 SPI Master dynamic characteristics timing

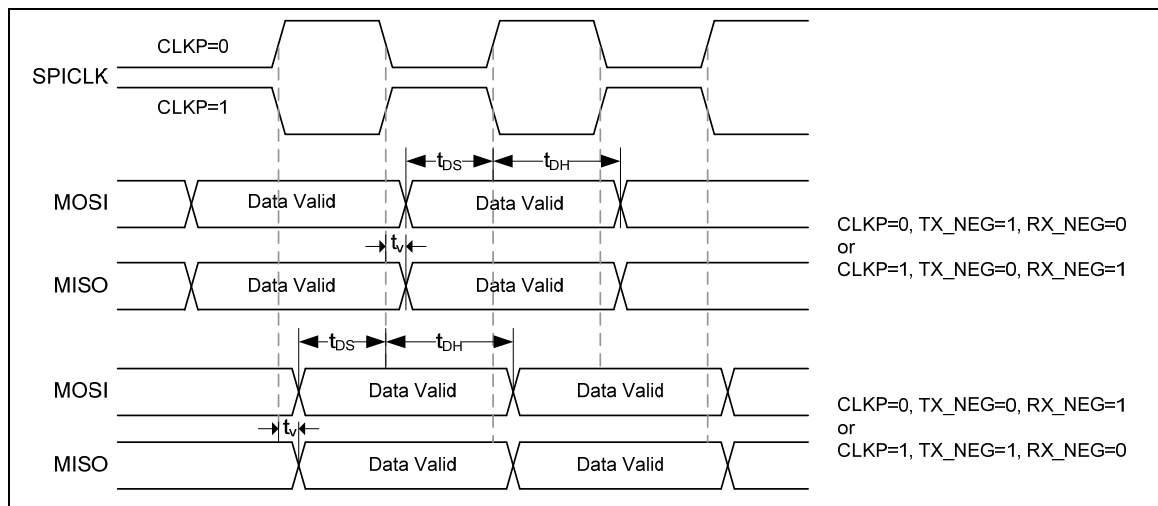


Figure 7-3 SPI Slave dynamic characteristics timing



Important Notice

Nuvoton Products are neither intended nor warranted for usage in systems or equipment, any malfunction or failure of which may cause loss of human life, bodily injury or severe property damage. Such applications are deemed, "Insecure Usage".

Insecure usage includes, but is not limited to: equipment for surgical implementation, atomic energy control instruments, airplane or spaceship instruments, the control or operation of dynamic, brake or safety systems designed for vehicular use, traffic signal instruments, all types of safety devices, and other applications intended to support or sustain life.

All Insecure Usage shall be made at customer's risk, and in the event that third parties lay claims to Nuvoton as a result of customer's Insecure Usage, customer shall indemnify the damages and liabilities thus incurred by Nuvoton.

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