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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | R8C |
| Core Size | 16-Bit |
| Speed | 20MHz |
| Connectivity | I²C, LINbus, SIO, SSU, UART/USART |
| Peripherals | POR, PWM, Voltage Detect, WDT |
| Number of I/O | 75 |
| Program Memory Size | 48KB (48K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | 4K x 8 |
| RAM Size | 4K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.8V ~ 5.5V |
| Data Converters | A/D 20x10b; D/A 2x8b |
| Oscillator Type | Internal |
| Operating Temperature | -20°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 80-LQFP |
| Supplier Device Package | 80-LQFP (12x12) |
| Purchase URL | https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f21387cnfp-30 |

### 1.1.2 Specifications

Tables 1.1 and 1.2 outline the Specifications for R8C/38C Group.

**Table 1.1 Specifications for R8C/38C Group (1)**

| Item | Function | Specification |
|---|---|---|
| CPU | Central processing unit | R8C CPU core<br>• Number of fundamental instructions: 89<br>• Minimum instruction execution time:<br>50 ns (f(XIN) = 20 MHz, VCC = 2.7 to 5.5 V)<br>200 ns (f(XIN) = 5 MHz, VCC = 1.8 to 5.5 V)<br>• Multiplier: 16 bits × 16 bits → 32 bits<br>• Multiply-accumulate instruction: 16 bits × 16 bits + 32 bits → 32 bits<br>• Operation mode: Single-chip mode (address space: 1 Mbyte) |
| Memory | ROM, RAM, Data flash | Refer to **Table 1.3 Product List for R8C/38C Group** |
| Power Supply Voltage Detection | Voltage detection circuit | • Power-on reset<br>• Voltage detection 3 (detection level of voltage detection 0 and voltage detection 1 selectable) |
| I/O Ports | Programmable I/O ports | • Input-only: 1 pin<br>• CMOS I/O ports: 75, selectable pull-up resistor<br>• High current drive ports: 75 |
| Clock | Clock generation circuits | • 4 circuits: XIN clock oscillation circuit,<br>XCIN clock oscillation circuit (32 kHz),<br>High-speed on-chip oscillator (with frequency adjustment function),<br>Low-speed on-chip oscillator<br>• Oscillation stop detection: XIN clock oscillation stop detection function<br>• Frequency divider circuit: Dividing selectable 1, 2, 4, 8, and 16<br>• Low power consumption modes:<br>Standard operating mode (high-speed clock, low-speed clock, high-speed on-chip oscillator, low-speed on-chip oscillator), wait mode, stop mode |
| | | Real-time clock (timer RE) |
| Interrupts | | • Interrupt Vectors: 69<br>• External: 9 sources ($\overline{\text{INT}}$ × 5, key input × 4)<br>• Priority levels: 7 levels |
| Watchdog Timer | | • 14 bits × 1 (with prescaler)<br>• Reset start selectable<br>• Low-speed on-chip oscillator for watchdog timer selectable |
| DTC (Data Transfer Controller) | | • 1 channel<br>• Activation sources: 39<br>• Transfer modes: 2 (normal mode, repeat mode) |
| Timer | Timer RA | 8 bits × 1 (with 8-bit prescaler)<br>Timer mode (period timer), pulse output mode (output level inverted every period), event counter mode, pulse width measurement mode, pulse period measurement mode |
| | Timer RB | 8 bits × 1 (with 8-bit prescaler)<br>Timer mode (period timer), programmable waveform generation mode (PWM output), programmable one-shot generation mode, programmable wait one-shot generation mode |
| | Timer RC | 16 bits × 1 (with 4 capture/compare registers)<br>Timer mode (input capture function, output compare function), PWM mode (output 3 pins), PWM2 mode (PWM output pin) |
| | Timer RD | 16 bits × 2 (with 4 capture/compare registers)<br>Timer mode (input capture function, output compare function), PWM mode (output 6 pins), reset synchronous PWM mode (output three-phase waveforms (6 pins), sawtooth wave modulation), complementary PWM mode (output three-phase waveforms (6 pins), triangular wave modulation), PWM3 mode (PWM output 2 pins with fixed period) |

## 1.2 Product List

Table 1.3 lists Product List for R8C/38C Group. Figure 1.1 shows a Part Number, Memory Size, and Package of R8C/38C Group.

**Table 1.3 Product List for R8C/38C Group** **Current of Nov 2010**

| Part No. | ROM Capacity | | RAM Capacity | Package Type | Remarks | |
|---|---|---|---|---|---|---|
| | Program ROM | Data flash | | | | |
| R5F21386CNFP | 32 Kbytes | 1 Kbyte × 4 | 2.5 Kbytes | PLQP0080KB-A | N version | |
| R5F21387CNFP | 48 Kbytes | 1 Kbyte × 4 | 4 Kbytes | PLQP0080KB-A | | |
| R5F21388CNFP | 64 Kbytes | 1 Kbyte × 4 | 6 Kbytes | PLQP0080KB-A | | |
| R5F2138ACNFP | 96 Kbytes | 1 Kbyte × 4 | 8 Kbytes | PLQP0080KB-A | | |
| R5F2138CCNFP | 128 Kbytes | 1 Kbyte × 4 | 10 Kbytes | PLQP0080KB-A | | |
| R5F21386CNXXXFP | 32 Kbytes | 1 Kbyte × 4 | 2.5 Kbytes | PLQP0080KB-A | N version | Factory programming product (1) |
| R5F21387CNXXXFP | 48 Kbytes | 1 Kbyte × 4 | 4 Kbytes | PLQP0080KB-A | | |
| R5F21388CNXXXFP | 64 Kbytes | 1 Kbyte × 4 | 6 Kbytes | PLQP0080KB-A | | |
| R5F2138ACNXXXFP | 96 Kbytes | 1 Kbyte × 4 | 8 Kbytes | PLQP0080KB-A | | |
| R5F2138CCNXXXFP | 128 Kbytes | 1 Kbyte × 4 | 10 Kbytes | PLQP0080KB-A | | |
| R5F21386CDFP | 32 Kbytes | 1 Kbyte × 4 | 2.5 Kbytes | PLQP0080KB-A | D version | |
| R5F21387CDFP | 48 Kbytes | 1 Kbyte × 4 | 4 Kbytes | PLQP0080KB-A | | |
| R5F21388CDFP | 64 Kbytes | 1 Kbyte × 4 | 6 Kbytes | PLQP0080KB-A | | |
| R5F2138ACDFP | 96 Kbytes | 1 Kbyte × 4 | 8 Kbytes | PLQP0080KB-A | | |
| R5F2138CCDFP | 128 Kbytes | 1 Kbyte × 4 | 10 Kbytes | PLQP0080KB-A | | |
| R5F21386CDXXXFP | 32 Kbytes | 1 Kbyte × 4 | 2.5 Kbytes | PLQP0080KB-A | D version | Factory programming product (1) |
| R5F21387CDXXXFP | 48 Kbytes | 1 Kbyte × 4 | 4 Kbytes | PLQP0080KB-A | | |
| R5F21388CDXXXFP | 64 Kbytes | 1 Kbyte × 4 | 6 Kbytes | PLQP0080KB-A | | |
| R5F2138ACDXXXFP | 96 Kbytes | 1 Kbyte × 4 | 8 Kbytes | PLQP0080KB-A | | |
| R5F2138CCDXXXFP | 128 Kbytes | 1 Kbyte × 4 | 10 Kbytes | PLQP0080KB-A | | |

Note:
1. The user ROM is programmed before shipment.

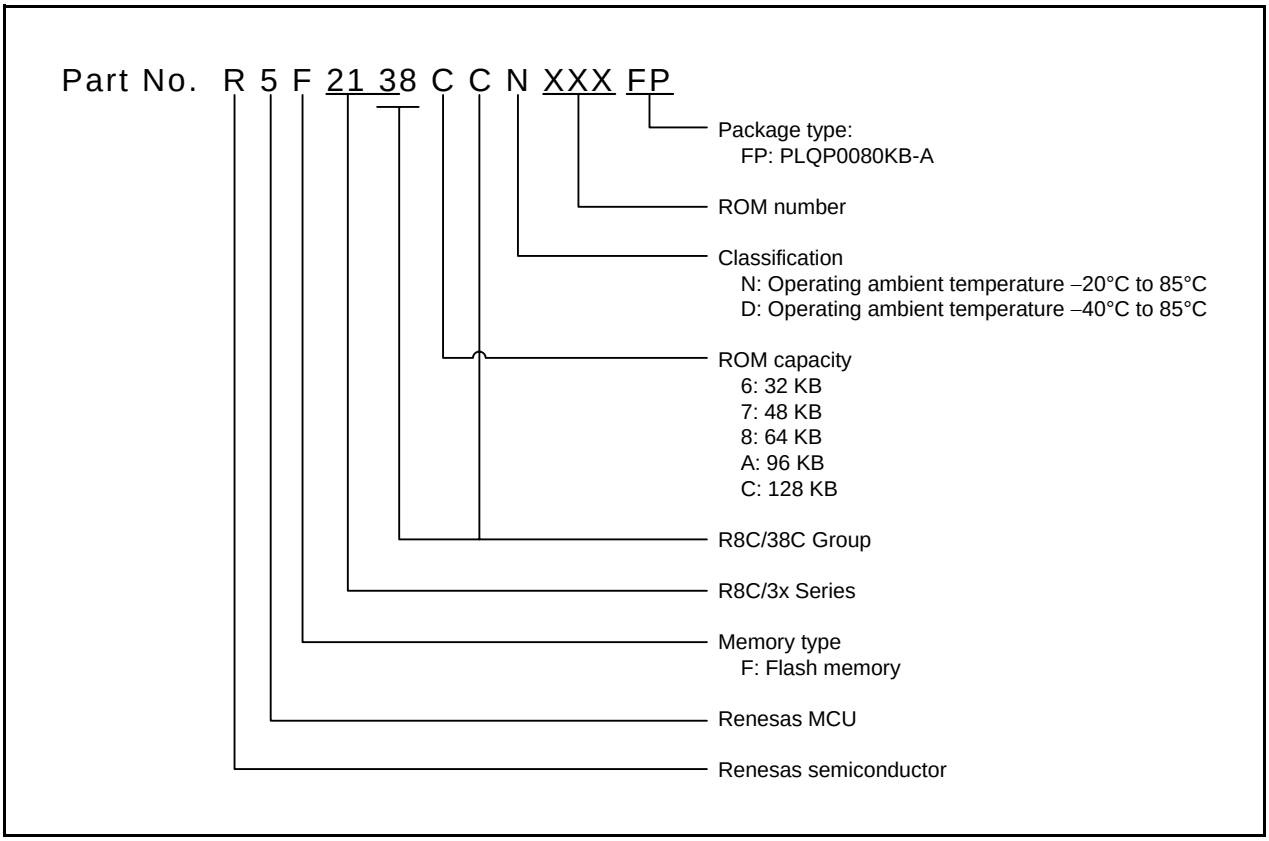



**Figure 1.1 Part Number, Memory Size, and Package of R8C/38C Group**

## 1.3 Block Diagram

Figure 1.2 shows a Block Diagram.

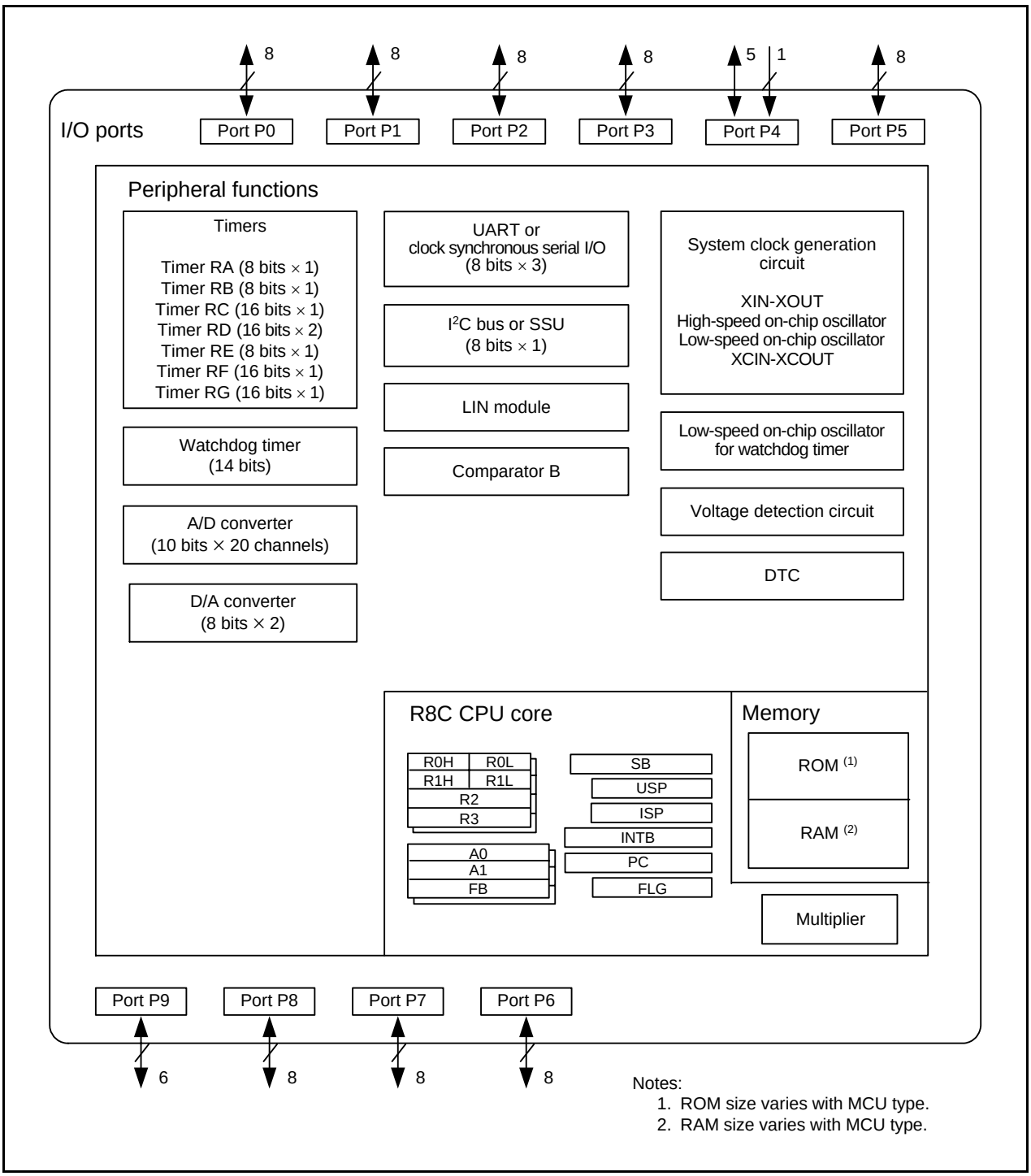



**Figure 1.2 Block Diagram**

## 1.5 Pin Functions

Tables 1.6 and 1.7 list Pin Functions.

**Table 1.6 Pin Functions (1)**

| Item | Pin Name | I/O Type | Description |
|---|---|---|---|
| Power supply input | VCC, VSS | — | Apply 1.8 to 5.5 V to the VCC pin.<br>Apply 0 V to the VSS pin. |
| Analog power supply input | AVCC, AVSS | — | Power supply for the A/D converter.<br>Connect a capacitor between AVCC and AVSS. |
| Reset input | $\overline{\text{RESET}}$ | I | Input “L” on this pin resets the MCU. |
| MODE | MODE | I | Connect this pin to VCC via a resistor. |
| XIN clock input | XIN | I | These pins are provided for XIN clock generation circuit I/O.<br>Connect a ceramic resonator or a crystal oscillator between the XIN and XOUT pins. (1)<br>To use an external clock, input it to the XOUT pin and leave the XIN pin open. |
| XIN clock output | XOUT | I/O | |
| XCIN clock input | XCIN | I | These pins are provided for XCIN clock generation circuit I/O.<br>Connect a crystal oscillator between the XCIN and XCOUT pins. (1)<br>To use an external clock, input it to the XCIN pin and leave the XCOUT pin open. |
| XCIN clock output | XCOUT | O | |
| $\overline{\text{INT}}$ interrupt input | $\overline{\text{INT0}}$ to $\overline{\text{INT4}}$ | I | $\overline{\text{INT}}$ interrupt input pins. |
| Key input interrupt | $\overline{\text{KI0}}$ to $\overline{\text{KI3}}$ | I | Key input interrupt input pins. |
| Timer RA | TRAIO | I/O | Timer RA I/O pin. |
| | TRAO | O | Timer RA output pin. |
| Timer RB | TRBO | O | Timer RB output pin. |
| Timer RC | TRCCLK | I | External clock input pin. |
| | TRCTRG | I | External trigger input pin. |
| | TRCIOA, TRCIOB, TRCIOC, TRCIOD | I/O | Timer RC I/O pins. |
| Timer RD | TRDIOA0, TRDIOA1, TRDIOB0, TRDIOB1, TRDIOC0, TRDIOC1, TRDIOD0, TRDIOD1 | I/O | Timer RD I/O pins. |
| | TRDCLK | I | External clock input pin. |
| Timer RE | TREO | O | Divided clock output pin. |
| Timer RF | TRFO00, TRFO10, TRFO01,TRFO11, TRFO02,TRFO12 | O | Timer RF output pins. |
| | TRFI | I | Timer RF input pin. |
| Timer RG | TRGIOA, TRGIOB | I/O | Timer RG I/O ports. |
| | TRGCLKA, TRGCLKB | I | External clock input pins. |
| Serial interface | CLK0, CLK1, CLK2 | I/O | Transfer clock I/O pins. |
| | RXD0, RXD1, RXD2 | I | Serial data input pins. |
| | TXD0, TXD1, TXD2 | O | Serial data output pins. |
| | $\overline{\text{CTS2}}$ | I | Transmission control input pin. |
| | $\overline{\text{RTS2}}$ | O | Reception control output pin. |
| | SCL2 | I/O | $I^2C$ mode clock I/O pin. |
| | SDA2 | I/O | $I^2C$ mode data I/O pin. |

I: Input O: Output I/O: Input and output

Note:

1. Refer to the oscillator manufacturer for oscillation characteristics.

**Table 4.4 SFR Information (4) (1)**

| Address | Register | Symbol | After Reset |
|---|---|---|---|
| 00C0h | A/D Register 0 | AD0 | XXh |
| 00C1h | | | 000000XXb |
| 00C2h | A/D Register 1 | AD1 | XXh |
| 00C3h | | | 000000XXb |
| 00C4h | A/D Register 2 | AD2 | XXh |
| 00C5h | | | 000000XXb |
| 00C6h | A/D Register 3 | AD3 | XXh |
| 00C7h | | | 000000XXb |
| 00C8h | A/D Register 4 | AD4 | XXh |
| 00C9h | | | 000000XXb |
| 00CAh | A/D Register 5 | AD5 | XXh |
| 00CBh | | | 000000XXb |
| 00CCh | A/D Register 6 | AD6 | XXh |
| 00CDh | | | 000000XXb |
| 00CEh | A/D Register 7 | AD7 | XXh |
| 00CFh | | | 000000XXb |
| 00D0h | | | |
| 00D1h | | | |
| 00D2h | | | |
| 00D3h | | | |
| 00D4h | A/D Mode Register | ADMOD | 00h |
| 00D5h | A/D Input Select Register | ADINSEL | 11000000b |
| 00D6h | A/D Control Register 0 | ADCON0 | 00h |
| 00D7h | A/D Control Register 1 | ADCON1 | 00h |
| 00D8h | D/A0 Register | DA0 | 00h |
| 00D9h | D/A1 Register | DA1 | 00h |
| 00DAh | | | |
| 00DBh | | | |
| 00DCh | D/A Control Register | DACON | 00h |
| 00DDh | | | |
| 00DEh | | | |
| 00DFh | | | |
| 00E0h | Port P0 Register | P0 | XXh |
| 00E1h | Port P1 Register | P1 | XXh |
| 00E2h | Port P0 Direction Register | PD0 | 00h |
| 00E3h | Port P1 Direction Register | PD1 | 00h |
| 00E4h | Port P2 Register | P2 | XXh |
| 00E5h | Port P3 Register | P3 | XXh |
| 00E6h | Port P2 Direction Register | PD2 | 00h |
| 00E7h | Port P3 Direction Register | PD3 | 00h |
| 00E8h | Port P4 Register | P4 | XXh |
| 00E9h | Port P5 Register | P5 | XXh |
| 00EAh | Port P4 Direction Register | PD4 | 00h |
| 00EBh | Port P5 Direction Register | PD5 | 00h |
| 00ECh | Port P6 Register | P6 | XXh |
| 00EDh | Port P7 Register | P7 | XXh |
| 00EEh | Port P6 Direction Register | PD6 | 00h |
| 00EFh | Port P7 Direction Register | PD7 | 00h |
| 00F0h | Port P8 Register | P8 | XXh |
| 00F1h | Port P9 Register | P9 | XXh |
| 00F2h | Port P8 Direction Register | PD8 | 00h |
| 00F3h | Port P9 Direction Register | PD9 | 00h |
| 00F4h | | | |
| 00F5h | | | |
| 00F6h | | | |
| 00F7h | | | |
| 00F8h | | | |
| 00F9h | | | |
| 00FAh | | | |
| 00FBh | | | |
| 00FCh | | | |
| 00FDh | | | |
| 00FEh | | | |
| 00FFh | | | |

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

**Table 4.5 SFR Information (5) (1)**

| Address | Register | Symbol | After Reset |
|---|---|---|---|
| 0100h | Timer RA Control Register | TRACR | 00h |
| 0101h | Timer RA I/O Control Register | TRAIOC | 00h |
| 0102h | Timer RA Mode Register | TRAMR | 00h |
| 0103h | Timer RA Prescaler Register | TRAPRE | FFh |
| 0104h | Timer RA Register | TRA | FFh |
| 0105h | LIN Control Register 2 | LINCR2 | 00h |
| 0106h | LIN Control Register | LINCR | 00h |
| 0107h | LIN Status Register | LINST | 00h |
| 0108h | Timer RB Control Register | TRBCR | 00h |
| 0109h | Timer RB One-Shot Control Register | TRBOCR | 00h |
| 010Ah | Timer RB I/O Control Register | TRBIOC | 00h |
| 010Bh | Timer RB Mode Register | TRBMR | 00h |
| 010Ch | Timer RB Prescaler Register | TRBPRE | FFh |
| 010Dh | Timer RB Secondary Register | TRBSC | FFh |
| 010Eh | Timer RB Primary Register | TRBPR | FFh |
| 010Fh | | | |
| 0110h | | | |
| 0111h | | | |
| 0112h | | | |
| 0113h | | | |
| 0114h | | | |
| 0115h | | | |
| 0116h | | | |
| 0117h | | | |
| 0118h | Timer RE Second Data Register / Counter Data Register | TRESEC | 00h |
| 0119h | Timer RE Minute Data Register / Compare Data Register | TREMIN | 00h |
| 011Ah | Timer RE Hour Data Register | TREHR | 00h |
| 011Bh | Timer RE Day of Week Data Register | TREWK | 00h |
| 011Ch | Timer RE Control Register 1 | TRECR1 | 00h |
| 011Dh | Timer RE Control Register 2 | TRECR2 | 00h |
| 011Eh | Timer RE Count Source Select Register | TRECSR | 00001000b |
| 011Fh | | | |
| 0120h | Timer RC Mode Register | TRCMR | 01001000b |
| 0121h | Timer RC Control Register 1 | TRCCR1 | 00h |
| 0122h | Timer RC Interrupt Enable Register | TRCIER | 01110000b |
| 0123h | Timer RC Status Register | TRCSR | 01110000b |
| 0124h | Timer RC I/O Control Register 0 | TRCIOR0 | 10001000b |
| 0125h | Timer RC I/O Control Register 1 | TRCIOR1 | 10001000b |
| 0126h | Timer RC Counter | TRC | 00h |
| 0127h | | | 00h |
| 0128h | Timer RC General Register A | TRCGRA | FFh |
| 0129h | | | FFh |
| 012Ah | Timer RC General Register B | TRCGRB | FFh |
| 012Bh | | | FFh |
| 012Ch | Timer RC General Register C | TRCGRC | FFh |
| 012Dh | | | FFh |
| 012Eh | Timer RC General Register D | TRCGRD | FFh |
| 012Fh | | | FFh |
| 0130h | Timer RC Control Register 2 | TRCCR2 | 00011000b |
| 0131h | Timer RC Digital Filter Function Select Register | TRCDF | 00h |
| 0132h | Timer RC Output Master Enable Register | TRCOER | 01111111b |
| 0133h | Timer RC Trigger Control Register | TRCADCR | 00h |
| 0134h | | | |
| 0135h | Timer RD Control Expansion Register | TRDECR | 00h |
| 0136h | Timer RD Trigger Control Register | TRDADCR | 00h |
| 0137h | Timer RD Start Register | TRDSTR | 11111100b |
| 0138h | Timer RD Mode Register | TRDMR | 00001110b |
| 0139h | Timer RD PWM Mode Register | TRDPMR | 10001000b |
| 013Ah | Timer RD Function Control Register | TRDFCR | 10000000b |
| 013Bh | Timer RD Output Master Enable Register 1 | TRDOER1 | FFh |
| 013Ch | Timer RD Output Master Enable Register 2 | TRDOER2 | 01111111b |
| 013Dh | Timer RD Output Control Register | TRDOCR | 00h |
| 013Eh | Timer RD Digital Filter Function Select Register 0 | TRDDF0 | 00h |
| 013Fh | Timer RD Digital Filter Function Select Register 1 | TRDDF1 | 00h |

Note:
1. The blank areas are reserved and cannot be accessed by users.

**Table 4.6 SFR Information (6) (1)**

| Address | Register | Symbol | After Reset |
|---|---|---|---|
| 0140h | Timer RD Control Register 0 | TRDCR0 | 00h |
| 0141h | Timer RD I/O Control Register A0 | TRDIORA0 | 10001000b |
| 0142h | Timer RD I/O Control Register C0 | TRDIORC0 | 10001000b |
| 0143h | Timer RD Status Register 0 | TRDSR0 | 11100000b |
| 0144h | Timer RD Interrupt Enable Register 0 | TRDIER0 | 11100000b |
| 0145h | Timer RD PWM Mode Output Level Control Register 0 | TRDPOCR0 | 11111000b |
| 0146h | Timer RD Counter 0 | TRD0 | 00h |
| 0147h | | | 00h |
| 0148h | Timer RD General Register A0 | TRDGRA0 | FFh |
| 0149h | | | FFh |
| 014Ah | Timer RD General Register B0 | TRDGRB0 | FFh |
| 014Bh | | | FFh |
| 014Ch | Timer RD General Register C0 | TRDGRC0 | FFh |
| 014Dh | | | FFh |
| 014Eh | Timer RD General Register D0 | TRDGRD0 | FFh |
| 014Fh | | | FFh |
| 0150h | Timer RD Control Register 1 | TRDCR1 | 00h |
| 0151h | Timer RD I/O Control Register A1 | TRDIORA1 | 10001000b |
| 0152h | Timer RD I/O Control Register C1 | TRDIORC1 | 10001000b |
| 0153h | Timer RD Status Register 1 | TRDSR1 | 11000000b |
| 0154h | Timer RD Interrupt Enable Register 1 | TRDIER1 | 11100000b |
| 0155h | Timer RD PWM Mode Output Level Control Register 1 | TRDPOCR1 | 11111000b |
| 0156h | Timer RD Counter 1 | TRD1 | 00h |
| 0157h | | | 00h |
| 0158h | Timer RD General Register A1 | TRDGRA1 | FFh |
| 0159h | | | FFh |
| 015Ah | Timer RD General Register B1 | TRDGRB1 | FFh |
| 015Bh | | | FFh |
| 015Ch | Timer RD General Register C1 | TRDGRC1 | FFh |
| 015Dh | | | FFh |
| 015Eh | Timer RD General Register D1 | TRDGRD1 | FFh |
| 015Fh | | | FFh |
| 0160h | UART1 Transmit/Receive Mode Register | U1MR | 00h |
| 0161h | UART1 Bit Rate Register | U1BRG | XXh |
| 0162h | UART1 Transmit Buffer Register | U1TB | XXh |
| 0163h | | | XXh |
| 0164h | UART1 Transmit/Receive Control Register 0 | U1C0 | 00001000b |
| 0165h | UART1 Transmit/Receive Control Register 1 | U1C1 | 00000010b |
| 0166h | UART1 Receive Buffer Register | U1RB | XXh |
| 0167h | | | XXh |
| 0168h | | | |
| 0169h | | | |
| 016Ah | | | |
| 016Bh | | | |
| 016Ch | | | |
| 016Dh | | | |
| 016Eh | | | |
| 016Fh | | | |
| 0170h | Timer RG Mode Register | TRGMR | 01000000b |
| 0171h | Timer RG Count Control Register | TRGCNTC | 00h |
| 0172h | Timer RG Control Register | TRGCR | 10000000b |
| 0173h | Timer RG Interrupt Enable Register | TRGIER | 11110000b |
| 0174h | Timer RG Status Register | TRGSR | 11100000b |
| 0175h | Timer RG I/O Control Register | TRGIOR | 00h |
| 0176h | Timer RG Counter | TRG | 00h |
| 0177h | | | 00h |
| 0178h | Timer RG General Register A | TRGGRA | FFh |
| 0179h | | | FFh |
| 017Ah | Timer RG General Register B | TRGGRB | FFh |
| 017Bh | | | FFh |
| 017Ch | Timer RG General Register C | TRGGRC | FFh |
| 017Dh | | | FFh |
| 017Eh | Timer RG General Register D | TRGGRD | FFh |
| 017Fh | | | FFh |

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

**Table 4.10 SFR Information (10) (1)**

| Address | Register | Symbol | After Reset |
|---|---|---|---|
| 2C70h | DTC Control Data 6 | DTCD6 | XXh |
| 2C71h | | | XXh |
| 2C72h | | | XXh |
| 2C73h | | | XXh |
| 2C74h | | | XXh |
| 2C75h | | | XXh |
| 2C76h | | | XXh |
| 2C77h | | | XXh |
| 2C78h | DTC Control Data 7 | DTCD7 | XXh |
| 2C79h | | | XXh |
| 2C7Ah | | | XXh |
| 2C7Bh | | | XXh |
| 2C7Ch | | | XXh |
| 2C7Dh | | | XXh |
| 2C7Eh | | | XXh |
| 2C7Fh | | | XXh |
| 2C80h | DTC Control Data 8 | DTCD8 | XXh |
| 2C81h | | | XXh |
| 2C82h | | | XXh |
| 2C83h | | | XXh |
| 2C84h | | | XXh |
| 2C85h | | | XXh |
| 2C86h | | | XXh |
| 2C87h | | | XXh |
| 2C88h | DTC Control Data 9 | DTCD9 | XXh |
| 2C89h | | | XXh |
| 2C8Ah | | | XXh |
| 2C8Bh | | | XXh |
| 2C8Ch | | | XXh |
| 2C8Dh | | | XXh |
| 2C8Eh | | | XXh |
| 2C8Fh | | | XXh |
| 2C90h | DTC Control Data 10 | DTCD10 | XXh |
| 2C91h | | | XXh |
| 2C92h | | | XXh |
| 2C93h | | | XXh |
| 2C94h | | | XXh |
| 2C95h | | | XXh |
| 2C96h | | | XXh |
| 2C97h | | | XXh |
| 2C98h | DTC Control Data 11 | DTCD11 | XXh |
| 2C99h | | | XXh |
| 2C9Ah | | | XXh |
| 2C9Bh | | | XXh |
| 2C9Ch | | | XXh |
| 2C9Dh | | | XXh |
| 2C9Eh | | | XXh |
| 2C9Fh | | | XXh |
| 2CA0h | DTC Control Data 12 | DTCD12 | XXh |
| 2CA1h | | | XXh |
| 2CA2h | | | XXh |
| 2CA3h | | | XXh |
| 2CA4h | | | XXh |
| 2CA5h | | | XXh |
| 2CA6h | | | XXh |
| 2CA7h | | | XXh |
| 2CA8h | DTC Control Data 13 | DTCD13 | XXh |
| 2CA9h | | | XXh |
| 2CAAh | | | XXh |
| 2CABh | | | XXh |
| 2CACh | | | XXh |
| 2CADh | | | XXh |
| 2CAEh | | | XXh |
| 2CAFh | | | XXh |

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

### Table 4.12 SFR Information (12) (1)

| Address | Register | Symbol | After Reset |
|---|---|---|---|
| 2CF0h | DTC Control Data 22 | DTCD22 | XXh |
| 2CF1h | | | XXh |
| 2CF2h | | | XXh |
| 2CF3h | | | XXh |
| 2CF4h | | | XXh |
| 2CF5h | | | XXh |
| 2CF6h | | | XXh |
| 2CF7h | | | XXh |
| 2CF8h | DTC Control Data 23 | DTCD23 | XXh |
| 2CF9h | | | XXh |
| 2CFAh | | | XXh |
| 2CFBh | | | XXh |
| 2CFCh | | | XXh |
| 2CFDh | | | XXh |
| 2CFEh | | | XXh |
| 2CFFh | | | XXh |
| 2D00h | | | |
| : | | | |
| 2FFFh | | | |

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

### Table 4.13 ID Code Areas and Option Function Select Area

| Address | Area Name | Symbol | After Reset |
|---|---|---|---|
| : | | | |
| FFDBh | Option Function Select Register 2 | OFS2 | (Note 1) |
| : | | | |
| FFDFh | ID1 | | (Note 2) |
| : | | | |
| FFE3h | ID2 | | (Note 2) |
| : | | | |
| FFEBh | ID3 | | (Note 2) |
| : | | | |
| FFEFh | ID4 | | (Note 2) |
| : | | | |
| FFF3h | ID5 | | (Note 2) |
| : | | | |
| FFF7h | ID6 | | (Note 2) |
| : | | | |
| FFFBh | ID7 | | (Note 2) |
| : | | | |
| FFFFh | Option Function Select Register | OFS | (Note 1) |

Notes:

1. The option function select area is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.
   Do not write additions to the option function select area. If the block including the option function select area is erased, the option function select area is set to FFh.
   When blank products are shipped, the option function select area is set to FFh. It is set to the written value after written by the user.
   When factory-programming products are shipped, the value of the option function select area is the value programmed by the user.
2. The ID code areas are allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.
   Do not write additions to the ID code areas. If the block including the ID code areas is erased, the ID code areas are set to FFh.
   When blank products are shipped, the ID code areas are set to FFh. They are set to the written value after written by the user.
   When factory-programming products are shipped, the value of the ID code areas is the value programmed by the user.

**Table 5.2 Recommended Operating Conditions (1)**

| Symbol | Parameter | | | | Conditions | Standard | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | Min. | Typ. | Max. | |
| $V_{CC}$/$AV_{CC}$ | Supply voltage | | | | | 1.8 | — | 5.5 | V |
| $V_{SS}$/$AV_{SS}$ | Supply voltage | | | | | — | 0 | — | V |
| $V_{IH}$ | Input “H” voltage | Other than CMOS input | | | | 0.8 $V_{CC}$ | — | $V_{CC}$ | V |
| | | CMOS input | Input level switching function (I/O port) | Input level selection: 0.35 $V_{CC}$ | 4.0 V ≤ $V_{CC}$ ≤ 5.5 V | 0.5 $V_{CC}$ | — | $V_{CC}$ | V |
| | | | | | 2.7 V ≤ $V_{CC}$ < 4.0 V | 0.55 $V_{CC}$ | — | $V_{CC}$ | V |
| | | | | | 1.8 V ≤ $V_{CC}$ < 2.7 V | 0.65 $V_{CC}$ | — | $V_{CC}$ | V |
| | | | | Input level selection: 0.5 $V_{CC}$ | 4.0 V ≤ $V_{CC}$ ≤ 5.5 V | 0.65 $V_{CC}$ | — | $V_{CC}$ | V |
| | | | | | 2.7 V ≤ $V_{CC}$ < 4.0 V | 0.7 $V_{CC}$ | — | $V_{CC}$ | V |
| | | | | | 1.8 V ≤ $V_{CC}$ < 2.7 V | 0.8 $V_{CC}$ | — | $V_{CC}$ | V |
| | | | | Input level selection: 0.7 $V_{CC}$ | 4.0 V ≤ $V_{CC}$ ≤ 5.5 V | 0.85 $V_{CC}$ | — | $V_{CC}$ | V |
| | | | | | 2.7 V ≤ $V_{CC}$ < 4.0 V | 0.85 $V_{CC}$ | — | $V_{CC}$ | V |
| | | | | | 1.8 V ≤ $V_{CC}$ < 2.7 V | 0.85 $V_{CC}$ | — | $V_{CC}$ | V |
| | | External clock input (XOUT) | | | | 1.2 | — | $V_{CC}$ | V |
| $V_{IL}$ | Input “L” voltage | Other than CMOS input | | | | 0 | — | 0.2 $V_{CC}$ | V |
| | | CMOS input | Input level switching function (I/O port) | Input level selection: 0.35 $V_{CC}$ | 4.0 V ≤ $V_{CC}$ ≤ 5.5 V | 0 | — | 0.2 $V_{CC}$ | V |
| | | | | | 2.7 V ≤ $V_{CC}$ < 4.0 V | 0 | — | 0.2 $V_{CC}$ | V |
| | | | | | 1.8 V ≤ $V_{CC}$ < 2.7 V | 0 | — | 0.2 $V_{CC}$ | V |
| | | | | Input level selection: 0.5 $V_{CC}$ | 4.0 V ≤ $V_{CC}$ ≤ 5.5 V | 0 | — | 0.4 $V_{CC}$ | V |
| | | | | | 2.7 V ≤ $V_{CC}$ < 4.0 V | 0 | — | 0.3 $V_{CC}$ | V |
| | | | | | 1.8 V ≤ $V_{CC}$ < 2.7 V | 0 | — | 0.2 $V_{CC}$ | V |
| | | | | Input level selection: 0.7 $V_{CC}$ | 4.0 V ≤ $V_{CC}$ ≤ 5.5 V | 0 | — | 0.55 $V_{CC}$ | V |
| | | | | | 2.7 V ≤ $V_{CC}$ < 4.0 V | 0 | — | 0.45 $V_{CC}$ | V |
| | | | | | 1.8 V ≤ $V_{CC}$ < 2.7 V | 0 | — | 0.35 $V_{CC}$ | V |
| | | External clock input (XOUT) | | | | 0 | — | 0.4 | V |
| $I_{OH(sum)}$ | Peak sum output “H” current | Sum of all pins $I_{OH(peak)}$ | | | | — | — | –160 | mA |
| $I_{OH(sum)}$ | Average sum output “H” current | Sum of all pins $I_{OH(avg)}$ | | | | — | — | –80 | mA |
| $I_{OH(peak)}$ | Peak output “H” current | Drive capacity Low | | | | — | — | –10 | mA |
| | | Drive capacity High | | | | — | — | –40 | mA |
| $I_{OH(avg)}$ | Average output “H” current | Drive capacity Low | | | | — | — | –5 | mA |
| | | Drive capacity High | | | | — | — | –20 | mA |
| $I_{OL(sum)}$ | Peak sum output “L” current | Sum of all pins $I_{OL(peak)}$ | | | | — | — | 160 | mA |
| $I_{OL(sum)}$ | Average sum output “L” current | Sum of all pins $I_{OL(avg)}$ | | | | — | — | 80 | mA |
| $I_{OL(peak)}$ | Peak output “L” current | Drive capacity Low | | | | — | — | 10 | mA |
| | | Drive capacity High | | | | — | — | 40 | mA |
| $I_{OL(avg)}$ | Average output “L” current | Drive capacity Low | | | | — | — | 5 | mA |
| | | Drive capacity High | | | | — | — | 20 | mA |
| $f_{(XIN)}$ | XIN clock input oscillation frequency | | | | 2.7 V ≤ $V_{CC}$ ≤ 5.5 V | — | — | 20 | MHz |
| | | | | | 1.8 V ≤ $V_{CC}$ < 2.7 V | — | — | 5 | MHz |
| $f_{(XCIN)}$ | XCIN clock input oscillation frequency | | | | 1.8 V ≤ $V_{CC}$ ≤ 5.5 V | — | 32.768 | 50 | kHz |
| fOCO40M | When used as the count source for timer RC, timer RD or timer RG (3) | | | | 2.7 V ≤ $V_{CC}$ ≤ 5.5 V | 32 | — | 40 | MHz |
| fOCO-F | fOCO-F frequency | | | | 2.7 V ≤ $V_{CC}$ ≤ 5.5 V | — | — | 20 | MHz |
| | | | | | 1.8 V ≤ $V_{CC}$ < 2.7 V | — | — | 5 | MHz |
| — | System clock frequency | | | | 2.7 V ≤ $V_{CC}$ ≤ 5.5 V | — | — | 20 | MHz |
| | | | | | 1.8 V ≤ $V_{CC}$ < 2.7 V | — | — | 5 | MHz |
| $f_{(BCLK)}$ | CPU clock frequency | | | | 2.7 V ≤ $V_{CC}$ ≤ 5.5 V | — | — | 20 | MHz |
| | | | | | 1.8 V ≤ $V_{CC}$ < 2.7 V | — | — | 5 | MHz |

Notes:
1. $V_{CC}$ = 1.8 to 5.5 V and $T_{opr}$ = –20 to 85 °C (N version)/–40 to 85 °C (D version), unless otherwise specified.
2. The average output current indicates the average value of current measured during 100 ms.
3. fOCO40M can be used as the count source for timer RC, timer RD, or timer RG in the range of $V_{CC}$ = 2.7 to 5.5 V.

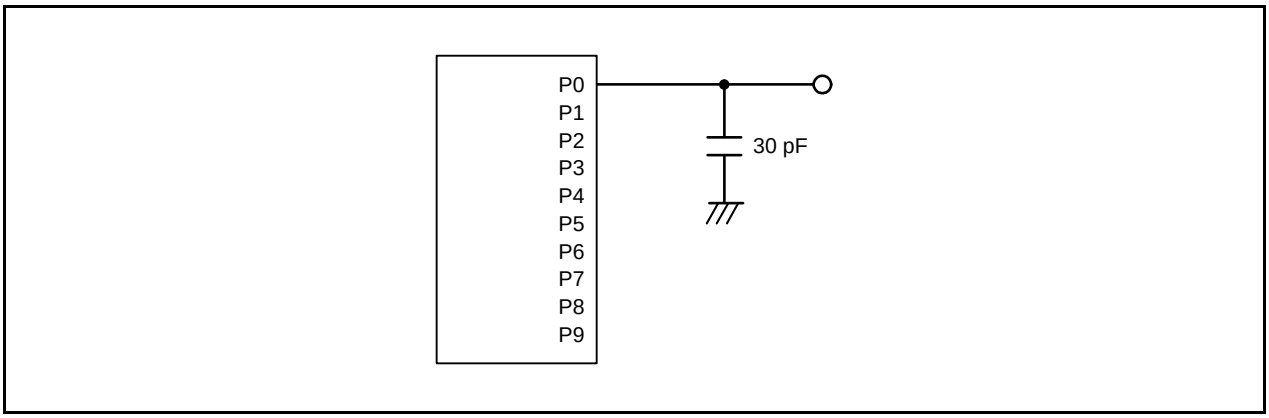



**Figure 5.1 Ports P0 to P9 Timing Measurement Circuit**

### Table 5.8 Voltage Detection 0 Circuit Electrical Characteristics

| Symbol | Parameter | Condition | Standard | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| $V_{det0}$ | Voltage detection level Vdet0_0 (2) | | 1.80 | 1.90 | 2.05 | V |
| | Voltage detection level Vdet0_1 (2) | | 2.15 | 2.35 | 2.50 | V |
| | Voltage detection level Vdet0_2 (2) | | 2.70 | 2.85 | 3.05 | V |
| | Voltage detection level Vdet0_3 (2) | | 3.55 | 3.80 | 4.05 | V |
| — | Voltage detection 0 circuit response time (4) | At the falling of $V_{CC}$ from 5.0 V to (Vdet0_0 – 0.1) V | — | 6 | 150 | µs |
| — | Voltage detection circuit self power consumption | VCA25 = 1, $V_{CC}$ = 5.0 V | — | 1.5 | — | µA |
| $t_{d(E-A)}$ | Waiting time until voltage detection circuit operation starts (3) | | — | — | 100 | µs |

Notes:
1. The measurement condition is $V_{CC}$ = 1.8 to 5.5 V and $T_{opr}$ = –20 to 85 °C (N version)/–40 to 85 °C (D version).
2. Select the voltage detection level with bits VDSEL0 and VDSEL1 in the OFS register.
3. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA25 bit in the VCA2 register to 0.
4. Time until the voltage monitor 0 reset is generated after the voltage passes $V_{det0}$.

### Table 5.9 Voltage Detection 1 Circuit Electrical Characteristics

| Symbol | Parameter | Condition | Standard | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| $V_{det1}$ | Voltage detection level Vdet1_0 (2) | At the falling of $V_{CC}$ | 2.00 | 2.20 | 2.40 | V |
| | Voltage detection level Vdet1_1 (2) | At the falling of $V_{CC}$ | 2.15 | 2.35 | 2.55 | V |
| | Voltage detection level Vdet1_2 (2) | At the falling of $V_{CC}$ | 2.30 | 2.50 | 2.70 | V |
| | Voltage detection level Vdet1_3 (2) | At the falling of $V_{CC}$ | 2.45 | 2.65 | 2.85 | V |
| | Voltage detection level Vdet1_4 (2) | At the falling of $V_{CC}$ | 2.60 | 2.80 | 3.00 | V |
| | Voltage detection level Vdet1_5 (2) | At the falling of $V_{CC}$ | 2.75 | 2.95 | 3.15 | V |
| | Voltage detection level Vdet1_6 (2) | At the falling of $V_{CC}$ | 2.85 | 3.10 | 3.40 | V |
| | Voltage detection level Vdet1_7 (2) | At the falling of $V_{CC}$ | 3.00 | 3.25 | 3.55 | V |
| | Voltage detection level Vdet1_8 (2) | At the falling of $V_{CC}$ | 3.15 | 3.40 | 3.70 | V |
| | Voltage detection level Vdet1_9 (2) | At the falling of $V_{CC}$ | 3.30 | 3.55 | 3.85 | V |
| | Voltage detection level Vdet1_A (2) | At the falling of $V_{CC}$ | 3.45 | 3.70 | 4.00 | V |
| | Voltage detection level Vdet1_B (2) | At the falling of $V_{CC}$ | 3.60 | 3.85 | 4.15 | V |
| | Voltage detection level Vdet1_C (2) | At the falling of $V_{CC}$ | 3.75 | 4.00 | 4.30 | V |
| | Voltage detection level Vdet1_D (2) | At the falling of $V_{CC}$ | 3.90 | 4.15 | 4.45 | V |
| | Voltage detection level Vdet1_E (2) | At the falling of $V_{CC}$ | 4.05 | 4.30 | 4.60 | V |
| | Voltage detection level Vdet1_F (2) | At the falling of $V_{CC}$ | 4.20 | 4.45 | 4.75 | V |
| — | Hysteresis width at the rising of $V_{CC}$ in voltage detection 1 circuit | Vdet1_0 to Vdet1_5 selected | — | 0.07 | — | V |
| | | Vdet1_6 to Vdet1_F selected | — | 0.10 | — | V |
| — | Voltage detection 1 circuit response time (3) | At the falling of $V_{CC}$ from 5.0 V to (Vdet1_0 – 0.1) V | — | 60 | 150 | µs |
| — | Voltage detection circuit self power consumption | VCA26 = 1, $V_{CC}$ = 5.0 V | — | 1.7 | — | µA |
| $t_{d(E-A)}$ | Waiting time until voltage detection circuit operation starts (4) | | — | — | 100 | µs |

Notes:
1. The measurement condition is $V_{CC}$ = 1.8 to 5.5 V and $T_{opr}$ = –20 to 85 °C (N version)/–40 to 85 °C (D version).
2. Select the voltage detection level with bits VD1S0 to VD1S3 in the VD1LS register.
3. Time until the voltage monitor 1 interrupt request is generated after the voltage passes $V_{det1}$.
4. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA26 bit in the VCA2 register to 0.

**Table 5.10 Voltage Detection 2 Circuit Electrical Characteristics**

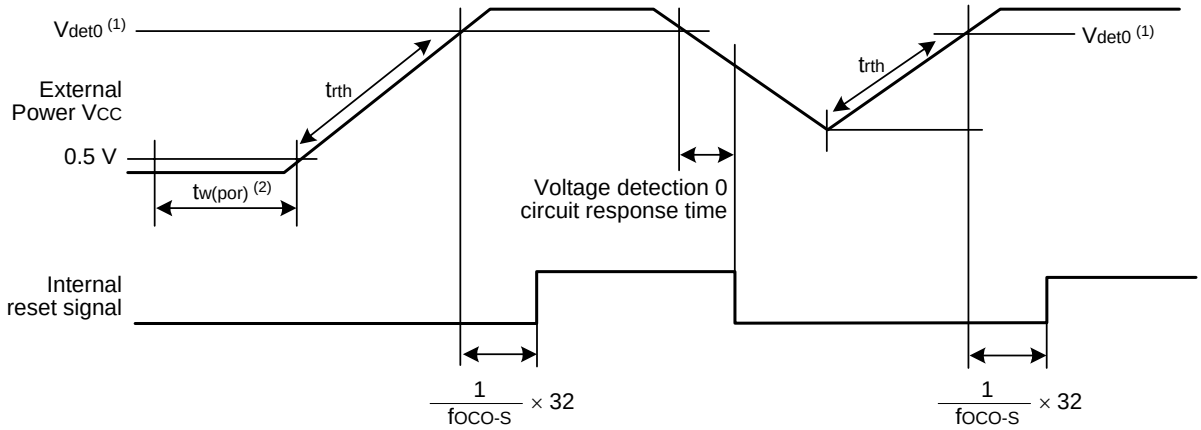
| Symbol | Parameter | Condition | Standard | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| $V_{det2}$ | Voltage detection level Vdet2_0 | At the falling of $V_{CC}$ | 3.70 | 4.00 | 4.30 | V |
| — | Hysteresis width at the rising of $V_{CC}$ in voltage detection 2 circuit | | — | 0.10 | — | V |
| — | Voltage detection 2 circuit response time (2) | At the falling of $V_{CC}$ from 5.0 V to (Vdet2_0 – 0.1) V | — | 20 | 150 | µs |
| — | Voltage detection circuit self power consumption | VCA27 = 1, $V_{CC}$ = 5.0 V | — | 1.7 | — | µA |
| $t_{d(E-A)}$ | Waiting time until voltage detection circuit operation starts (3) | | — | — | 100 | µs |

Notes:
1. The measurement condition is $V_{CC}$ = 1.8 to 5.5 V and $T_{opr}$ = –20 to 85 °C (N version)/–40 to 85 °C (D version).
2. Time until the voltage monitor 2 interrupt request is generated after the voltage passes $V_{det2}$.
3. Necessary time until the voltage detection circuit operates after setting to 1 again after setting the VCA27 bit in the VCA2 register to 0.

**Table 5.11 Power-on Reset Circuit (2)**

| Symbol | Parameter | Condition | Standard | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| $t_{rth}$ | External power $V_{CC}$ rise gradient | (1) | 0 | — | 50,000 | mV/msec |

Notes:
1. The measurement condition is $T_{opr}$ = –20 to 85 °C (N version)/–40 to 85 °C (D version), unless otherwise specified.
2. To use the power-on reset function, enable voltage monitor 0 reset by setting the LVDAS bit in the OFS register to 0.




Notes:
1. $V_{det0}$ indicates the voltage detection level of the voltage detection 0 circuit. Refer to **6. Voltage Detection Circuit** of User's Manual: Hardware (R01UH0094EJ0110) for details.
2. $t_{w(por)}$ indicates the duration the external power $V_{CC}$ must be held below the valid voltage (0.5 V) to enable a power-on reset. When turning on the power after it falls with voltage monitor 0 reset disabled, maintain $t_{w(por)}$ for 1 ms or more.

**Figure 5.3 Power-on Reset Circuit Electrical Characteristics**

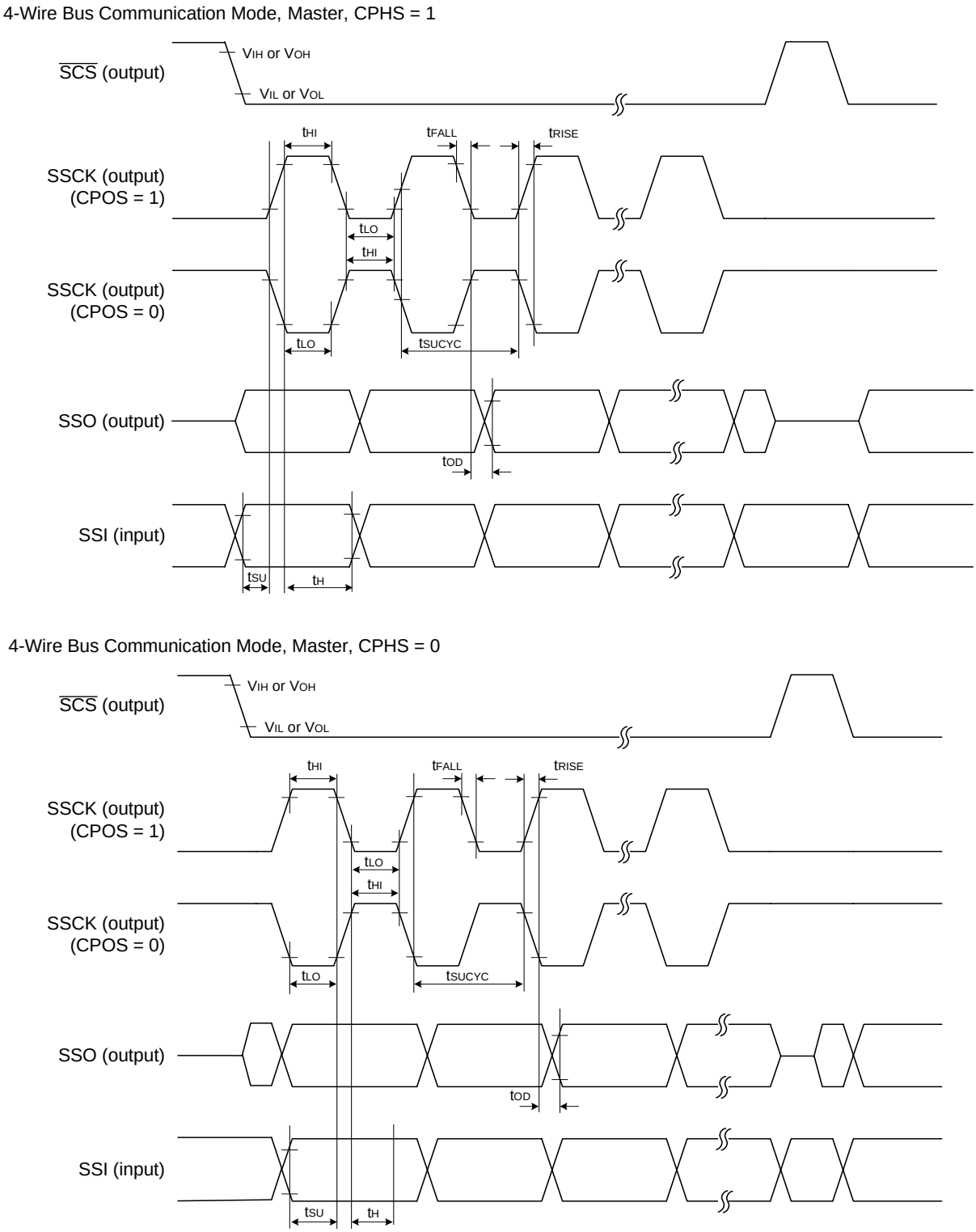



**Figure 5.4 I/O Timing of Synchronous Serial Communication Unit (SSU) (Master)**

**Table 5.17 Electrical Characteristics (1) [4.2 V ≤ Vcc ≤ 5.5 V]**

| Symbol | Parameter | | Condition | | Standard | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min. | Typ. | Max. | |
| $V_{OH}$ | Output "H" voltage | Other than XOUT | Drive capacity High $V_{CC}$ = 5 V | $I_{OH}$ = –20 mA | $V_{CC}$ – 2.0 | — | $V_{CC}$ | V |
| | | | Drive capacity Low $V_{CC}$ = 5 V | $I_{OH}$ = –5 mA | $V_{CC}$ – 2.0 | — | $V_{CC}$ | V |
| | | XOUT | $V_{CC}$ = 5 V | $I_{OH}$ = –200 µA | 1.0 | — | $V_{CC}$ | V |
| $V_{OL}$ | Output "L" voltage | Other than XOUT | Drive capacity High $V_{CC}$ = 5 V | $I_{OL}$ = 20 mA | — | — | 2.0 | V |
| | | | Drive capacity Low $V_{CC}$ = 5 V | $I_{OL}$ = 5 mA | — | — | 2.0 | V |
| | | XOUT | $V_{CC}$ = 5 V | $I_{OL}$ = 200 µA | — | — | 0.5 | V |
| $V_{T+}$-$V_{T-}$ | Hysteresis | $\overline{INT0}$, $\overline{INT1}$, $\overline{INT2}$, $\overline{INT3}$, $\overline{INT4}$, $\overline{KI0}$, $\overline{KI1}$, $\overline{KI2}$, $\overline{KI3}$, TRAIO, TRBO, TRCIOA, TRCIOB, TRCIOC, TRCIOD, TRDIOA0, TRDIOB0, TRDIOC0, TRDIOD0, TRDIOA1, TRDIOB1, TRDIOC1, TRDIOD1, TRCTRG, TRCCLK, TRFI, $\overline{TRGIOA}$, $\overline{TRGIOB}$, $\overline{ADTRG}$, RXD0, RXD1, RXD2, CLK0, CLK1, CLK2, SSI, SCL, SDA, SSO | | | 0.1 | 1.2 | — | V |
| | | $\overline{RESET}$ | | | 0.1 | 1.2 | — | V |
| $I_{IH}$ | Input "H" current | | $V_I$ = 5 V, $V_{CC}$ = 5.0 V | | — | — | 5.0 | µA |
| $I_{IL}$ | Input "L" current | | $V_I$ = 0 V, $V_{CC}$ = 5.0 V | | — | — | –5.0 | µA |
| $R_{PULLUP}$ | Pull-up resistance | | $V_I$ = 0 V, $V_{CC}$ = 5.0 V | | 25 | 50 | 100 | kΩ |
| $R_{fXIN}$ | Feedback resistance | XIN | | | — | 0.3 | — | MΩ |
| $R_{fXCIN}$ | Feedback resistance | XCIN | | | — | 8 | — | MΩ |
| $V_{RAM}$ | RAM hold voltage | | During stop mode | | 1.8 | — | — | V |

Note:
1. 4.2 V ≤ $V_{CC}$ ≤ 5.5 V, $T_{opr}$ = –20 to 85 °C (N version)/–40 to 85 °C (D version), and f(XIN) = 20 MHz, unless otherwise specified.

**Table 5.24 Electrical Characteristics (3) [2.7 V ≤ Vcc < 4.2 V]**

| Symbol | Parameter | | Condition | | Standard | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min. | Typ. | Max. | |
| $V_{OH}$ | Output “H” voltage | Other than XOUT | Drive capacity High | $I_{OH}$ = –5 mA | $V_{CC}$ – 0.5 | — | $V_{CC}$ | V |
| | | | Drive capacity Low | $I_{OH}$ = –1 mA | $V_{CC}$ – 0.5 | — | $V_{CC}$ | V |
| | | XOUT | | $I_{OH}$ = –200 μA | 1.0 | — | $V_{CC}$ | V |
| $V_{OL}$ | Output “L” voltage | Other than XOUT | Drive capacity High | $I_{OL}$ = 5 mA | — | — | 0.5 | V |
| | | | Drive capacity Low | $I_{OL}$ = 1 mA | — | — | 0.5 | V |
| | | XOUT | | $I_{OL}$ = 200 μA | — | — | 0.5 | V |
| $V_{T+}$-$V_{T-}$ | Hysteresis | $\overline{INT0}$, $\overline{INT1}$, $\overline{INT2}$, $\overline{INT3}$, $\overline{INT4}$, $\overline{KI0}$, $\overline{KI1}$, $\overline{KI2}$, $\overline{KI3}$, TRAIO, TRBO, TRCIOA, TRCIOB, TRCIOC, TRCIOD, TRDIOA0, TRDIOB0, TRDIOC0, TRDIOD0, TRDIOA1, TRDIOB1, TRDIOC1, TRDIOD1, TRCTRG, TRCCLK, TRFI, $\overline{TRGIOA}$, TRGIOB, $\overline{ADTRG}$, RXD0, RXD1, RXD2, CLK0, CLK1, CLK2, SSI, SCL, SDA, SSO | $V_{CC}$ = 3.0 V | | 0.1 | 0.4 | — | V |
| | | $\overline{RESET}$ | $V_{CC}$ = 3.0 V | | 0.1 | 0.5 | — | V |
| $I_{IH}$ | Input “H” current | | $V_I$ = 3 V, $V_{CC}$ = 3.0 V | | — | — | 4.0 | μA |
| $I_{IL}$ | Input “L” current | | $V_I$ = 0 V, $V_{CC}$ = 3.0 V | | — | — | –4.0 | μA |
| $R_{PULLUP}$ | Pull-up resistance | | $V_I$ = 0 V, $V_{CC}$ = 3.0 V | | 42 | 84 | 168 | kΩ |
| $R_{fXIN}$ | Feedback resistance | XIN | | | — | 0.3 | — | MΩ |
| $R_{fXCIN}$ | Feedback resistance | XCIN | | | — | 8 | — | MΩ |
| $V_{RAM}$ | RAM hold voltage | | During stop mode | | 1.8 | — | — | V |

Note:
1. 2.7 V ≤ $V_{CC}$ < 4.2 V, $T_{opr}$ = –20 to 85 °C (N version)/–40 to 85 °C (D version), and f(XIN) = 10 MHz, unless otherwise specified.

**Timing requirements (Unless Otherwise Specified: $V_{CC}$ = 3 V, $V_{SS}$ = 0 V, $T_{opr}$ = 25 °C)**

**Table 5.26 External Clock Input (XOUT, XCIN)**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(XOUT)}$ | XOUT input cycle time | 50 | — | ns |
| $t_{WH(XOUT)}$ | XOUT input “H” width | 24 | — | ns |
| $t_{WL(XOUT)}$ | XOUT input “L” width | 24 | — | ns |
| $t_{c(XCIN)}$ | XCIN input cycle time | 14 | — | µs |
| $t_{WH(XCIN)}$ | XCIN input “H” width | 7 | — | µs |
| $t_{WL(XCIN)}$ | XCIN input “L” width | 7 | — | µs |

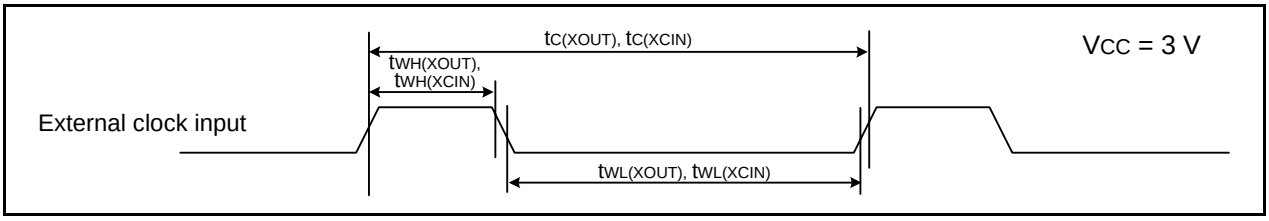



**Figure 5.13 External Clock Input Timing Diagram when $V_{CC}$ = 3 V**

**Table 5.27 TRAIO Input**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(TRAIO)}$ | TRAIO input cycle time | 300 | — | ns |
| $t_{WH(TRAIO)}$ | TRAIO input “H” width | 120 | — | ns |
| $t_{WL(TRAIO)}$ | TRAIO input “L” width | 120 | — | ns |

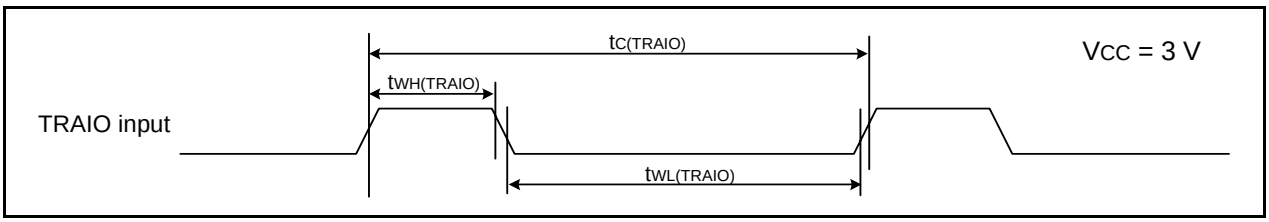



**Figure 5.14 TRAIO Input Timing Diagram when $V_{CC}$ = 3 V**

**Table 5.28 TRFI Input**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(TRFI)}$ | TRFI input cycle time | 1200 (1) | — | ns |
| $t_{WH(TRFI)}$ | TRFI input “H” width | 600 (2) | — | ns |
| $t_{WL(TRFI)}$ | TRFI input “L” width | 600 (2) | — | ns |

Notes:
1. When using timer RF input capture mode, adjust the cycle time to (1/timer RF count source frequency × 3) or above.
2. When using timer RF input capture mode, adjust the pulse width to (1/timer RF count source frequency × 1.5) or above.

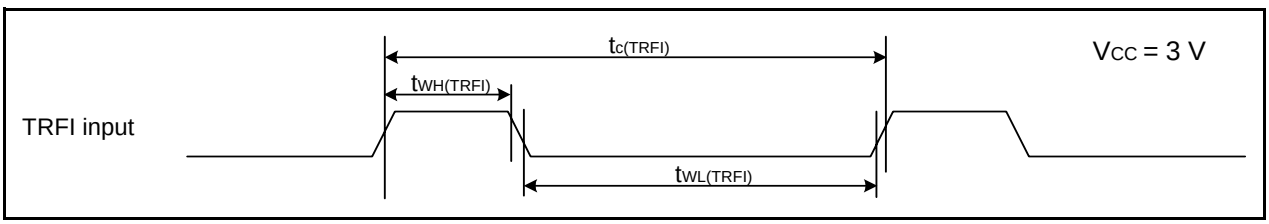



**Figure 5.15 TRFI Input Timing Diagram when $V_{CC}$ = 3 V**

**Timing requirements (Unless Otherwise Specified: $V_{CC}$ = 2.2 V, $V_{SS}$ = 0 V, $T_{opr}$ = 25 °C)**

**Table 5.33 External Clock Input (XOUT, XCIN)**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(XOUT)}$ | XOUT input cycle time | 200 | — | ns |
| $t_{WH(XOUT)}$ | XOUT input “H” width | 90 | — | ns |
| $t_{WL(XOUT)}$ | XOUT input “L” width | 90 | — | ns |
| $t_{c(XCIN)}$ | XCIN input cycle time | 14 | — | µs |
| $t_{WH(XCIN)}$ | XCIN input “H” width | 7 | — | µs |
| $t_{WL(XCIN)}$ | XCIN input “L” width | 7 | — | µs |

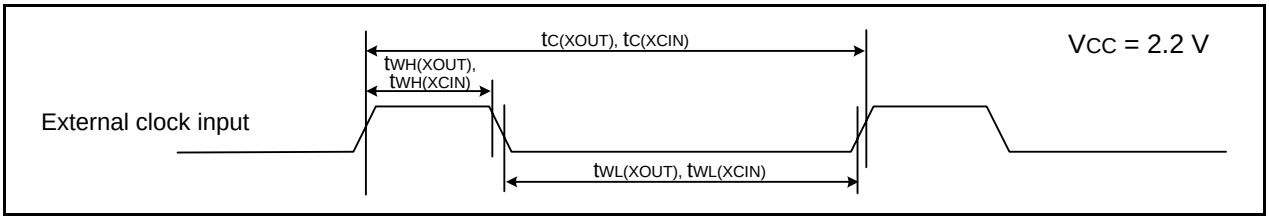



**Figure 5.18 External Clock Input Timing Diagram when $V_{CC}$ = 2.2 V**

**Table 5.34 TRAIO Input**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(TRAIO)}$ | TRAIO input cycle time | 500 | — | ns |
| $t_{WH(TRAIO)}$ | TRAIO input “H” width | 200 | — | ns |
| $t_{WL(TRAIO)}$ | TRAIO input “L” width | 200 | — | ns |

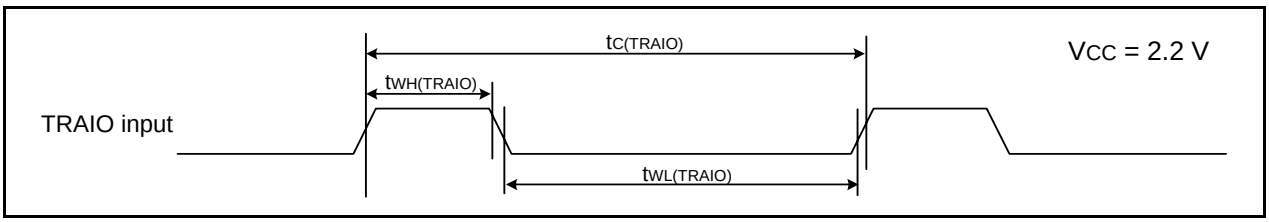



**Figure 5.19 TRAIO Input Timing Diagram when $V_{CC}$ = 2.2 V**

**Table 5.35 TRFI Input**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(TRFI)}$ | TRFI input cycle time | 2000 (1) | — | ns |
| $t_{WH(TRFI)}$ | TRFI input “H” width | 1000 (2) | — | ns |
| $t_{WL(TRFI)}$ | TRFI input “L” width | 1000 (2) | — | ns |

Notes:
1. When using timer RF input capture mode, adjust the cycle time to (1/timer RF count source frequency × 3) or above.
2. When using timer RF input capture mode, adjust the pulse width to (1/timer RF count source frequency × 1.5) or above.

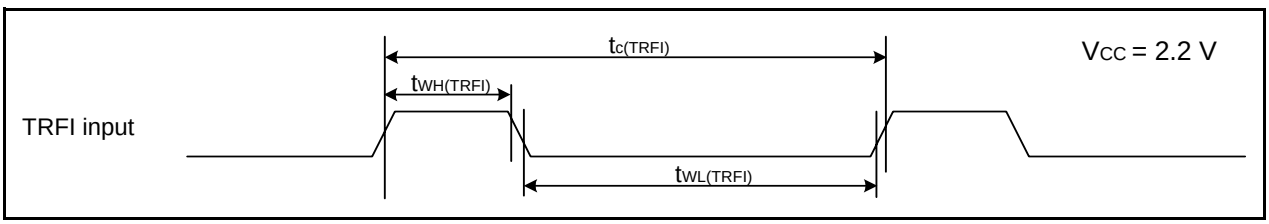



**Figure 5.20 TRFI Input Timing Diagram when $V_{CC}$ = 2.2 V**

**Table 5.36 Serial Interface**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(CK)}$ | CLKi input cycle time | 800 | — | ns |
| $t_{W(CKH)}$ | CLKi input “H” width | 400 | — | ns |
| $t_{W(CKL)}$ | CLKi input “L” width | 400 | — | ns |
| $t_{d(C-Q)}$ | TXDi output delay time | — | 200 | ns |
| $t_{h(C-Q)}$ | TXDi hold time | 0 | — | ns |
| $t_{su(D-C)}$ | RXDi input setup time | 150 | — | ns |
| $t_{h(C-D)}$ | RXDi input hold time | 90 | — | ns |

i = 0 to 2

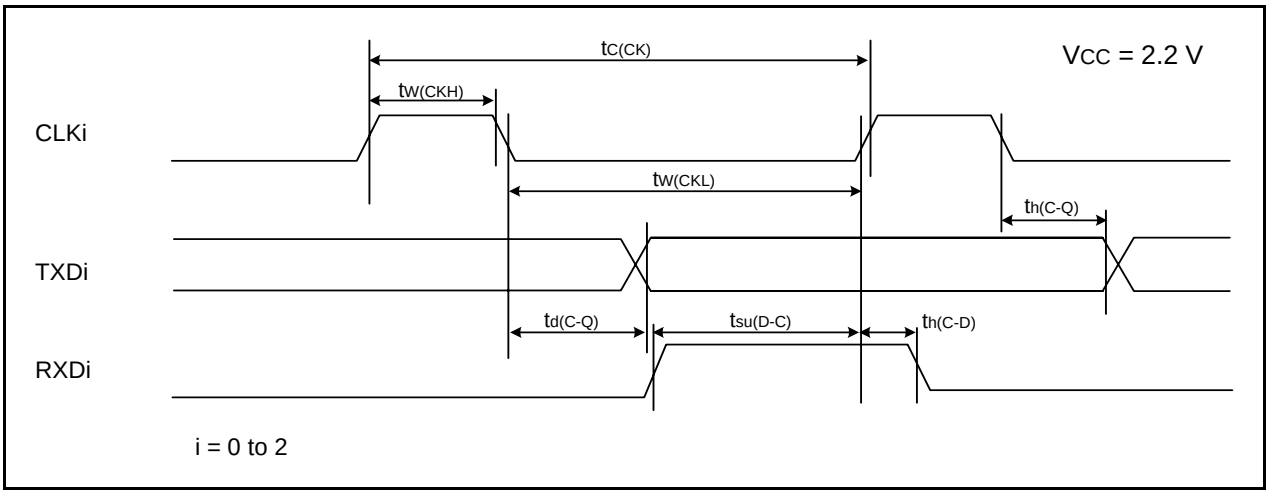



**Figure 5.21 Serial Interface Timing Diagram when Vcc = 2.2 V**

**Table 5.37 External Interrupt $\overline{INTi}$ (i = 0 to 4) Input, Key Input Interrupt $\overline{KIi}$ (i = 0 to 3)**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{W(INH)}$ | $\overline{INTi}$ input “H” width, $\overline{KIi}$ input “H” width | 1000 (1) | — | ns |
| $t_{W(INL)}$ | $\overline{INTi}$ input “L” width, $\overline{KIi}$ input “L” width | 1000 (2) | — | ns |

Notes:
1. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

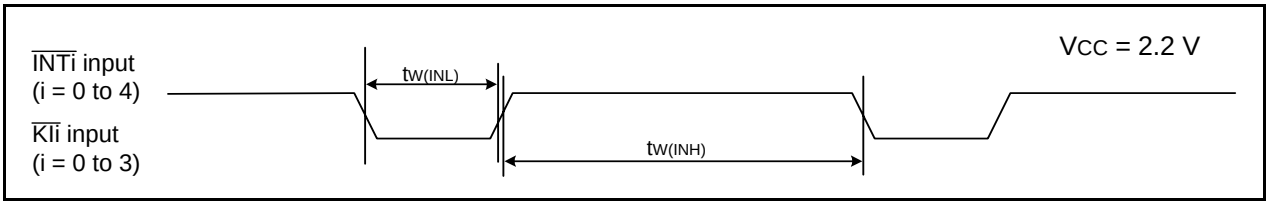



**Figure 5.22 Input Timing Diagram for External Interrupt $\overline{INTi}$ and Key Input Interrupt $\overline{KIi}$ when Vcc = 2.2 V**