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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	I ² C, LINbus, SIO, SSU, UART/USART
Peripherals	POR, PWM, Voltage Detect, WDT
Number of I/O	75
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	10K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 20x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f2138ccnfp-v0

1.1.2 Specifications

Tables 1.1 and 1.2 outline the Specifications for R8C/38C Group.

Table 1.1 Specifications for R8C/38C Group (1)

Item	Function	Specification
CPU	Central processing unit	R8C CPU core • Number of fundamental instructions: 89 • Minimum instruction execution time: 50 ns (f(XIN) = 20 MHz, VCC = 2.7 to 5.5 V) 200 ns (f(XIN) = 5 MHz, VCC = 1.8 to 5.5 V) • Multiplier: 16 bits × 16 bits → 32 bits • Multiply-accumulate instruction: 16 bits × 16 bits + 32 bits → 32 bits • Operation mode: Single-chip mode (address space: 1 Mbyte)
Memory	ROM, RAM, Data flash	Refer to Table 1.3 Product List for R8C/38C Group
Power Supply Voltage Detection	Voltage detection circuit	• Power-on reset • Voltage detection 3 (detection level of voltage detection 0 and voltage detection 1 selectable)
I/O Ports	Programmable I/O ports	• Input-only: 1 pin • CMOS I/O ports: 75, selectable pull-up resistor • High current drive ports: 75
Clock	Clock generation circuits	• 4 circuits: XIN clock oscillation circuit, XCIN clock oscillation circuit (32 kHz), High-speed on-chip oscillator (with frequency adjustment function), Low-speed on-chip oscillator • Oscillation stop detection: XIN clock oscillation stop detection function • Frequency divider circuit: Dividing selectable 1, 2, 4, 8, and 16 • Low power consumption modes: - Standard operating mode (high-speed clock, low-speed clock, high-speed on-chip oscillator, low-speed on-chip oscillator), wait mode, stop mode
		Real-time clock (timer RE)
Interrupts		• Interrupt Vectors: 69 • External: 9 sources ($\overline{INT} \times 5$, key input $\times 4$) • Priority levels: 7 levels
Watchdog Timer		• 14 bits × 1 (with prescaler) • Reset start selectable • Low-speed on-chip oscillator for watchdog timer selectable
DTC (Data Transfer Controller)		• 1 channel • Activation sources: 39 • Transfer modes: 2 (normal mode, repeat mode)
Timer	Timer RA	8 bits × 1 (with 8-bit prescaler) Timer mode (period timer), pulse output mode (output level inverted every period), event counter mode, pulse width measurement mode, pulse period measurement mode
	Timer RB	8 bits × 1 (with 8-bit prescaler) Timer mode (period timer), programmable waveform generation mode (PWM output), programmable one-shot generation mode, programmable wait one-shot generation mode
	Timer RC	16 bits × 1 (with 4 capture/compare registers) Timer mode (input capture function, output compare function), PWM mode (output 3 pins), PWM2 mode (PWM output pin)
	Timer RD	16 bits × 2 (with 4 capture/compare registers) Timer mode (input capture function, output compare function), PWM mode (output 6 pins), reset synchronous PWM mode (output three-phase waveforms (6 pins), sawtooth wave modulation), complementary PWM mode (output three-phase waveforms (6 pins), triangular wave modulation), PWM3 mode (PWM output 2 pins with fixed period)

1.4 Pin Assignment

Figure 1.3 shows Pin Assignment (Top View). Tables 1.4 and 1.5 outline the Pin Name Information by Pin Number.

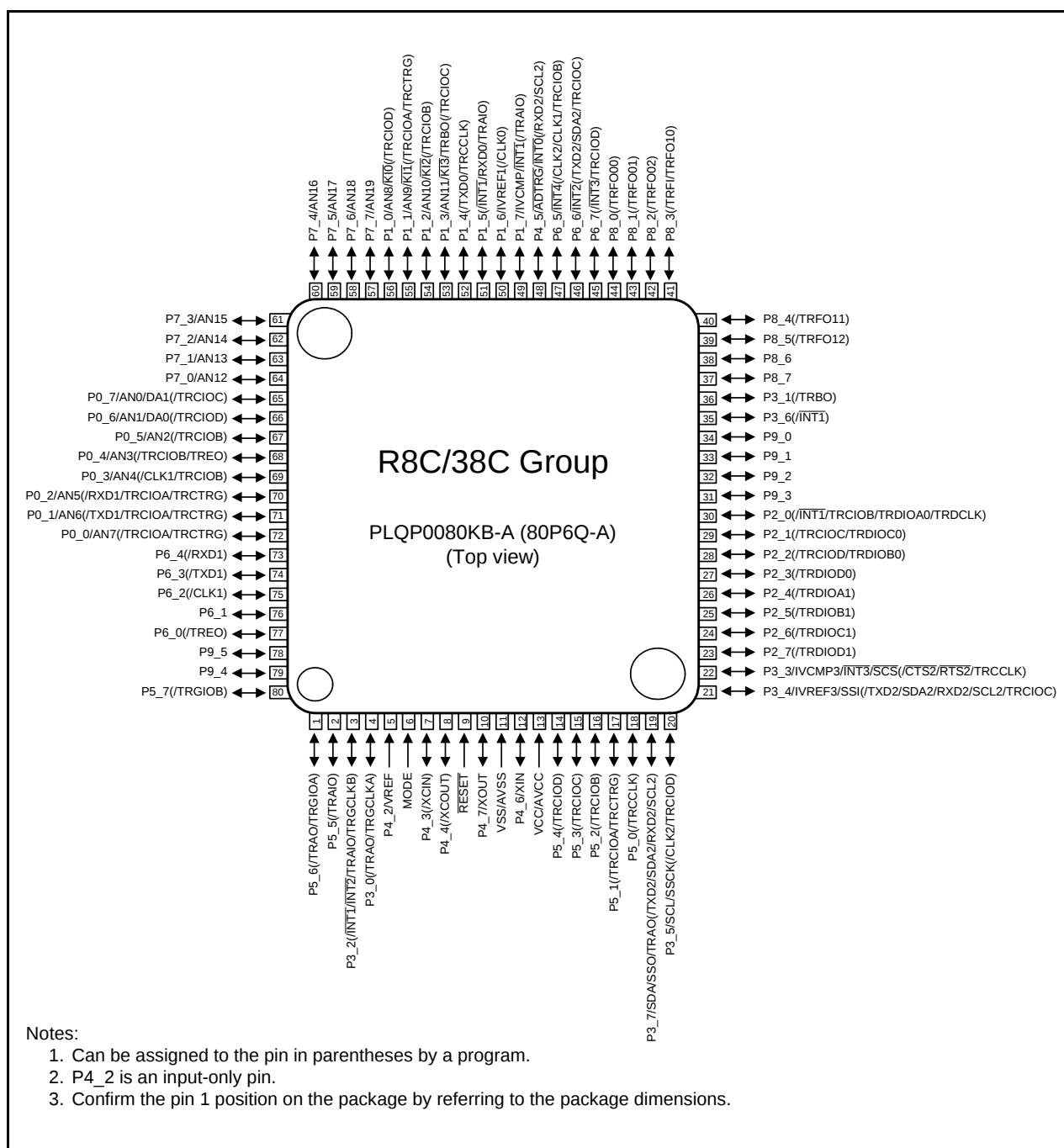


Figure 1.3 Pin Assignment (Top View)

Table 1.4 Pin Name Information by Pin Number (1)

Pin Number	Control Pin	Port	I/O Pin Functions for Peripheral Modules					
			Interrupt	Timer	Serial Interface	SSU	I ² C bus	A/D Converter, D/A Converter, Comparator B
1		P5_6		(TRA0/TRGIOA)				
2		P5_5		(TRAIO)				
3		P3_2	($\overline{\text{INT1}}$ / $\overline{\text{INT2}}$)	(TRAIO/TRGCLKB)				
4		P3_0		(TRA0/TRGCLKA)				
5		P4_2						VREF
6	MODE							
7	(XCIN)	P4_3						
8	(XCOUT)	P4_4						
9	$\overline{\text{RESET}}$							
10	XOUT	P4_7						
11	VSS/AVSS							
12	XIN	P4_6						
13	VCC/AVCC							
14		P5_4		(TRCIOD)				
15		P5_3		(TRCIOC)				
16		P5_2		(TRCIOB)				
17		P5_1		(TRCIOA/TRCTRG)				
18		P5_0		(TRCCLK)				
19		P3_7		TRA0	(TXD2/SDA2/ RXD2/SCL2)	SSO	SDA	
20		P3_5		(TRCIOD)	(CLK2)	SSCK	SCL	
21		P3_4		(TRCIOC)	(TXD2/SDA2/ RXD2/SCL2)	SSI		IVREF3
22		P3_3	$\overline{\text{INT3}}$	(TRCCLK)	(CTS2/RTS2)	$\overline{\text{SCS}}$		IVCMP3
23		P2_7		(TRDIOD1)				
24		P2_6		(TRDIOC1)				
25		P2_5		(TRDIOB1)				
26		P2_4		(TRDIOA1)				
27		P2_3		(TRDIOD0)				
28		P2_2		(TRCIOD/TRDIOB0)				
29		P2_1		(TRCIOC/TRDIOC0)				
30		P2_0	($\overline{\text{INT1}}$)	(TRCIOB/TRDIOA0/ TRDCLK)				
31		P9_3						
32		P9_2						
33		P9_1						
34		P9_0						
35		P3_6	($\overline{\text{INT1}}$)					
36		P3_1		(TRBO)				
37		P8_7						
38		P8_6						
39		P8_5		(TRFO12)				
40		P8_4		(TRFO11)				

Note:

1. Can be assigned to the pin in parentheses by a program.

1.5 Pin Functions

Tables 1.6 and 1.7 list Pin Functions.

Table 1.6 Pin Functions (1)

Item	Pin Name	I/O Type	Description
Power supply input	VCC, VSS	—	Apply 1.8 to 5.5 V to the VCC pin. Apply 0 V to the VSS pin.
Analog power supply input	AVCC, AVSS	—	Power supply for the A/D converter. Connect a capacitor between AVCC and AVSS.
Reset input	RESET	I	Input "L" on this pin resets the MCU.
MODE	MODE	I	Connect this pin to VCC via a resistor.
XIN clock input	XIN	I	These pins are provided for XIN clock generation circuit I/O. Connect a ceramic resonator or a crystal oscillator between the XIN and XOUT pins. ⁽¹⁾ To use an external clock, input it to the XOUT pin and leave the XIN pin open.
XIN clock output	XOUT	I/O	
XCIN clock input	XCIN	I	These pins are provided for XCIN clock generation circuit I/O. Connect a crystal oscillator between the XCIN and XCOU pins. ⁽¹⁾ To use an external clock, input it to the XCIN pin and leave the XCOU pin open.
XCIN clock output	XCOU	O	
INT interrupt input	INT0 to INT4	I	INT interrupt input pins.
Key input interrupt	KI0 to KI3	I	Key input interrupt input pins.
Timer RA	TRAIO	I/O	Timer RA I/O pin.
	TRAO	O	Timer RA output pin.
Timer RB	TRBO	O	Timer RB output pin.
Timer RC	TRCCLK	I	External clock input pin.
	TRCTRG	I	External trigger input pin.
	TRCIOA, TRCIOB, TRCIOC, TRCIOD	I/O	Timer RC I/O pins.
Timer RD	TRDIOA0, TRDIOA1, TRDIOB0, TRDIOB1, TRDIOC0, TRDIOC1, TRDIOD0, TRDIOD1	I/O	Timer RD I/O pins.
	TRDCLK	I	External clock input pin.
Timer RE	TREO	O	Divided clock output pin.
Timer RF	TRFO00, TRFO10, TRFO01, TRFO11, TRFO02, TRFO12	O	Timer RF output pins.
	TRFI	I	Timer RF input pin.
Timer RG	TRGIOA, TRGIOB	I/O	Timer RG I/O ports.
	TRGCLKA, TRGCLKB	I	External clock input pins.
Serial interface	CLK0, CLK1, CLK2	I/O	Transfer clock I/O pins.
	RXD0, RXD1, RXD2	I	Serial data input pins.
	TXD0, TXD1, TXD2	O	Serial data output pins.
	CTS2	I	Transmission control input pin.
	RTS2	O	Reception control output pin.
	SCL2	I/O	I ² C mode clock I/O pin.
	SDA2	I/O	I ² C mode data I/O pin.

I: Input O: Output I/O: Input and output

Note:

1. Refer to the oscillator manufacturer for oscillation characteristics.

Table 1.7 Pin Functions (2)

Item	Pin Name	I/O Type	Description
SSU	SSI	I/O	Data I/O pin.
	$\overline{\text{SCS}}$	I/O	Chip-select signal I/O pin.
	SSCK	I/O	Clock I/O pin.
	SSO	I/O	Data I/O pin.
I ² C bus	SCL	I/O	Clock I/O pin
	SDA	I/O	Data I/O pin
Reference voltage input	VREF	I	Reference voltage input pin to A/D converter.
A/D converter	AN0 to AN19	I	Analog input pins to A/D converter.
	$\overline{\text{ADTRG}}$	I	AD external trigger input pin.
D/A converter	DA0, DA1	O	D/A converter output pins.
Comparator B	IVCMP1, IVCMP3	I	Comparator B analog voltage input pins.
	IVREF1, IVREF3	I	Comparator B reference voltage input pins.
I/O port	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_3 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_5	I/O	CMOS I/O ports. Each port has an I/O select direction register, allowing each pin in the port to be directed for input or output individually. Any port set to input can be set to use a pull-up resistor or not by a program.
Input port	P4_2	I	Input-only port.

I: Input O: Output I/O: Input and output

2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU Registers. The CPU contains 13 registers. R0, R1, R2, R3, A0, A1, and FB configure a register bank. There are two sets of register bank.

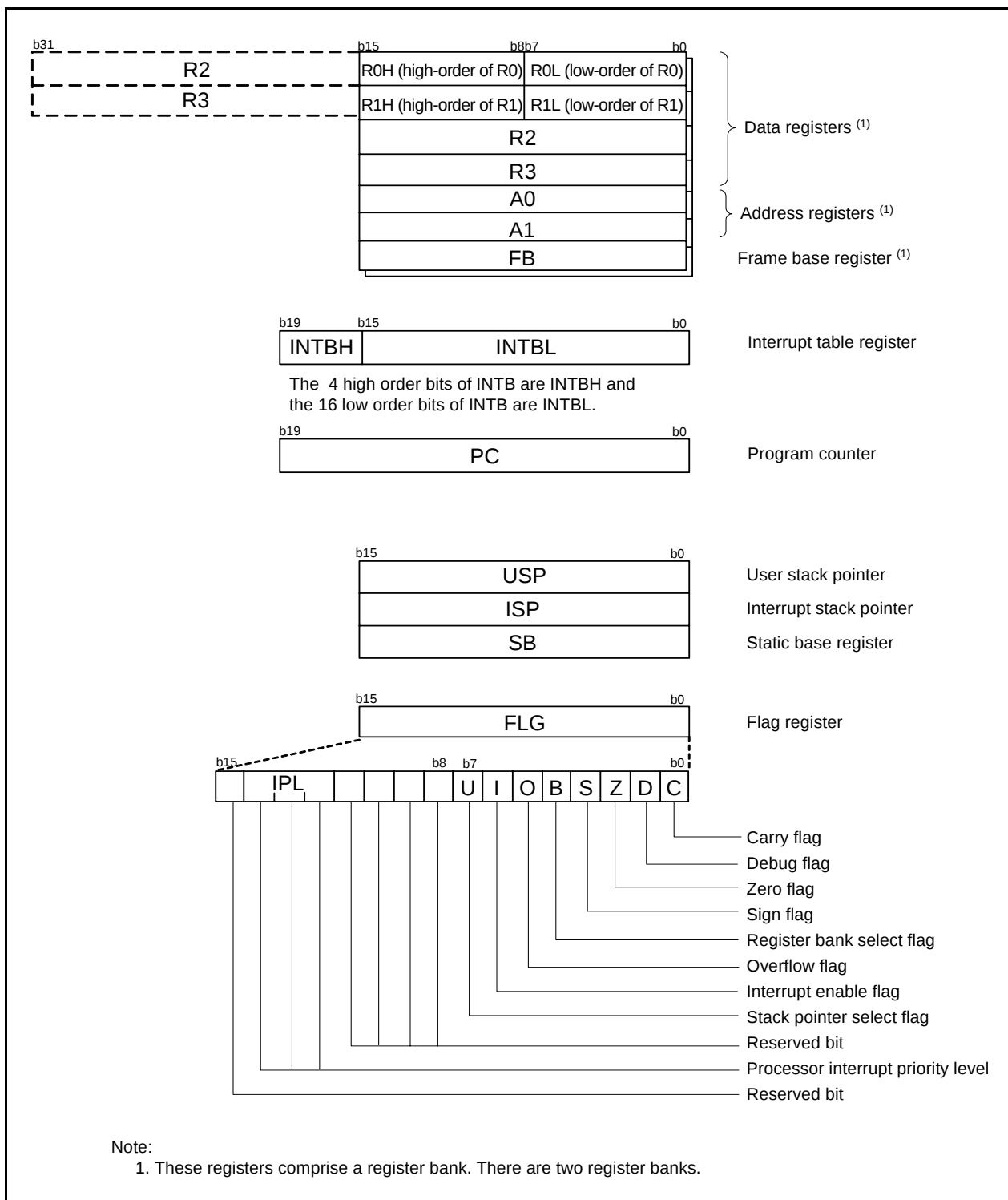


Figure 2.1 CPU Registers

2.1 Data Registers (R0, R1, R2, and R3)

R0 is a 16-bit register for transfer, arithmetic, and logic operations. The same applies to R1 to R3. R0 can be split into high-order bits (R0H) and low-order bits (R0L) to be used separately as 8-bit data registers. R1H and R1L are analogous to R0H and R0L. R2 can be combined with R0 and used as a 32-bit data register (R2R0). R3R1 is analogous to R2R0.

2.2 Address Registers (A0 and A1)

A0 is a 16-bit register for address register indirect addressing and address register relative addressing. It is also used for transfer, arithmetic, and logic operations. A1 is analogous to A0. A1 can be combined with A0 and as a 32-bit address register (A1A0).

2.3 Frame Base Register (FB)

FB is a 16-bit register for FB relative addressing.

2.4 Interrupt Table Register (INTB)

INTB is a 20-bit register that indicates the starting address of an interrupt vector table.

2.5 Program Counter (PC)

PC is 20 bits wide and indicates the address of the next instruction to be executed.

2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

The stack pointers (SP), USP and ISP, are each 16 bits wide. The U flag of FLG is used to switch between USP and ISP.

2.7 Static Base Register (SB)

SB is a 16-bit register for SB relative addressing.

2.8 Flag Register (FLG)

FLG is an 11-bit register indicating the CPU state.

2.8.1 Carry Flag (C)

The C flag retains carry, borrow, or shift-out bits that have been generated by the arithmetic and logic unit.

2.8.2 Debug Flag (D)

The D flag is for debugging only. Set it to 0.

2.8.3 Zero Flag (Z)

The Z flag is set to 1 when an arithmetic operation results in 0; otherwise to 0.

2.8.4 Sign Flag (S)

The S flag is set to 1 when an arithmetic operation results in a negative value; otherwise to 0.

2.8.5 Register Bank Select Flag (B)

Register bank 0 is selected when the B flag is 0. Register bank 1 is selected when this flag is set to 1.

2.8.6 Overflow Flag (O)

The O flag is set to 1 when an operation results in an overflow; otherwise to 0.

Table 4.6 SFR Information (6) ⁽¹⁾

Address	Register	Symbol	After Reset
0140h	Timer RD Control Register 0	TRDCR0	00h
0141h	Timer RD I/O Control Register A0	TRDIORA0	10001000b
0142h	Timer RD I/O Control Register C0	TRDIORC0	10001000b
0143h	Timer RD Status Register 0	TRDSR0	11100000b
0144h	Timer RD Interrupt Enable Register 0	TRDIER0	11100000b
0145h	Timer RD PWM Mode Output Level Control Register 0	TRDPOCR0	11111000b
0146h	Timer RD Counter 0	TRD0	00h
0147h			00h
0148h	Timer RD General Register A0	TRDGRA0	FFh
0149h			FFh
014Ah	Timer RD General Register B0	TRDGRB0	FFh
014Bh			FFh
014Ch	Timer RD General Register C0	TRDGRC0	FFh
014Dh			FFh
014Eh	Timer RD General Register D0	TRDGRD0	FFh
014Fh			FFh
0150h	Timer RD Control Register 1	TRDCR1	00h
0151h	Timer RD I/O Control Register A1	TRDIORA1	10001000b
0152h	Timer RD I/O Control Register C1	TRDIORC1	10001000b
0153h	Timer RD Status Register 1	TRDSR1	11000000b
0154h	Timer RD Interrupt Enable Register 1	TRDIER1	11100000b
0155h	Timer RD PWM Mode Output Level Control Register 1	TRDPOCR1	11111000b
0156h	Timer RD Counter 1	TRD1	00h
0157h			00h
0158h	Timer RD General Register A1	TRDGRA1	FFh
0159h			FFh
015Ah	Timer RD General Register B1	TRDGRB1	FFh
015Bh			FFh
015Ch	Timer RD General Register C1	TRDGRC1	FFh
015Dh			FFh
015Eh	Timer RD General Register D1	TRDGRD1	FFh
015Fh			FFh
0160h	UART1 Transmit/Receive Mode Register	U1MR	00h
0161h	UART1 Bit Rate Register	U1BRG	XXh
0162h	UART1 Transmit Buffer Register	U1TB	XXh
0163h			XXh
0164h	UART1 Transmit/Receive Control Register 0	U1C0	00001000b
0165h	UART1 Transmit/Receive Control Register 1	U1C1	00000010b
0166h	UART1 Receive Buffer Register	U1RB	XXh
0167h			XXh
0168h			
0169h			
016Ah			
016Bh			
016Ch			
016Dh			
016Eh			
016Fh			
0170h	Timer RG Mode Register	TRGMR	01000000b
0171h	Timer RG Count Control Register	TRGCNTC	00h
0172h	Timer RG Control Register	TRGCR	10000000b
0173h	Timer RG Interrupt Enable Register	TRGIER	11110000b
0174h	Timer RG Status Register	TRGSR	11100000b
0175h	Timer RG I/O Control Register	TRGIOR	00h
0176h	Timer RG Counter	TRG	00h
0177h			00h
0178h	Timer RG General Register A	TRGGRA	FFh
0179h			FFh
017Ah	Timer RG General Register B	TRGGRB	FFh
017Bh			FFh
017Ch	Timer RG General Register C	TRGGRC	FFh
017Dh			FFh
017Eh	Timer RG General Register D	TRGGRD	FFh
017Fh			FFh

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

Table 4.7 SFR Information (7) ⁽¹⁾

Address	Register	Symbol	After Reset
0180h	Timer RA Pin Select Register	TRASR	00h
0181h	Timer RB/RC Pin Select Register	TRBRCR	00h
0182h	Timer RC Pin Select Register 0	TRCPSR0	00h
0183h	Timer RC Pin Select Register 1	TRCPSR1	00h
0184h	Timer RD Pin Select Register 0	TRDPSR0	00h
0185h	Timer RD Pin Select Register 1	TRDPSR1	00h
0186h	Timer Pin Select Register	TIMSR	00h
0187h	Timer RF Output Control Register	TRFOUT	00h
0188h	UART0 Pin Select Register	U0SR	00h
0189h	UART1 Pin Select Register	U1SR	00h
018Ah	UART2 Pin Select Register 0	U2SR0	00h
018Bh	UART2 Pin Select Register 1	U2SR1	00h
018Ch	SSU/IIC Pin Select Register	SSUIICSR	00h
018Dh			
018Eh	INT Interrupt Input Pin Select Register	INTSR	00h
018Fh	I/O Function Pin Select Register	PINSR	00h
0190h			
0191h			
0192h			
0193h	SS Bit Counter Register	SSBR	11111000b
0194h	SS Transmit Data Register L / IIC bus Transmit Data Register ⁽²⁾	SSTDR / ICDRT	FFh
0195h	SS Transmit Data Register H ⁽²⁾	SSTDRH	FFh
0196h	SS Receive Data Register L / IIC bus Receive Data Register ⁽²⁾	SSRDR / ICDRR	FFh
0197h	SS Receive Data Register H ⁽²⁾	SSRDRH	FFh
0198h	SS Control Register H / IIC bus Control Register 1 ⁽²⁾	SSCRH / ICCR1	00h
0199h	SS Control Register L / IIC bus Control Register 2 ⁽²⁾	SSCRL / ICCR2	01111101b
019Ah	SS Mode Register / IIC bus Mode Register ⁽²⁾	SSMR / ICMR	00010000b / 00011000b
019Bh	SS Enable Register / IIC bus Interrupt Enable Register ⁽²⁾	SSER / ICIER	00h
019Ch	SS Status Register / IIC bus Status Register ⁽²⁾	SSSR / ICSR	00h / 0000X000b
019Dh	SS Mode Register 2 / Slave Address Register ⁽²⁾	SSMR2 / SAR	00h
019Eh			
019Fh			
01A0h			
01A1h			
01A2h			
01A3h			
01A4h			
01A5h			
01A6h			
01A7h			
01A8h			
01A9h			
01AAh			
01ABh			
01ACh			
01ADh			
01AEh			
01AFh			
01B0h			
01B1h			
01B2h	Flash Memory Status Register	FST	10000X00b
01B3h			
01B4h	Flash Memory Control Register 0	FMR0	00h
01B5h	Flash Memory Control Register 1	FMR1	00h
01B6h	Flash Memory Control Register 2	FMR2	00h
01B7h			
01B8h			
01B9h			
01BAh			
01BBh			
01BCh			
01BDh			
01BEh			
01BFh			

X: Undefined

Notes:

1. The blank areas are reserved and cannot be accessed by users.
2. Selectable by the IICSEL bit in the SSUIICSR register.

5. Electrical Characteristics

Table 5.1 Absolute Maximum Ratings

Symbol	Parameter	Condition	Rated Value	Unit
V _{CC} /AV _{CC}	Supply voltage		–0.3 to 6.5	V
V _I	Input voltage		–0.3 to V _{CC} + 0.3	V
V _O	Output voltage		–0.3 to V _{CC} + 0.3	V
P _d	Power dissipation	–40°C ≤ T _{opr} ≤ 85°C	500	mW
T _{opr}	Operating ambient temperature		–20 to 85 (N version)/ –40 to 85 (D version)	°C
T _{stg}	Storage temperature		–65 to 150	°C

Table 5.3 A/D Converter Characteristics

Symbol	Parameter		Conditions		Standard			Unit
					Min.	Typ.	Max.	
—	Resolution		V _{ref} = AV _{CC}		—	—	10	Bit
—	Absolute accuracy	10-bit mode	V _{ref} = AV _{CC} = 5.0 V	AN0 to AN7 input, AN8 to AN11 input, AN12 to AN19 input	—	—	±3	LSB
			V _{ref} = AV _{CC} = 3.3 V	AN0 to AN7 input, AN8 to AN11 input, AN12 to AN19 input	—	—	±5	LSB
			V _{ref} = AV _{CC} = 3.0 V	AN0 to AN7 input, AN8 to AN11 input, AN12 to AN19 input	—	—	±5	LSB
			V _{ref} = AV _{CC} = 2.2 V	AN0 to AN7 input, AN8 to AN11 input, AN12 to AN19 input	—	—	±5	LSB
		8-bit mode	V _{ref} = AV _{CC} = 5.0 V	AN0 to AN7 input, AN8 to AN11 input, AN12 to AN19 input	—	—	±2	LSB
			V _{ref} = AV _{CC} = 3.3 V	AN0 to AN7 input, AN8 to AN11 input, AN12 to AN19 input	—	—	±2	LSB
			V _{ref} = AV _{CC} = 3.0 V	AN0 to AN7 input, AN8 to AN11 input, AN12 to AN19 input	—	—	±2	LSB
			V _{ref} = AV _{CC} = 2.2 V	AN0 to AN7 input, AN8 to AN11 input, AN12 to AN19 input	—	—	±2	LSB
φAD	A/D conversion clock		4.0 V ≤ V _{ref} = AV _{CC} ≤ 5.5 V ⁽²⁾		2	—	20	MHz
			3.2 V ≤ V _{ref} = AV _{CC} ≤ 5.5 V ⁽²⁾		2	—	16	MHz
			2.7 V ≤ V _{ref} = AV _{CC} ≤ 5.5 V ⁽²⁾		2	—	10	MHz
			2.2 V ≤ V _{ref} = AV _{CC} ≤ 5.5 V ⁽²⁾		2	—	5	MHz
—	Tolerance level impedance				—	3	—	kΩ
tCONV	Conversion time	10-bit mode	V _{ref} = AV _{CC} = 5.0 V, φAD = 20 MHz		2.2	—	—	μs
		8-bit mode	V _{ref} = AV _{CC} = 5.0 V, φAD = 20 MHz		2.2	—	—	μs
tsAMP	Sampling time		φAD = 20 MHz		0.8	—	—	μs
Ivref	V _{ref} current		V _{CC} = 5.0 V, XIN = f1 = φAD = 20 MHz		—	45	—	μA
Vref	Reference voltage				2.2	—	AV _{CC}	V
VIA	Analog input voltage ⁽³⁾				0	—	V _{ref}	V
OCVREF	On-chip reference voltage		2 MHz ≤ φAD ≤ 4 MHz		1.19	1.34	1.49	V

Notes:

1. $V_{CC}/AV_{CC} = V_{ref} = 2.2$ to 5.5 V , $V_{SS} = 0\text{ V}$, and $T_{opr} = -20$ to 85°C (N version)/ -40 to 85°C (D version), unless otherwise specified.
2. The A/D conversion result will be undefined in wait mode, stop mode, when the flash memory stops, and in low-current-consumption mode. Do not perform A/D conversion in these states or transition to these states during A/D conversion.
3. When the analog input voltage is over the reference voltage, the A/D conversion result will be 3FFh in 10-bit mode and FFh in 8-bit mode.

Table 5.4 D/A Converter Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
—	Resolution		—	—	8	Bit
—	Absolute accuracy		—	—	2.5	LSB
t_{su}	Setup time		—	—	3	μs
R_o	Output resistor		—	6	—	$k\Omega$
I_{vref}	Reference power input current	(Note 2)	—	—	1.5	mA

Notes:

1. $V_{CC}/AV_{CC} = V_{ref} = 2.7$ to 5.5 V and $T_{opr} = -20$ to 85 °C (N version)/ -40 to 85 °C (D version), unless otherwise specified.
2. This applies when one D/A converter is used and the value of the DAI register ($i = 0$ or 1) for the unused D/A converter is 00h. The resistor ladder of the A/D converter is not included.

Table 5.5 Comparator B Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{ref}	IVREF1, IVREF3 input reference voltage		0	—	$V_{CC} - 1.4$	V
V_i	IVCMP1, IVCMP3 input voltage		-0.3	—	$V_{CC} + 0.3$	V
—	Offset		—	5	100	mV
t_d	Comparator output delay time ⁽²⁾	$V_i = V_{ref} \pm 100$ mV	—	0.1	—	μs
I_{CMP}	Comparator operating current	$V_{CC} = 5.0$ V	—	17.5	—	μA

Notes:

1. $V_{CC} = 2.7$ to 5.5 V and $T_{opr} = -20$ to 85 °C (N version)/ -40 to 85 °C (D version), unless otherwise specified.
2. When the digital filter is disabled.

Table 5.7 Flash Memory (Data flash Block A to Block D) Electrical Characteristics

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
—	Program/erase endurance ⁽²⁾		10,000 ⁽³⁾	—	—	times
—	Byte program time (program/erase endurance ≤ 1,000 times)		—	160	1500	μs
—	Byte program time (program/erase endurance > 1,000 times)		—	300	1500	μs
—	Block erase time (program/erase endurance ≤ 1,000 times)		—	0.2	1	s
—	Block erase time (program/erase endurance > 1,000 times)		—	0.3	1	s
t _d (SR-SUS)	Time delay from suspend request until suspend		—	—	5 + CPU clock × 3 cycles	ms
—	Interval from erase start/restart until following suspend request		0	—	—	μs
—	Time from suspend until erase restart		—	—	30 + CPU clock × 1 cycle	μs
t _d (CMDRST-READY)	Time from when command is forcibly stopped until reading is enabled		—	—	30 + CPU clock × 1 cycle	μs
—	Program, erase voltage		2.7	—	5.5	V
—	Read voltage		1.8	—	5.5	V
—	Program, erase temperature		−20 ⁽⁷⁾	—	85	°C
—	Data hold time ⁽⁸⁾	Ambient temperature = 55 °C	20	—	—	year

Notes:

1. V_{CC} = 2.7 to 5.5 V and T_{opr} = −20 to 85 °C (N version)/−40 to 85 °C (D version), unless otherwise specified.
2. Definition of programming/erasure endurance
The programming and erasure endurance is defined on a per-block basis.
If the programming and erasure endurance is n (n = 10,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to different addresses in block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one. However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
3. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed.)
4. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. In addition, averaging the erasure endurance between blocks A to D can further reduce the actual erasure endurance. It is also advisable to retain data on the erasure endurance of each block and limit the number of erase operations to a certain number.
5. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
6. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
7. −40 °C for D version.
8. The data hold time includes time that the power supply is off or the clock is not supplied.

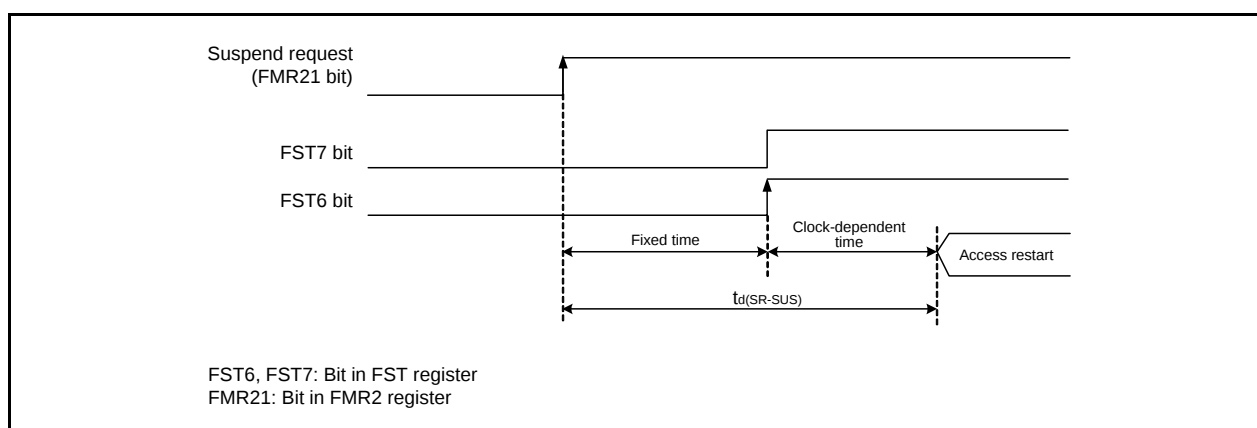
**Figure 5.2 Time delay until Suspend**

Table 5.8 Voltage Detection 0 Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
Vdet0	Voltage detection level Vdet0_0 ⁽²⁾		1.80	1.90	2.05	V
	Voltage detection level Vdet0_1 ⁽²⁾		2.15	2.35	2.50	V
	Voltage detection level Vdet0_2 ⁽²⁾		2.70	2.85	3.05	V
	Voltage detection level Vdet0_3 ⁽²⁾		3.55	3.80	4.05	V
—	Voltage detection 0 circuit response time ⁽⁴⁾	At the falling of Vcc from 5.0 V to (Vdet0_0 – 0.1) V	—	6	150	μs
—	Voltage detection circuit self power consumption	VCA25 = 1, Vcc = 5.0 V	—	1.5	—	μA
td(E-A)	Waiting time until voltage detection circuit operation starts ⁽³⁾		—	—	100	μs

Notes:

1. The measurement condition is Vcc = 1.8 to 5.5 V and T_{opr} = –20 to 85 °C (N version)/–40 to 85 °C (D version).
2. Select the voltage detection level with bits VDSEL0 and VDSEL1 in the OFS register.
3. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA25 bit in the VCA2 register to 0.
4. Time until the voltage monitor 0 reset is generated after the voltage passes Vdet0.

Table 5.9 Voltage Detection 1 Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
Vdet1	Voltage detection level Vdet1_0 ⁽²⁾	At the falling of Vcc	2.00	2.20	2.40	V
	Voltage detection level Vdet1_1 ⁽²⁾	At the falling of Vcc	2.15	2.35	2.55	V
	Voltage detection level Vdet1_2 ⁽²⁾	At the falling of Vcc	2.30	2.50	2.70	V
	Voltage detection level Vdet1_3 ⁽²⁾	At the falling of Vcc	2.45	2.65	2.85	V
	Voltage detection level Vdet1_4 ⁽²⁾	At the falling of Vcc	2.60	2.80	3.00	V
	Voltage detection level Vdet1_5 ⁽²⁾	At the falling of Vcc	2.75	2.95	3.15	V
	Voltage detection level Vdet1_6 ⁽²⁾	At the falling of Vcc	2.85	3.10	3.40	V
	Voltage detection level Vdet1_7 ⁽²⁾	At the falling of Vcc	3.00	3.25	3.55	V
	Voltage detection level Vdet1_8 ⁽²⁾	At the falling of Vcc	3.15	3.40	3.70	V
	Voltage detection level Vdet1_9 ⁽²⁾	At the falling of Vcc	3.30	3.55	3.85	V
	Voltage detection level Vdet1_A ⁽²⁾	At the falling of Vcc	3.45	3.70	4.00	V
	Voltage detection level Vdet1_B ⁽²⁾	At the falling of Vcc	3.60	3.85	4.15	V
	Voltage detection level Vdet1_C ⁽²⁾	At the falling of Vcc	3.75	4.00	4.30	V
	Voltage detection level Vdet1_D ⁽²⁾	At the falling of Vcc	3.90	4.15	4.45	V
	Voltage detection level Vdet1_E ⁽²⁾	At the falling of Vcc	4.05	4.30	4.60	V
	Voltage detection level Vdet1_F ⁽²⁾	At the falling of Vcc	4.20	4.45	4.75	V
—	Hysteresis width at the rising of Vcc in voltage detection 1 circuit	Vdet1_0 to Vdet1_5 selected	—	0.07	—	V
		Vdet1_6 to Vdet1_F selected	—	0.10	—	V
—	Voltage detection 1 circuit response time ⁽³⁾	At the falling of Vcc from 5.0 V to (Vdet1_0 – 0.1) V	—	60	150	μs
—	Voltage detection circuit self power consumption	VCA26 = 1, Vcc = 5.0 V	—	1.7	—	μA
td(E-A)	Waiting time until voltage detection circuit operation starts ⁽⁴⁾		—	—	100	μs

Notes:

1. The measurement condition is Vcc = 1.8 to 5.5 V and T_{opr} = –20 to 85 °C (N version)/–40 to 85 °C (D version).
2. Select the voltage detection level with bits VD1S0 to VD1S3 in the VD1LS register.
3. Time until the voltage monitor 1 interrupt request is generated after the voltage passes Vdet1.
4. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA26 bit in the VCA2 register to 0.

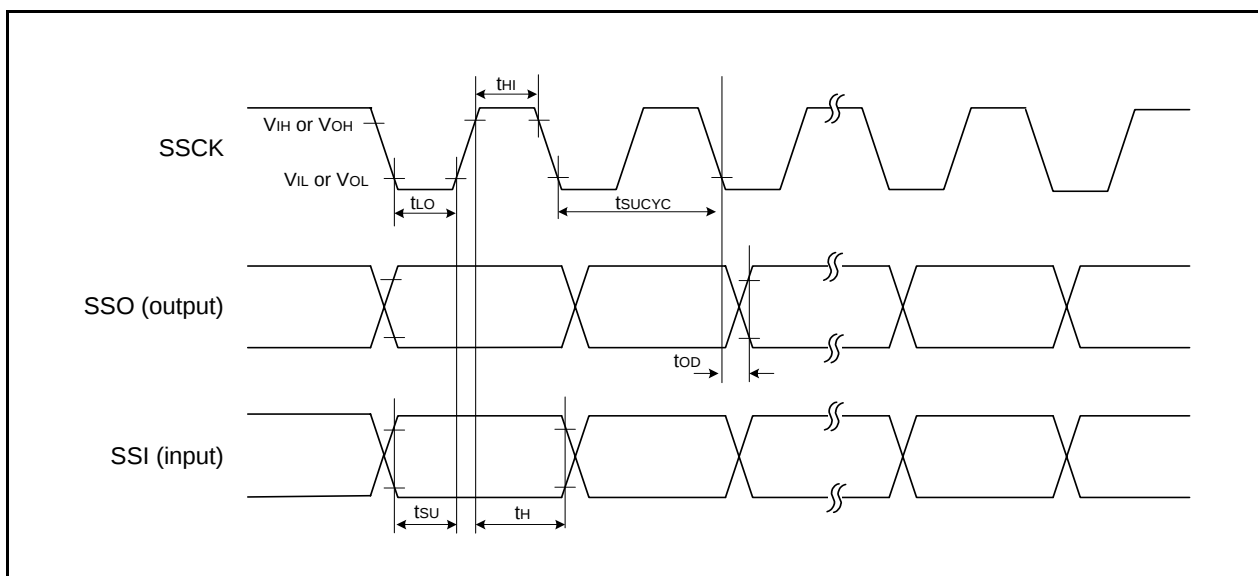


Figure 5.6 I/O Timing of Synchronous Serial Communication Unit (SSU) (Clock Synchronous Communication Mode)

Table 5.17 Electrical Characteristics (1) [4.2 V ≤ V_{CC} ≤ 5.5 V]

Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
V _{OH}	Output "H" voltage	Other than XOUT	Drive capacity High V _{CC} = 5 V	I _{OH} = -20 mA	V _{CC} - 2.0	—	V _{CC}	V
			Drive capacity Low V _{CC} = 5 V	I _{OH} = -5 mA	V _{CC} - 2.0	—	V _{CC}	V
		XOUT	V _{CC} = 5 V	I _{OH} = -200 μA	1.0	—	V _{CC}	V
V _{OL}	Output "L" voltage	Other than XOUT	Drive capacity High V _{CC} = 5 V	I _{OL} = 20 mA	—	—	2.0	V
			Drive capacity Low V _{CC} = 5 V	I _{OL} = 5 mA	—	—	2.0	V
		XOUT	V _{CC} = 5 V	I _{OL} = 200 μA	—	—	0.5	V
V _{T+} -V _{T-}	Hysteresis	INT0, INT1, INT2, INT3, INT4, KI0, KI1, KI2, KI3, TRAIO, TRBO, TRCIOA, TRCIOB, TRCIOC, TRCIOD, TRDIOA0, TRDIOB0, TRDIOC0, TRDIOD0, TRDIOA1, TRDIOB1, TRDIOC1, TRDIOD1, TRCTRG, TRCCLK, TRFI, TRGIOA, TRGIOB, ADTRG, RXD0, RXD1, RXD2, CLK0, CLK1, CLK2, SSI, SCL, SDA, SSO			0.1	1.2	—	V
		RESET			0.1	1.2	—	V
I _{IH}	Input "H" current		V _I = 5 V, V _{CC} = 5.0 V		—	—	5.0	μA
I _{IL}	Input "L" current		V _I = 0 V, V _{CC} = 5.0 V		—	—	-5.0	μA
R _{PULLUP}	Pull-up resistance		V _I = 0 V, V _{CC} = 5.0 V		25	50	100	kΩ
R _{FXIN}	Feedback resistance	XIN			—	0.3	—	MΩ
R _{FXCIN}	Feedback resistance	XCIN			—	8	—	MΩ
V _{RAM}	RAM hold voltage		During stop mode		1.8	—	—	V

Note:

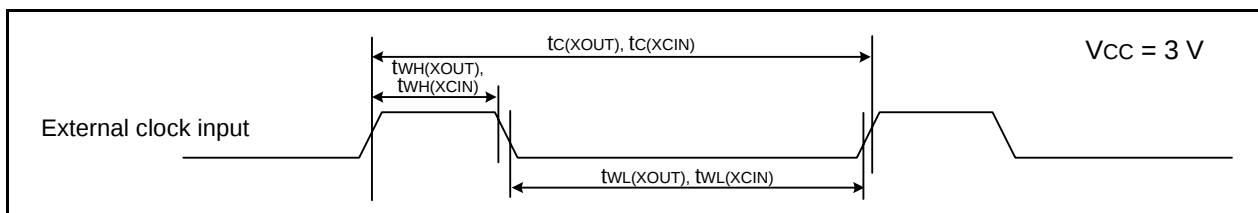
1. 4.2 V ≤ V_{CC} ≤ 5.5 V, T_{opr} = -20 to 85 °C (N version)/-40 to 85 °C (D version), and f(XIN) = 20 MHz, unless otherwise specified.

Table 5.18 Electrical Characteristics (2) [3.3 V ≤ V_{CC} ≤ 5.5 V]**(T_{opr} = −20 to 85 °C (N version)/−40 to 85 °C (D version), unless otherwise specified.)**

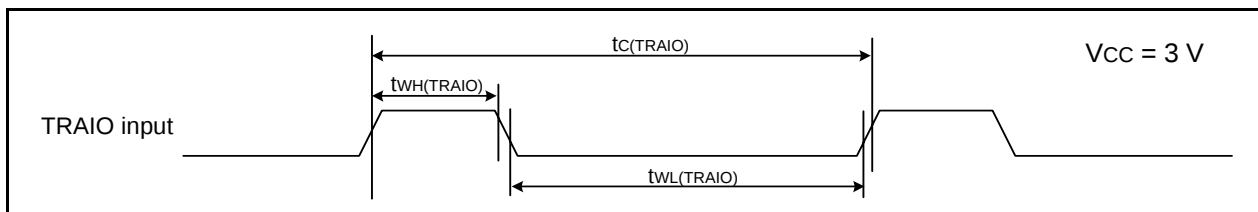
Symbol	Parameter	Condition	Standard			Unit	
			Min.	Typ.	Max.		
Icc	Power supply current (Vcc = 3.3 to 5.5 V) Single-chip mode, output pins are open, other pins are Vss	High-speed clock mode	XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	—	6.5	15	mA
			XIN = 16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	—	5.3	12.5	mA
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	—	3.6	—	mA
			XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	—	3.0	—	mA
			XIN = 16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	—	2.2	—	mA
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	—	1.5	—	mA
		High-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator on fOCO-F = 20 MHz Low-speed on-chip oscillator on = 125 kHz No division	—	7.0	15	mA
			XIN clock off High-speed on-chip oscillator on fOCO-F = 20 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	—	3.0	—	mA
			XIN clock off High-speed on-chip oscillator on fOCO-F = 4 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-16, MSTIIC = MSTTRD = MSTTRC = 1	—	1	—	mA
		Low-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR27 = 1, VCA20 = 0	—	90	400	μA
		Low-speed clock mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz No division FMR27 = 1, VCA20 = 0	—	85	400	μA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz No division Program operation on RAM Flash memory off, FMSTP = 1, VCA20 = 0	—	47	—	μA
		Wait mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = VCA25 = 0, VCA20 = 1	—	15	100	μA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = VCA25 = 0, VCA20 = 1	—	4	90	μA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (peripheral clock off) While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0, VCA20 = 1	—	3.5	—	μA
		Stop mode	XIN clock off, Topr = 25 °C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	—	2.0	5.0	μA
			XIN clock off, Topr = 85 °C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	—	15	—	μA

Timing requirements (Unless Otherwise Specified: $V_{CC} = 3\text{ V}$, $V_{SS} = 0\text{ V}$, $T_{opr} = 25\text{ }^{\circ}\text{C}$)**Table 5.26 External Clock Input (XOUT, XCIN)**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(XOUT)}$	XOUT input cycle time	50	—	ns
$t_{WH(XOUT)}$	XOUT input "H" width	24	—	ns
$t_{WL(XOUT)}$	XOUT input "L" width	24	—	ns
$t_{c(XCIN)}$	XCIN input cycle time	14	—	μs
$t_{WH(XCIN)}$	XCIN input "H" width	7	—	μs
$t_{WL(XCIN)}$	XCIN input "L" width	7	—	μs

**Figure 5.13 External Clock Input Timing Diagram when $V_{CC} = 3\text{ V}$** **Table 5.27 TRAIO Input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TRAIO)}$	TRAIO input cycle time	300	—	ns
$t_{WH(TRAIO)}$	TRAIO input "H" width	120	—	ns
$t_{WL(TRAIO)}$	TRAIO input "L" width	120	—	ns

**Figure 5.14 TRAIO Input Timing Diagram when $V_{CC} = 3\text{ V}$** **Table 5.28 TRFI Input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TRFI)}$	TRFI input cycle time	1200 (1)	—	ns
$t_{WH(TRFI)}$	TRFI input "H" width	600 (2)	—	ns
$t_{WL(TRFI)}$	TRFI input "L" width	600 (2)	—	ns

Notes:

1. When using timer RF input capture mode, adjust the cycle time to $(1/\text{timer RF count source frequency} \times 3)$ or above.
2. When using timer RF input capture mode, adjust the pulse width to $(1/\text{timer RF count source frequency} \times 1.5)$ or above.

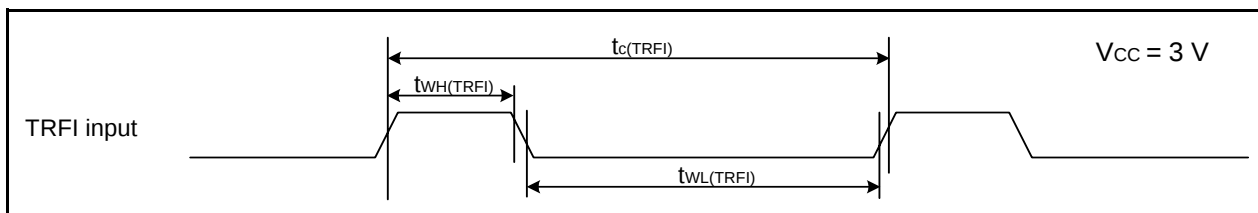
**Figure 5.15 TRFI Input Timing Diagram when $V_{CC} = 3\text{ V}$**

Table 5.31 Electrical Characteristics (5) [$1.8\text{ V} \leq V_{CC} < 2.7\text{ V}$]

Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
V _{OH}	Output "H" voltage	Other than XOUT	Drive capacity High	I _{OH} = -2 mA	V _{CC} - 0.5	—	V _{CC}	V
			Drive capacity Low	I _{OH} = -1 mA	V _{CC} - 0.5	—	V _{CC}	V
		XOUT		I _{OH} = -200 μ A	1.0	—	V _{CC}	V
V _{OL}	Output "L" voltage	Other than XOUT	Drive capacity High	I _{OL} = 2 mA	—	—	0.5	V
			Drive capacity Low	I _{OL} = 1 mA	—	—	0.5	V
		XOUT		I _{OL} = 200 μ A	—	—	0.5	V
V _{T+} -V _{T-}	Hysteresis	$\overline{\text{NT0}}$, $\overline{\text{INT1}}$, $\overline{\text{INT2}}$, $\overline{\text{INT3}}$, $\overline{\text{INT4}}$, $\overline{\text{KI0}}$, $\overline{\text{KI1}}$, $\overline{\text{KI2}}$, $\overline{\text{KI3}}$, $\overline{\text{TRAIO}}$, $\overline{\text{TRBO}}$, $\overline{\text{TRCIOA}}$, $\overline{\text{TRCIOB}}$, $\overline{\text{TRCI0C}}$, $\overline{\text{TRCI0D}}$, $\overline{\text{TRDIOA0}}$, $\overline{\text{TRDIOB0}}$, $\overline{\text{TRDIO0C}}$, $\overline{\text{TRDIO0D}}$, $\overline{\text{TRDIOA1}}$, $\overline{\text{TRDIOB1}}$, $\overline{\text{TRDIO0C1}}$, $\overline{\text{TRDIO0D1}}$, $\overline{\text{TRCTRG}}$, $\overline{\text{TRCCLK}}$, $\overline{\text{TRFI}}$, $\overline{\text{TRGIOA}}$, $\overline{\text{TRGIOB}}$, $\overline{\text{ADTRG}}$, $\overline{\text{RXD0}}$, $\overline{\text{RXD1}}$, $\overline{\text{RXD2}}$, $\overline{\text{CLK0}}$, $\overline{\text{CLK1}}$, $\overline{\text{CLK2}}$, $\overline{\text{SSI}}$, $\overline{\text{SCL}}$, $\overline{\text{SDA}}$, $\overline{\text{SSO}}$			0.05	0.20	—	V
		$\overline{\text{RESET}}$			0.05	0.20	—	V
I _{IH}	Input "H" current		V _I = 2.2 V, V _{CC} = 2.2 V		—	—	4.0	μ A
I _{IL}	Input "L" current		V _I = 0 V, V _{CC} = 2.2 V		—	—	-4.0	μ A
R _{PULLUP}	Pull-up resistance		V _I = 0 V, V _{CC} = 2.2 V		70	140	300	k Ω
R _{FXIN}	Feedback resistance	XIN			—	0.3	—	M Ω
R _{FXCIN}	Feedback resistance	XCIN			—	8	—	M Ω
V _{RAM}	RAM hold voltage		During stop mode		1.8	—	—	V

Note:

1. $1.8\text{ V} \leq V_{CC} < 2.7\text{ V}$, T_{opr} = -20 to 85 °C (N version)/-40 to 85 °C (D version), and f(XIN) = 5 MHz, unless otherwise specified.

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

- The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

The state of the product is undefined at the moment when power is supplied.

- The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

Access to reserved addresses is prohibited.

- The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

- When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

- The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.