## 3.7 General-purpose inputs/outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions.

The I/O configuration can be locked if needed following a specific sequence in order to avoid spurious writing to the I/Os registers.

## 3.8 Direct memory access controller (DMA)

The 5-channel general-purpose DMAs manage memory-to-memory, peripheral-to-memory

# 2 Description

The STM32F050xx family incorporates the high-performance ARM Cortex™-M0 32-bit RISC core operating at a 48 MHz maximum frequency, high-speed embedded memories (Flash memory up to 32 Kbytes and SRAM up to 4 Kbytes), and an extensive range of enhanced peripherals and I/Os. All devices offer standard communication interfaces (one $I^2C$, one SPI, one I2S, and one USART), one 12-bit ADC, up to five general-purpose 16-bit timers, a 32-bit timer and an advanced-control PWM timer.

The STM32F050xx family operates in the -40 to +85 °C and -40 to +105 °C temperature ranges, from a 2.0 to 3.6 V power supply. A comprehensive set of power-saving modes allows the design of low-power applications.

The STM32F050xx family includes devices in five different packages ranging from 20 pins to 48 pins. Depending on the device chosen, different sets of peripherals are included. An overview of the complete range of peripherals proposed in this family is provided.

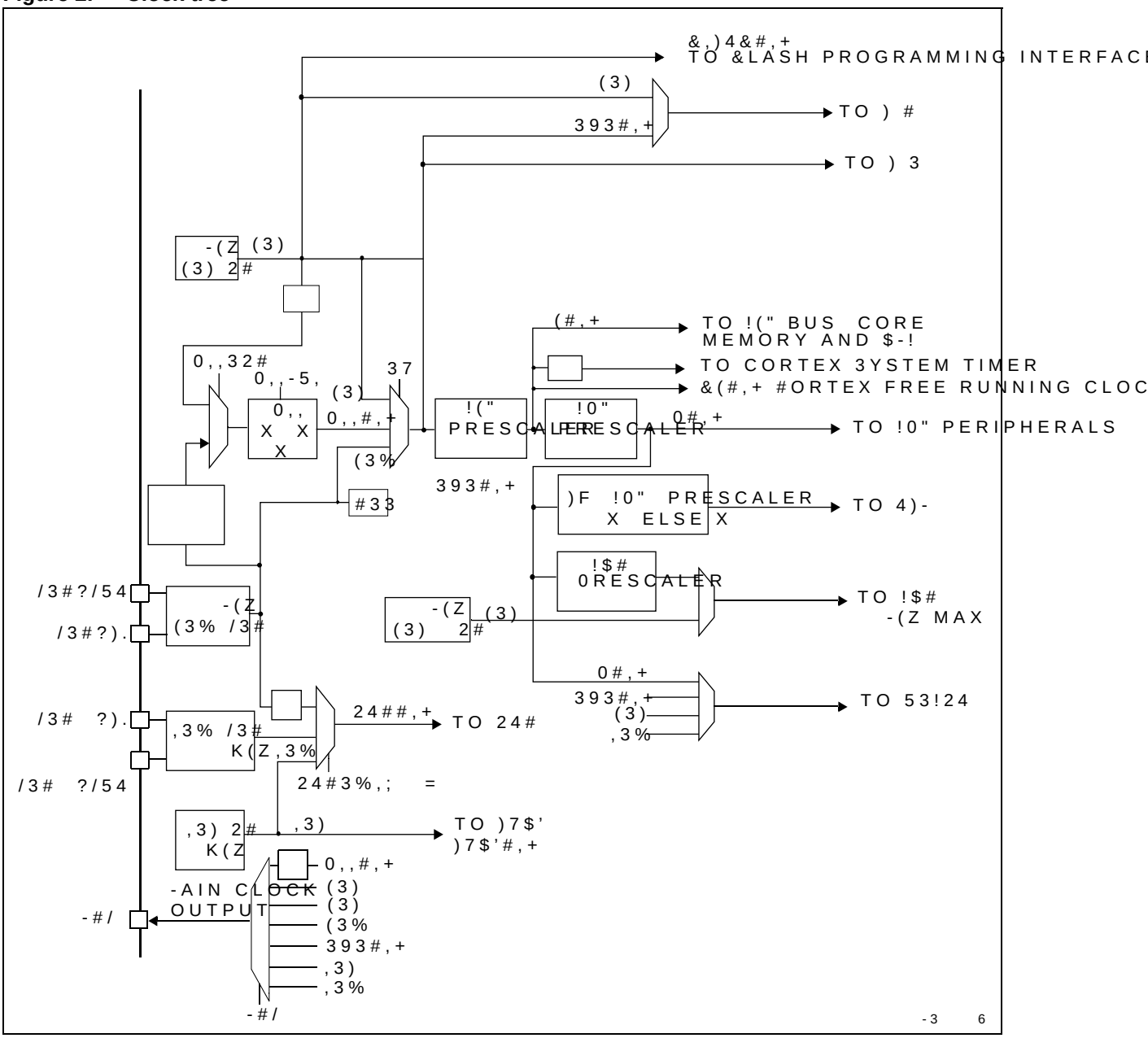
These features make the STM32F050xx microcontroller family suitable for a wide range of applications such as control application and user interfaces, handheld equipment, A/V receivers and digital TV, PC peripherals, gaming and GPS platforms, industrial applications, PLCs, inverters, printers, scanners, alarm systems, video intercoms, and HVACs.

## 3.6 Clocks and startup

System clock selection is performed on startup, however the internal RC 8 MHz oscillator is selected as default CPU clock on reset. An external 4-32 MHz clock can be selected, in which case it is monitored for failure. If failure is detected, the system automatically switches back to the internal RC oscillator. A software interrupt is generated if enabled. Similarly, full interrupt management of the PLL clock entry is available when necessary (for example on failure of an indirectly used external crystal, resonator or oscillator).

Several prescalers allow the application to configure the frequency of the AHB and the APB domains. The maximum frequency of the AHB and the APB domains is 48 MHz.

**Figure 2. Clock tree**



#### TIM2, TIM3

STM32F050xx devices feature two synchronizable 4-channel general-purpose timers. TIM2 is based on a 32-bit auto-reload up/downcounter and a 16-bit prescaler. TIM3 is based on a 16-bit auto-reload up/downcounter and a 16-bit prescaler. They feature 4 independent channels each for input capture/output compare, PWM or one-pulse mode output. This gives up to 12 input captures/output compares/PWMs on the largest packages.

The TIM2 and TIM3 general-purpose timers can work together or with the TIM1 advanced-control timer via the Timer Link feature for synchronization or event chaining.

TIM2 and TIM3 both have independent DMA request generation.

These timers are capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 3 hall-effect sensors.

Their counters can be frozen in debug mode.

#### TIM14

This timer is based on a 16-bit auto-reload upcounter and a 16-bit prescaler.

TIM14 features one single channel for input capture/output compare, PWM or one-pulse mode output.

Its counter can be frozen in debug mode.

#### TIM16 and TIM17

These timers are based on a 16-bit auto-reload upcounter and a 16-bit prescaler.

TIM16 and TIM17 feature one single channel for input capture/output compare, PWM or one-pulse mode output.

TIM16, and TIM17 have a complementary output with dead-time generation and independent DMA request generation

Their counters can be frozen in debug mode.

### 3.11.3 Independent watchdog (IWDG)

The independent watchdog is based on an 8-bit prescaler and 12-bit downcounter with user-defined refresh window. It is clocked from an independent 40 kHz internal RC and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free running timer for application timeout management. It is hardware or software configurable through the option bytes. The counter can be frozen in debug mode.

### 3.11.4 System window watchdog (WWDG)

The system window watchdog is based on a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the APB clock (PCLK). It has an early warning interrupt capability and the counter can be frozen in debug mode.

# 4 Pinouts and pin description

**Figure 3. LQFP48 48-pin package pinout**

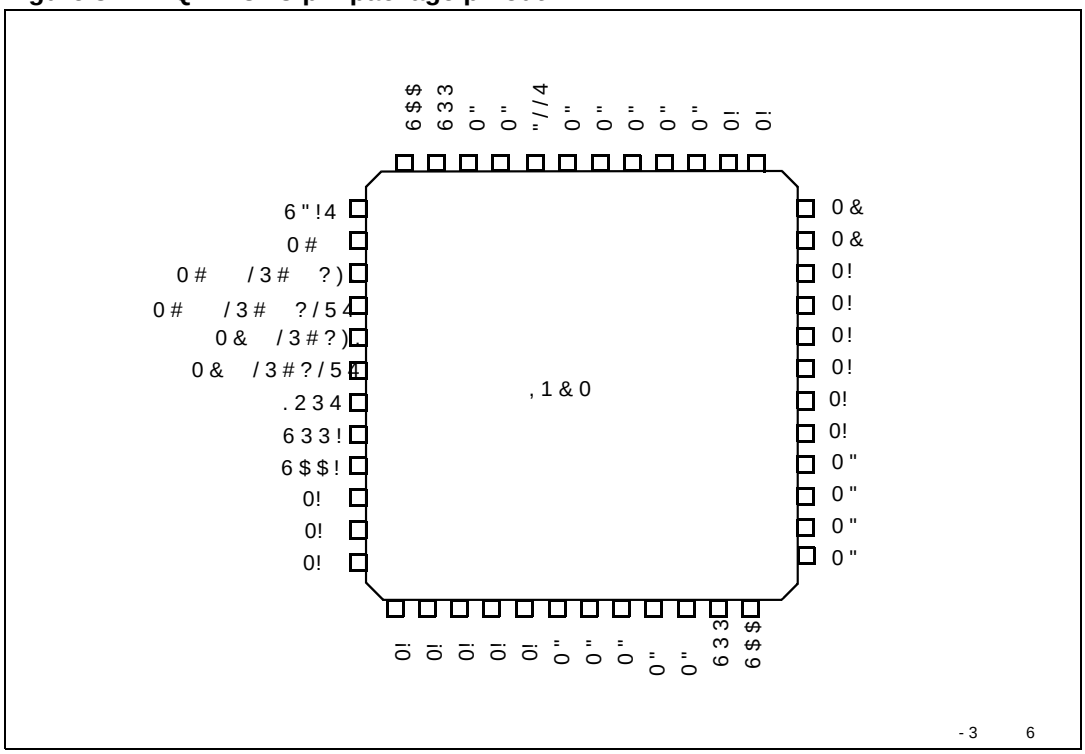
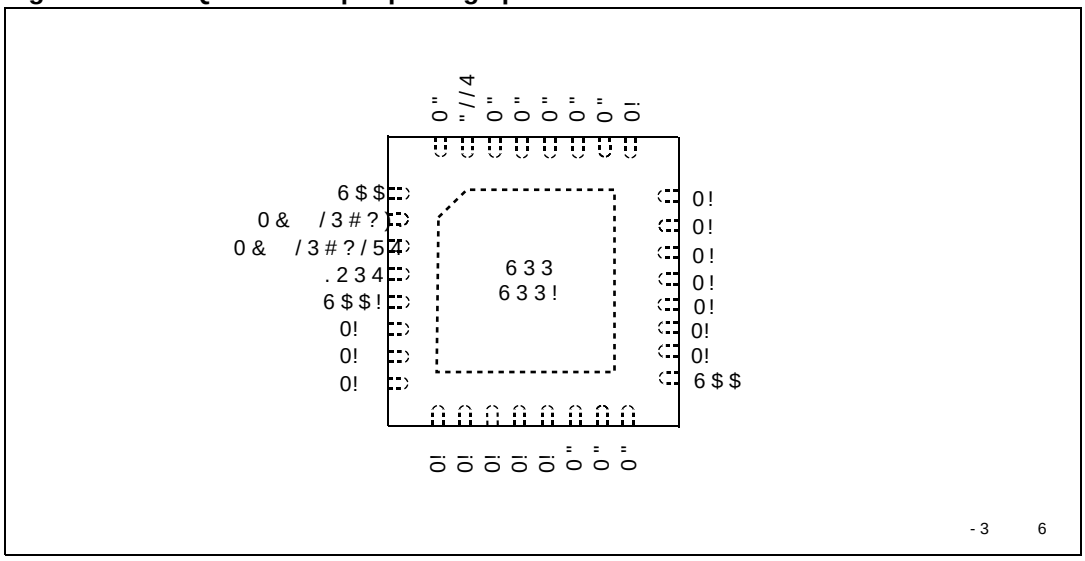



**Figure 4. UFQFPN32 32-pin package pinout**



## 6.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in Table 12: Voltage characteristics, Table 13: Current characteristics, and Table 14: Thermal characteristics may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

**Table 12. Voltage characteristics(1)**

| Symbol | Ratings | Min | Max | Unit |
|---|---|---|---|---|
| $V_{DD}$–$V_{DDA}$ | Allowed voltage difference for $V_{DD} > V_{DDA}$ | - | 0.4 | V |
| $V_{IN}$(2) | Input voltage on FT and FTf pins | $V_{SS}$ –0.3 | $V_{DD}$ + 4.0 | V |
| | Input voltage on TTa pins | $V_{SS}$ –0.3 | 4.0 | V |
| | Input voltage on any other pin | $V_{SS}$ –0.3 | 4.0 | V |
| $\lvert\Delta V_{DDx}\rvert$ | Variations between different $V_{DD}$ power pins | - | 50 | mV |
| $\lvert V_{SSX} - V_{SS}\rvert$ | Variations between all the different ground pins | - | 50 | mV |
| $V_{ESD(HBM)}$ | Electrostatic discharge voltage (human body model) | see Section 6.3.11: Electrical sensitivity characteristics | | |

1. All main power ($V_{DD}$, $V_{DDA}$) and ground ($V_{SS}$, $V_{SSA}$) pins must always be connected to the external power supply, in the permitted range.
2. $V_{IN}$ maximum must always be respected. Refer to Table 13: Current characteristics for the maximum allowed injected current values.

**Table 13. Current characteristics**

| Symbol | Ratings | Max. | Unit |
|---|---|---|---|
| $I_{VDD(\Sigma)}$ | Total current into sum of all VDD_x and VDDSDx power lines (source)(1) | 120 | |
| $I_{VSS(\Sigma)}$ | Total current out of sum of all VSS_x and VSSSD ground lines (sink)(1) | -120 | |
| $I_{VDD(PIN)}$ | Maximum current into each VDD_x or VDDSDx power pin (source)(1) | 100 | |
| $I_{VSS(PIN)}$ | Maximum current out of each VSS_x or VSSSD gou356 30Tm -.002IN | Tc-.002IN6.7( | |
| | | | mA |

2. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins referring to high pin count QFP packages.
3. Positive injection is not possible on these I/Os and does not occur for input voltages lower than the specified maximum value.
4. A positive injection is induced by $V_{IN}>V_{DD}$ while a negative injection is induced by $V_{IN}<V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to Table 12: Voltage characteristics for the maximum allowed input voltage values.
5. A positive injection is induced by $V_{IN}>V_{DDA}$ while a negative injection is induced by $V_{IN}<V_{SS}$. $I_{INJ}$(PIN) must never be exceeded. Refer also to Table 12: Voltage characteristics for the maximum allowed input voltage values. Negative injection disturbs the analog performance of the device. See note (2) below Table 51: ADC accuracy.
6. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

**Table 14. Thermal characteristics**

| Symbol | Ratings | Value | Unit |
|---|---|---|---|
| $T_{STG}$ | Storage temperature range | –65 to +150 | °C |
| $T_J$ | Maximum junction temperature | 150 | °C |

**Table 18. Programmable voltage detector characteristics (continued)**

| Symbol | Parameter | Conditions | Min(1) | Typ | Max(1) | Unit |
|---|---|---|---|---|---|---|
| $V_{PVD5}$ | PVD threshold 5 | Rising edge | 2.57 | 2.68 | 2.79 | V |
| | | Falling edge | 2.47 | 2.58 | 2.69 | V |
| $V_{PVD6}$ | PVD threshold 6 | Rising edge | 2.66 | 2.78 | 2.9 | V |
| | | Falling edge | 2.56 | 2.68 | 2.8 | V |
| $V_{PVD7}$ | PVD threshold 7 | Rising edge | 2.76 | 2.88 | 3 | V |
| | | Falling edge | 2.66 | 2.78 | 2.9 | V |
| $V_{PVDhyst}$(2) | PVD hysteresis | | - | 100 | - | mV |
| $I_{DD(PVD)}$ | PVD current consumption | | - | 0.15 | 0.26 | µA |

1. Data based on characterization results only, not tested in production.
2. Guaranteed by design, not tested in production.

## 6.3.4 Embedded reference voltage

The parameters given in Table 19 are derived from tests performed under ambient temperature and $V_{DD}$ supply voltage conditions summarized in Table 15: General operating conditions.

**Table 19. Embedded internal reference voltage**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{REFINT}$ | Internal reference voltage | –40 °C < $T_A$ < +105 °C | 1.16 | 1.2 | 1.25 | V |
| | | –40 °C < $T_A$ < +85 °C | 1.16 | 1.2 | 1.24(1) | V |
| $T_{S\_vrefint}$ (2) | ADC sampling time when reading the internal reference voltage | | - | 5.1 | 17.1(3) | µs |
| $\Delta V_{REFINT}$ | Internal reference voltage spread over the temperature range | $V_{DDA}$ = 3 V ±10 mV | - | - | 10(3) | mV |
| $T_{Coeff}$ | Temperature coeffi f 72ge- | | | | | |

1. Data based on characterization results, not tested in production.
2. Shortest sampling time can be determined in the application by multiple iterations.
3. Guaranteed by design, not tested in production.

**Table 26. Typical current consumption in Sleep mode, code running from Flash or RAM**

| Symbol | Parameter | Conditions | $f_{HCLK}$ | Typ | | Unit |
|---|---|---|---|---|---|---|
| | | | | Peripherals enabled | Peripherals disabled | |
| $I_{DD}$ | Supply current in Sleep mode from $V_{DD}$ supply | Running from HSE crystal clock 8 MHz, code executing from Flash or RAM | 48 MHz | 10.7 | 2.4 | mA |
| | | | 36 MHz | 8.1 | 1.8 | |
| | | | 32 MHz | 7.1 | 1.6 | |
| | | | 24 MHz | 5.5 | 1.3 | |
| | | | 16 MHz | 3.7 | 0.9 | |
| | | | 8 MHz | 1.9 | 0.5 | |
| | | | 4 MHz | 1.5 | 0.4 | |
| | | | 2 MHz | 1.1 | 0.3 | |
| | | | 1 MHz | 0.8 | 0.3 | |
| | | | 500 kHz | 0.6 | 0.3 | |
| | | | 125 kHz | 0.5 | 0.3 | |
| $I_{DDA}$ | Supply current in Sleep mode from $V_{DDA}$ supply | | 48 MHz | 140 | 140 | µA |
| | | | 36 MHz | 109 | 109 | |
| | | | 32 MHz | 96 | 96 | |
| | | | 24 MHz | 76 | 76 | |
| | | | 16 MHz | 51 | 51 | |
| | | | 8 MHz | 1.7 | 1.7 | |
| | | | 4 MHz | 1.6 | 1.6 | |
| | | | 2 MHz | 1.5 | 1.5 | |
| | | | 1 MHz | 1.1 | 1.1 | |
| | | | 500 kHz | 1.1 | 1.1 | |
| | | | 125 kHz | 1.1 | 1.1 | |

### Low-speed external user clock generated from an external source

In bypass mode the LSE oscillator is switched off and the input pin is a standard GPIO.

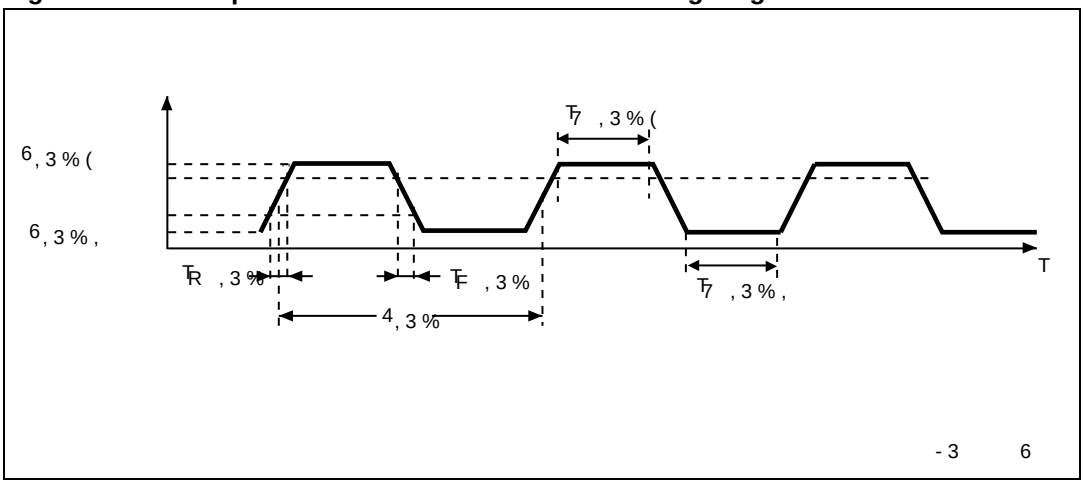
The external clock signal has to respect the I/O characteristics in Section 6.3.13. However, the recommended clock input waveform is shown in Figure 13.

**Table 30. Low-speed external user clock characteristics**

| Symbol | Parameter(1) | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{LSE\_ext}$ | User External clock source frequency | | - | 32.768 | 1000 | kHz |
| $V_{LSEH}$ | OSC32_IN input pin high level voltage | | $0.7V_{DD}$ | - | $V_{DD}$ | V |
| $V_{LSEL}$ | OSC32_IN input pin low level voltage | | $V_{SS}$ | - | $0.3V_{DD}$ | |
| $t_{w(LSEH)}$ $t_{w(LSEL)}$ | OSC32_IN high or low time | | 450 | - | - | ns |
| $t_{r(LSE)}$ $t_{f(LSE)}$ | OSC32_IN rise or fall time | | - | - | 50 | |

1. Guaranteed by design, not tested in production.

**Figure 13. Low-speed external clock source AC timing diagram**



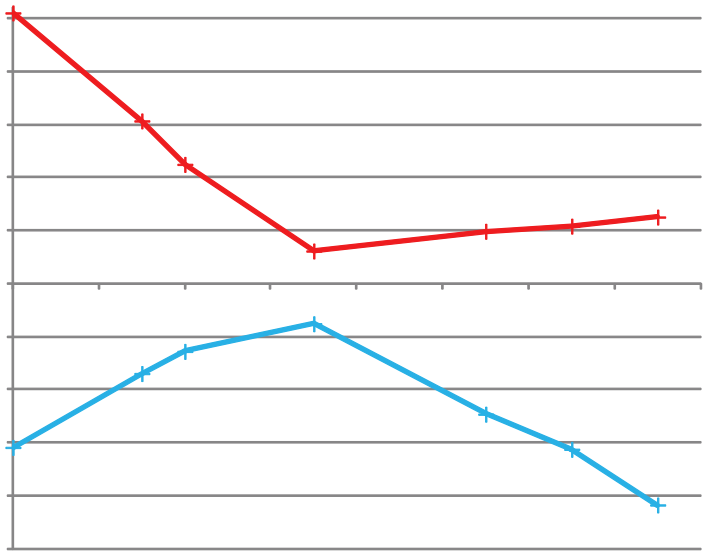
## High-speed internal 14 MHz (HSI14) RC oscillator (dedicated to ADC)

**Table 34. HSI14 oscillator characteristics(1)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{HSI14}$ | Frequency | | - | 14 | | MHz |
| TRIM | HSI14 user-trimming step | | - | - | 1(2) | % |
| $DuCy_{(HSI14)}$ | Duty cycle | | 45(2) | - | 55(2) | % |
| $ACC_{HSI14}$ | Accuracy of the HSI14 oscillator (factory calibrated) | $T_A$ = –40 to 105 °C | –4.2(3) | - | 5.1(3) | % |
| | | $T_A$ = –10 to 85 °C | –3.2(3) | - | 3.1(3) | % |
| | | $T_A$ = 0 to 70 °C | –2.5(3) | - | 2.3(3) | % |
| | | $T_A$ = 25 °C | –1 | - | 1 | % |
| $t_{su(HSI14)}$ | HSI14 oscillator startup time | | 1(2) | - | 2(2) | µs |
| $I_{DDA(HSI14)}$ | HSI14 oscillator power consumption | | - | 100 | 150(2) | µA |

1. $V_{DDA}$ = 3.3 V, $T_A$ = –40 to 105 °C unless otherwise specified.
2. Guaranteed by design, not tested in production.
3. Data based on characterization results, not tested in production.

**Figure 17. HSI14 oscillator accuracy characterization results**



- 3 6

### 6.3.15 12-bit ADC characteristics

Unless otherwise specified, the parameters given in Table 49 are preliminary values derived from tests performed under ambient temperature, $f_{PCLK2}$ frequency and $V_{DDA}$ supply voltage conditions summarized in Table 15: General operating conditions.

Note: It is recommended to perform a calibration after each power-up.

**Table 49. ADC characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DDA}$ | Analog supply voltage for ADC ON | | 2.4 | - | 3.6 | V |
| $f_{ADC}$ | ADC clock frequency | | 0.6 | - | 14 | MHz |
| $f_S$(1) | Sampling rate | | 0.05 | - | 1 | MHz |
| $f_{TRIG}$(1) | External trigger frequency | $f_{ADC}$ = 14 MHz | - | - | 823 | kHz |
| | | | - | - | 17 | $1/f_{ADC}$ |
| $V_{AIN}$ | Conversion voltage range | | 0 | - | $V_{DDA}$ | V |
| $R_{AIN}$(1) | External input impedance | See Equation 1 and Table 50 for details | - | - | 50 | kΩ |
| $R_{ADC}$(1) | Sampling switch resistance | | - | - | 1 | kΩ |
| $C_{ADC}$(1) | Internal sample and hold capacitor | | - | - | 8 | pF |
| $t_{CAL}$(1) | Calibration time | $f_{ADC}$ = 14 MHz | 5.9 | | | µs |
| | | | 83 | | | $1/f_{ADC}$ |
| $t_{latr}$(1) | Trigger conversion latency | $f_{ADC} = f_{PCLK}/2$ = 14 MHz | 0.196 | | | µs |
| | | $f_{ADC} = f_{PCLK}/2$ | 5.5 | | | $1/f_{PCLK}$ |
| | | $f_{ADC} = f_{PCLK}/4$ = 12 MHz | 0.219 | | | µs |
| | | $f_{ADC} = f_{PCLK}/4$ | 10.5 | | | $1/f_{PCLK}$ |
| | | $f_{ADC} = f_{HSI14}$ = 14 MHz | 0.188 | - | 0.259 | µs |
| $Jitter_{ADC}$ | ADC jitter on trigger conversion | $f_{ADC} = f_{HSI14}$ | - | 1 | - | $1/f_{HSI14}$ |
| $t_S$(1) | Sampling time | $f_{ADC}$ = 14 MHz | 0.107 | - | 17.1 | µs |
| | | | 1.5 | - | 239.5 | $1/f_{ADC}$ |
| $t_{STAB}$(1) | Power-up time | | 0 | 0 | 1 | µs |
| $t_{CONV}$(1) | Total conversion time (including sampling time) | $f_{ADC}$ = 14 MHz | 1 | | 18 | µs |
| | | | 14 to 252 ($t_S$ for sampling +12.5 for successive approximation) | | | $1/f_{ADC}$ |

1. Guaranteed by design, not tested in production.

2. ADC Accuracy vs. Negative Injection Current: Injecting negative current on any of the standard (non-robust) analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to standard analog pins which may potentially inject negative current.
Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in Section 6.3.13 does not affect the ADC accuracy.
3. Better performance may be achieved in restricted $V_{DDA}$, frequency and temperature ranges.
4. Data based on characterization results, not tested in production.

**Figure 24. ADC accuracy characteristics**

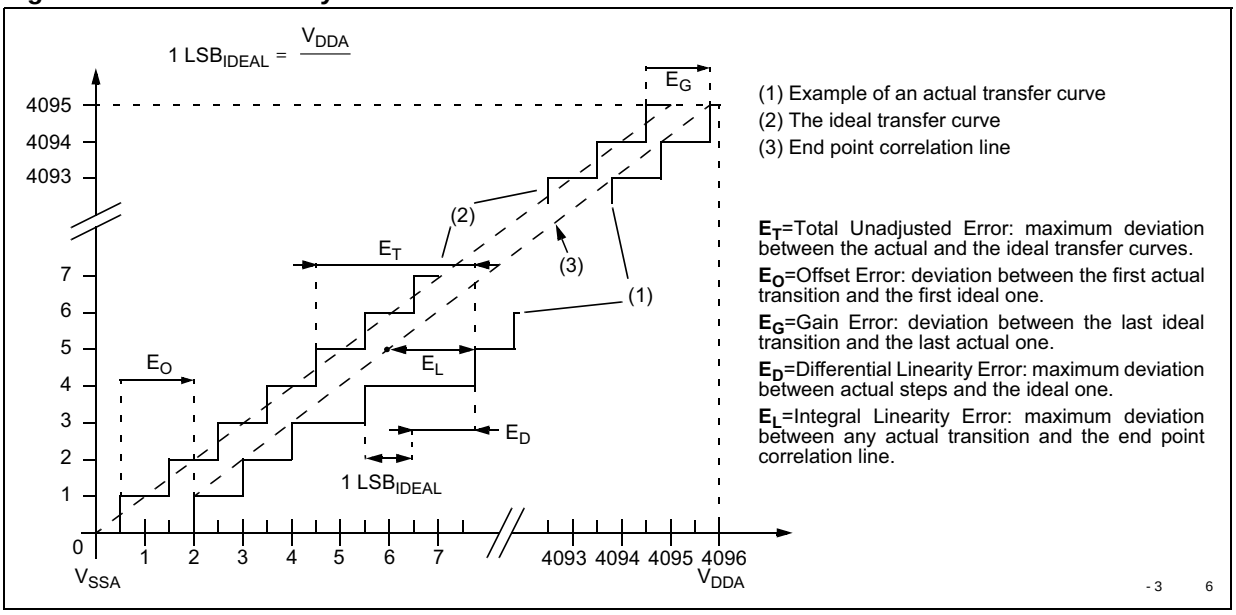
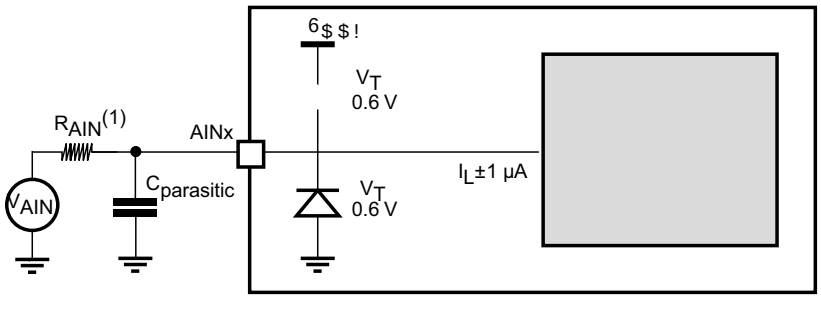



**Figure 25. Typical connection diagram using the ADC**




1. Refer to Table 49: ADC characteristics for the values of $R_{AIN}$, $R_{ADC}$ and $C_{ADC}$.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7 pF). A high $C_{parasitic}$ value will downgrade conversion accuracy. To remedy this, $f_{ADC}$ should be reduced.

## General PCB design guidelines

Power supply decoupling should be performed as shown in Figure 10. The 10 nF capacitor should be ceramic (good quality) and it should be placed as close as possible to the chip.

### 6.3.16 Temperature sensor characteristics

**Table 52. TS characteristics**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $T_L$(1) | $V_{SENSE}$ linearity with temperature | - | ±1 | ±2 | °C |
| Avg_Slope(1) | Average slope | 4.0 | 4.3 | 4.6 | mV/°C |
| $V_{25}$ | Voltage at 25 °C | 1.34 | 1.43 | 1.52 | V |
| $t_{START}$(1) | Startup time | 4 | - | 10 | µs |
| $T_{S\_temp}$(1)(2) | ADC sampling time when reading the temperature | 17.1 | - | - | µs |

1. Guaranteed by design, not tested in production.
2. Shortest sampling time can be determined in the application by multiple iterations.

### 6.3.17 $V_{BAT}$ monitoring characteristics

**Table 53. $V_{BAT}$ monitoring characteristics**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| R | Resistor bridge for $V_{BAT}$ | - | 50 | - | KΩ |
| Q | Ratio on $V_{BAT}$ measurement | - | 2 | - | |
| Er(1) | Error on Q | –1 | - | +1 | % |
| $T_{S\_vbat}$(1)(2) | ADC sampling time when reading the $V_{BAT}$ 1mV accuracy | 5 | - | - | µs |

1. Guaranteed by design, not tested in production.
2. Shortest sampling time can be determined in the application by multiple iterations.

### 6.3.18 Timer characteristics

The parameters given in Table 54 are guaranteed by design.

Refer to Section 6.3.13: I/O port characteristics for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

**Table 54. TIMx(1) characteristics**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $t_{res(TIM)}$ | Timer resolution time | | 1 | - | $t_{TIMxCLK}$ |
| | | $f_{TIMxCLK}$ = 48 MHz | 20.8 | - | ns |
| $f_{EXT}$ | Timer external clock frequency on CH1 to CH4 | | 0 | $f_{TIMxCLK}/2$ | MHz |
| | | $f_{TIMxCLK}$ = 48 MHz | 0 | 24 | MHz |
| $Res_{TIM}$ | Timer resolution | TIMx (except TIM2) | - | 16 | bit |
| | | TIM2 | - | 32 | |

**Table 59. SPI characteristics**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $f_{SCK}$<br>$1/t_{c(SCK)}$ | SPI clock frequency | Master mode | - | 18 | MHz |
| | | Slave mode | - | 18 | |
| $t_{r(SCK)}$<br>$t_{f(SCK)}$ | SPI clock rise and fall time | Capacitive load: C = 15 pF | - | 6 | ns |
| $t_{su(NSS)}$ (1) | NSS setup time | Slave mode | 4Tpclk | - | ns |
| $t_{h(NSS)}$ (1) | NSS hold time | Slave mode | 2Tpclk + 10 | - | |
| $t_{w(SCKH)}$ (1)<br>$t_{w(SCKL)}$ (1) | SCK high and low time | Master mode, $f_{PCLK}$ = 36 MHz, presc = 4 | Tpclk/2 -2 | Tpclk/2 + 1 | |
| $t_{su(MI)}$ (1)<br>$t_{su(SI)}$ (1) | Data input setup time | Master mode | 4 | - | |
| | | Slave mode | 5 | - | |
| $t_{h(MI)}$ (1) | Data input hold time | Master mode | 4 | - | |
| $t_{h(SI)}$ (1) | | Slave mode | 5 | - | |
| $t_{a(SO)}$ (1)(2) | Data output access time | Slave mode, $f_{PCLK}$ = 20 MHz | 0 | 3Tpclk | |
| $t_{dis(SO)}$ (1)(3) | Data output disable time | Slave mode | 0 | 18 | |
| $t_{v(SO)}$ (1) | Data output valid time | Slave mode (after enable edge) | - | 22.5 | |
| $t_{v(MO)}$ (1) | Data output valid time | Master mode (after enable edge) | - | 6 | |
| $t_{h(SO)}$ (1) | Data output hold time | Slave mode (after enable edge) | 11.5 | - | |
| $t_{h(MO)}$ (1) | | Master mode (after enable edge) | 2 | - | |
| DuCy(SCK) | SPI slave input clock duty cycle | Slave mode | 25 | 75 | % |

1. Data based on characterization results, not tested in production.
2. Min time is for the minimum time to drive the output and the max time is for the maximum time to validate the data.
3. Min time is for the minimum time to invalidate the output and the max time is for the maximum time to put the data in Hi-Z

### Example 1: High-performance application

Assuming the following application conditions:

Maximum ambient temperature $T_{Amax}$ = 80 °C (measured according to JESD51-2), $I_{DDmax}$ = 50 mA, $V_{DD}$ = 3.5 V, maximum 20 I/Os used at the same time in output at low level with $I_{OL}$ = 8 mA, $V_{OL}$= 0.4 V and maximum 8 I/Os used at the same time in output at low level with $I_{OL}$ = 20 mA, $V_{OL}$= 1.3 V

$P_{INTmax}$ = 50 mA × 3.5 V= 175 mW

$P_{IOmax}$ = 20 × 8 mA × 0.4 V + 8 × 20 mA × 1.3 V = 272 mW

This gives: $P_{INTmax}$ = 175 mW and $P_{IOmax}$ = 272 mW:

$P_{Dmax}$ = 175 + 272 = 447 mW

Using the values obtained in Table 65 $T_{Jmax}$ is calculated as follows:

– For LQFP48, 55 °C/W

$T_{Jmax}$ = 80 °C + (55°C/W × 447 mW) = 80 °C + 24.585 °C = 104.585 °C

This is within the range of the suffix 6 version parts (–40 < $T_J$ < 105 °C) see Table 15: General operating conditions on page 39.

In this case, parts must be ordered at least with the temperature range suffix 6 (see Section 8: Part numbering).

Note: With this given $P_{Dmax}$ we can find the $T_{Amax}$ allowed for a given device temperature range (order code suffix 6 or 7).

Suffix 6: $T_{Amax}$ = $T_{Jmax}$ - (55℃/W ×447 mW) = 105-24.585 = 80.415 ℃

Suffix 7: $T_{Amax}$ = $T_{Jmax}$ - (55℃/W ×447 mW) = 125-24.585 = 100.415 ℃

### Example 2: High-temperature application

Using the same rules, it is possible to address applications that run at high ambient temperatures with a low dissipation, as long as junction temperature $T_J$ remains within the specified range.

Assuming the following application conditions:

Maximum ambient temperature $T_{Amax}$ = 100 °C (measured according to JESD51-2), $I_{DDmax}$ = 20 mA, $V_{DD}$ = 3.5 V, maximum 20 I/Os used at the same time in output at low level with $I_{OL}$ = 8 mA, $V_{OL}$= 0.4 V

$P_{INTmax}$ = 20 mA × 3.5 V= 70 mW

$P_{IOmax}$ = 20 × 8 mA × 0.4 V = 64 mW

This gives: $P_{INTmax}$ = 70 mW and $P_{IOmax}$ = 64 mW:

$P_{Dmax}$ = 70 + 64 = 134 mW

Thus: $P_{Dmax}$ = 134 mW

Using the values obtained in Table 65 $T_{Jmax}$ is calculated as follows:

– For LQFP48, 55 °C/W

$T_{Jmax}$ = 100 °C + (55 °C/W × 134 mW) = 100 °C + 7.37 °C = 107.37 °C

This is above the range of the suffix 6 version parts (–40 < $T_J$ < 105 °C).

In this case, parts must be ordered at least with the temperature range suffix 7 (see Section 8: Part numbering) unless we reduce the power dissipation in order to be able to use suffix 6 parts.