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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	DMA, I ² S, POR, PWM, WDT
Number of I/O	27
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 10x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-UFQFN Exposed Pad
Supplier Device Package	32-UFQFPN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f050k4u6a

2 Description

The STM32F050xx family incorporates the high-performance ARM Cortex™-M0 32-bit RISC core operating at a 48 MHz maximum frequency, high-speed embedded memories (Flash memory up to 32 Kbytes and SRAM up to 4 Kbytes), and an extensive range of enhanced peripherals and I/Os. All devices offer standard communication interfaces (one I²C, one SPI, one I2S, and one USART), one 12-bit ADC, up to five general-purpose 16-bit timers, a 32-bit timer and an advanced-control PWM timer.

The STM32F050xx family operates in the -40 to +85 °C and -40 to +105 °C temperature ranges, from a 2.0 to 3.6 V power supply. A comprehensive set of power-saving modes allows the design of low-power applications.

The STM32F050xx family includes devices in five different packages ranging from 20 pins to 48 pins. Depending on the device chosen, different sets of peripherals are included. An overview of the complete range of peripherals proposed in this family is provided.

These features make the STM32F050xx microcontroller family suitable for a wide range of applications such as control application and user interfaces, handheld equipment, A/V receivers and digital TV, PC peripherals, gaming and GPS platforms, industrial applications, PLCs, inverters, printers, scanners, alarm systems, video intercoms, and HVACs.

3.10 Analog to digital converter (ADC)

The 12-bit analog to digital converter has up to 16 external and 3 internal (temperature sensor, voltage reference, VBAT voltage measurement) channels and performs conversions in single-shot or scan modes. In scan mode, automatic conversion is performed on a selected group of analog inputs.

The ADC can be served by the DMA controller.

An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

3.10.1 Temperature sensor

The temperature sensor (TS) generates a voltage V_{SENSE} that varies linearly with temperature.

The temperature sensor is internally connected to the ADC_IN16 input channel which is used to convert the sensor output voltage into a digital value.

The sensor provides good linearity but it has to be calibrated to obtain good overall accuracy of the temperature measurement. As the offset of the temperature sensor varies from chip to chip due to process variation, the uncalibrated internal temperature sensor is suitable for applications that detect temperature changes only.

To improve the accuracy of the temperature sensor measurement, each device is individually factory-calibrated by ST. The temperature sensor factory calibration data are stored by ST in the system memory area, accessible in read-only mode.

Table 3. Temperature sensor calibration values

Calibration value name	Description	Memory address
TS_CAL1	TS ADC raw data acquired at temperature of 30 °C, $V_{DDA} = 3.3\text{ V}$	0x1FFF F7B8 - 0x1FFF F7B9
TS_CAL2	TS ADC raw data acquired at temperature of 110 °C $V_{DDA} = 3.3\text{ V}$	0x1FFF F7C2 - 0x1FFF F7C3

3.10.2 Internal voltage reference (V_{REFINT})

The internal voltage reference (V_{REFINT}) provides a stable (bandgap) voltage output for the ADC. V_{REFINT} is internally connected to the ADC_IN17 input channel. The precise voltage of V_{REFINT} is individually measured for each part by ST during production test and stored in the system memory area. It is accessible in read-only mode.

Table 4. Temperature sensor calibration values

Calibration value name	Description	Memory address
VREFINT_CAL	Raw data acquired at temperature of 30 °C $V_{DDA} = 3.3\text{ V}$	0x1FFF F7BA - 0x1FFF F7BB

3.15 Serial peripheral interface (SPI)/Inter-integrated sound interfaces (I²S)

The SPI (SPI1) is able to communicate up to 18 Mbits/s in slave and master modes in full-duplex and half-duplex communication modes. The 3-bit prescaler gives 8 master mode frequencies and the frame size is configurable from 4 bits to 16 bits.

One standard I²S interface (multiplexed with SPI1) supporting four different audio standards can operate as master or slave at half-duplex communication mode. It can be configured to transfer 16 and 24 or 32 bits with 16-bit or 32-bit data resolution and synchronized by a specific signal. Audio sampling frequency from 8 kHz up to 192 kHz can be set by 8-bit programmable linear prescaler. When operating in master mode it can output a clock for an external audio component at 256 times the sampling frequency.

3.16 Serial wire debug port (SW-DP)

An ARM SW-DP interface is provided to allow a serial wire debugging tool to be connected to the MCU.

4 Pinouts and pin description

Figure 3. LQFP48 48-pin package pinout

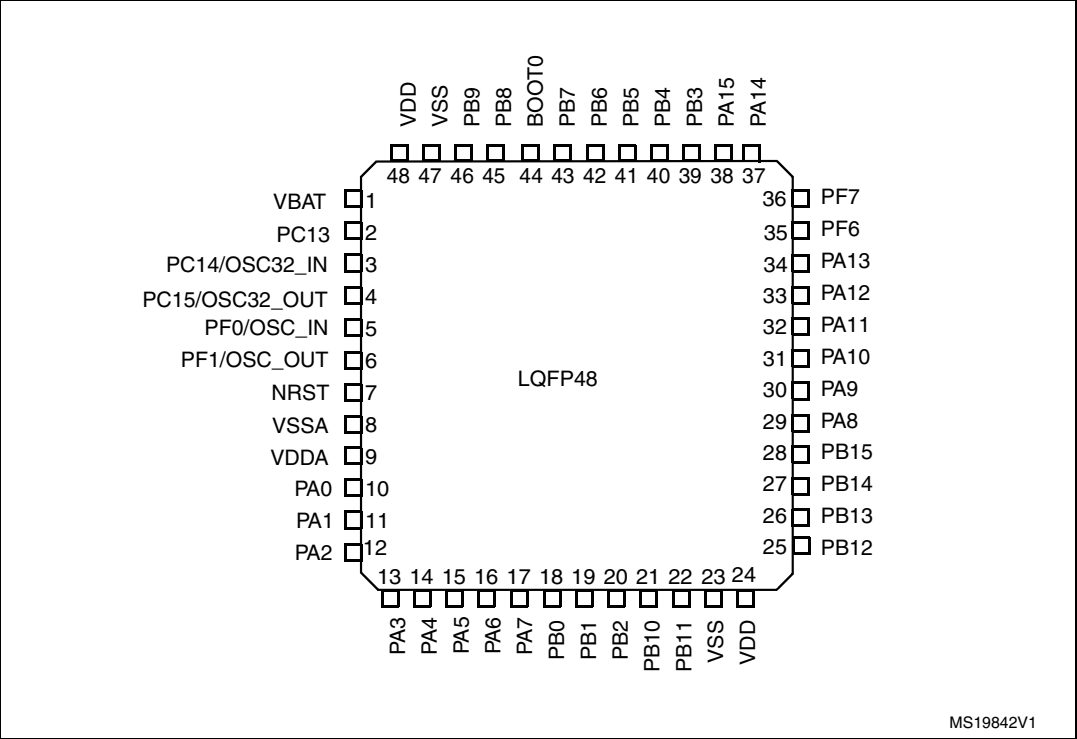


Figure 4. UFQFPN32 32-pin package pinout

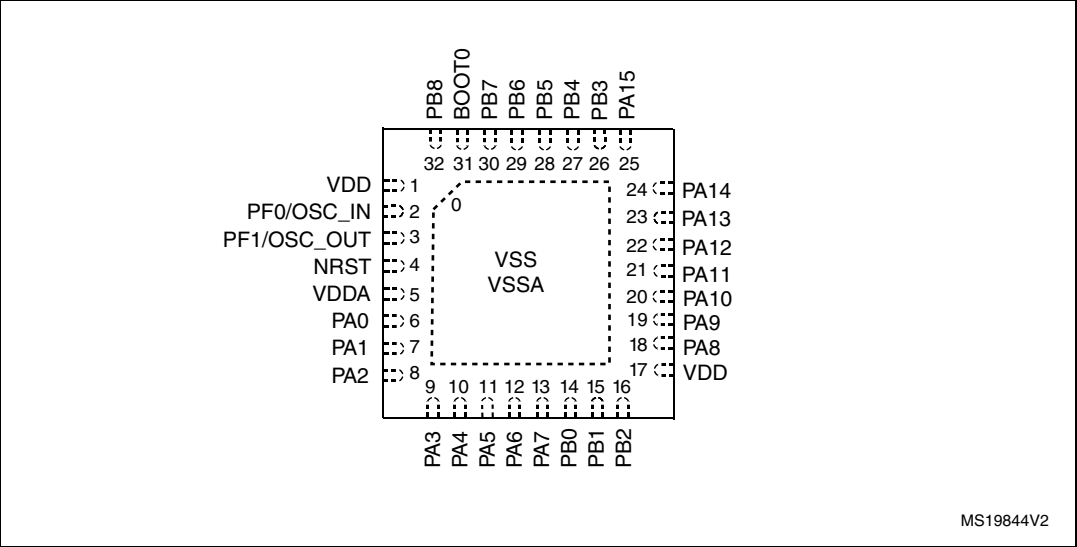
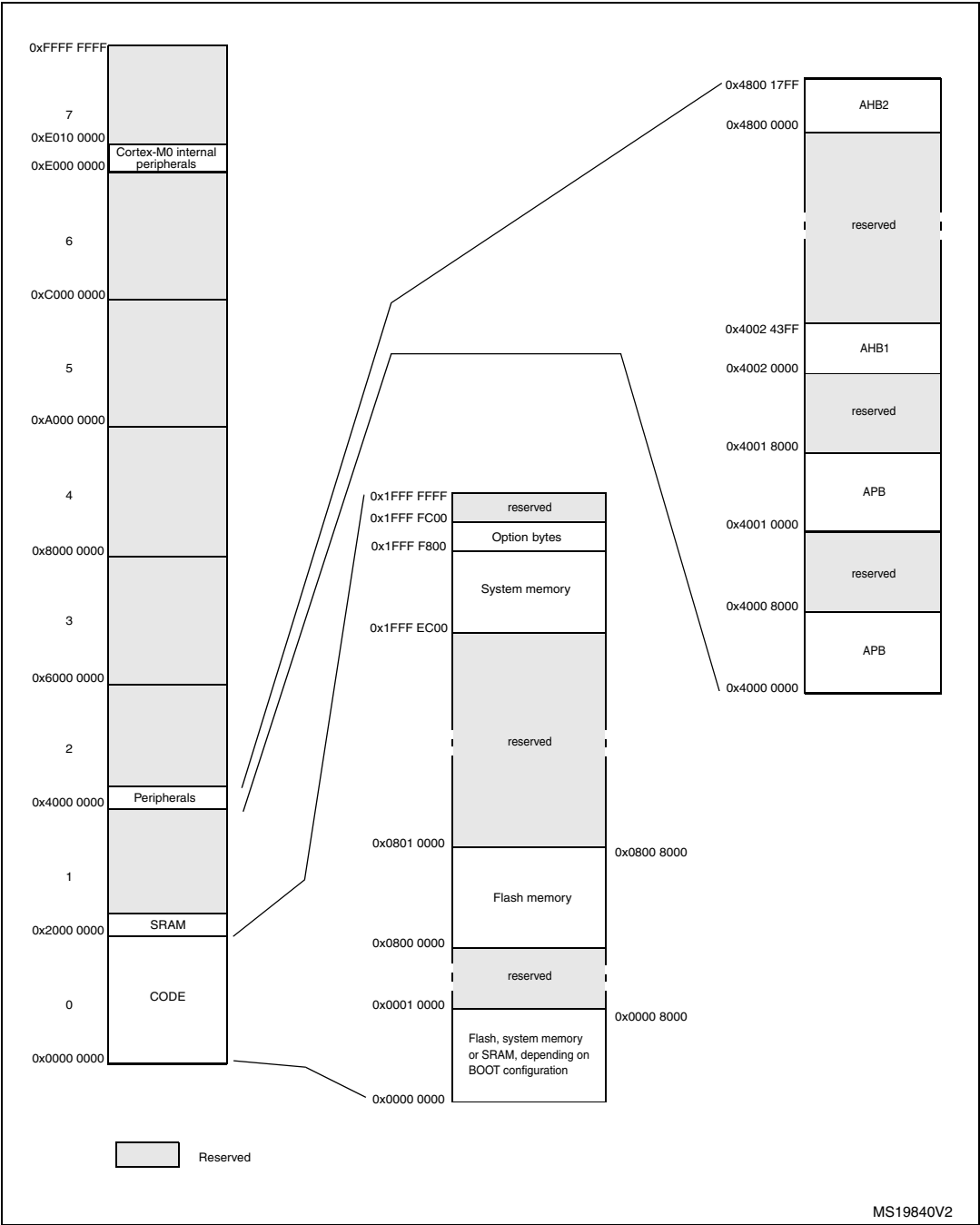


Table 8. Pin definitions (continued)

Pin number				Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP48	UFQFPN32	UFQFPN28	TSSOP20					Alternate functions	Additional functions
29	18	18	-	PA8	I/O	FT		USART1_CK, TIM1_CH1, EVENTOUT, MCO	
30	19	19	17	PA9	I/O	FTf		USART1_TX, TIM1_CH2, I2C1_SCL ⁽³⁾	
31	20	20	18	PA10	I/O	FTf		USART1_RX, TIM1_CH3, TIM17_BKIN, I2C1_SDA ⁽³⁾	
32	21	-	-	PA11	I/O	FT		USART1_CTS, TIM1_CH4, EVENTOUT	
33	22	-	-	PA12	I/O	FT		USART1_RTS, TIM1_ETR, EVENTOUT	
34	23	21	19	PA13 (SWDAT)	I/O	FT	(4)	IR_OUT, SWDAT	
35	-	-	-	PF6	I/O	FTf		I2C1_SCL ⁽³⁾	
36	-	-	-	PF7	I/O	FTf		I2C1_SDA ⁽³⁾	
37	24	22	20	PA14 (SWCLK)	I/O	FT	(4)	SWCLK, USART1_TX ⁽³⁾	
38	25	23	-	PA15	I/O	FT		SPI1_NSS, I2S1_WS, TIM2_CH_ETR, EVENTOUT, USART1_RX ⁽³⁾	
39	26	24	-	PB3	I/O	FT		SPI1_SCK, I2S1_CK, TIM2_CH2, EVENTOUT	
40	27	25	-	PB4	I/O	FT		SPI1_MISO, I2S1_MCK, TIM3_CH1, EVENTOUT	

5 Memory mapping

Figure 7. STM32F050xx memory map



2. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins referring to high pin count QFP packages.
3. Positive injection is not possible on these I/Os and does not occur for input voltages lower than the specified maximum value.
4. A positive injection is induced by $V_{IN} > V_{DD}$ while a negative injection is induced by $V_{IN} < V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to [Table 12: Voltage characteristics](#) for the maximum allowed input voltage values.
5. A positive injection is induced by $V_{IN} > V_{DDA}$ while a negative injection is induced by $V_{IN} < V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer also to [Table 12: Voltage characteristics](#) for the maximum allowed input voltage values. Negative injection disturbs the analog performance of the device. See note ⁽²⁾ below [Table 51: ADC accuracy](#).
6. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

Table 14. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	-65 to +150	°C
T_J	Maximum junction temperature	150	°C

Table 25. Typical current consumption in Run mode, code with data processing running from Flash

Symbol	Parameter	Conditions	f _{HCLK}	Typ		Unit
				Peripherals enabled	Peripherals disabled	
I _{DD}	Supply current in Run mode from V _{DD} supply	Running from HSE crystal clock 8 MHz, code executing from Flash	48 MHz	18.4	11.4	mA
			36 MHz	13.9	8.9	
			32 MHz	12.4	7.9	
			24 MHz	9.9	6.2	
			16 MHz	6.6	4.3	
			8 MHz	3.3	2.2	
			4 MHz	1.7	1.6	
			2 MHz	1.3	1.2	
			1 MHz	0.8	0.7	
			500 kHz	0.6	0.6	
I _{DDA}	Supply current in Run mode from V _{DDA} supply	Running from HSE crystal clock 8 MHz, code executing from Flash	48 MHz	140	140	μA
			36 MHz	109	109	
			32 MHz	96	96	
			24 MHz	76	76	
			16 MHz	51	51	
			8 MHz	1.7	1.7	
			4 MHz	1.6	1.6	
			2 MHz	1.5	1.5	
			1 MHz	1.1	1.1	
			500 kHz	1.1	1.1	

Table 26. Typical current consumption in Sleep mode, code running from Flash or RAM

Symbol	Parameter	Conditions	f _{HCLK}	Typ		Unit
				Peripherals enabled	Peripherals disabled	
I _{DD}	Supply current in Sleep mode from V _{DD} supply	Running from HSE crystal clock 8 MHz, code executing from Flash or RAM	48 MHz	10.7	2.4	mA
			36 MHz	8.1	1.8	
			32 MHz	7.1	1.6	
			24 MHz	5.5	1.3	
			16 MHz	3.7	0.9	
			8 MHz	1.9	0.5	
			4 MHz	1.5	0.4	
			2 MHz	1.1	0.3	
			1 MHz	0.8	0.3	
			500 kHz	0.6	0.3	
			125 kHz	0.5	0.3	
I _{DDA}	Supply current in Sleep mode from V _{DDA} supply	Running from HSE crystal clock 8 MHz, code executing from Flash or RAM	48 MHz	140	140	μA
			36 MHz	109	109	
			32 MHz	96	96	
			24 MHz	76	76	
			16 MHz	51	51	
			8 MHz	1.7	1.7	
			4 MHz	1.6	1.6	
			2 MHz	1.5	1.5	
			1 MHz	1.1	1.1	
			500 kHz	1.1	1.1	
			125 kHz	1.1	1.1	

On-chip peripheral current consumption

The current consumption of the on-chip peripherals is given in [Table 28](#). The MCU is placed under the following conditions:

- all I/O pins are in input mode with a static value at V_{DD} or V_{SS} (no load)
- all peripherals are disabled unless otherwise mentioned
- the given value is calculated by measuring the current consumption
 - with all peripherals clocked off
 - with only one peripheral clocked on
- ambient operating temperature and V_{DD} supply voltage conditions summarized in [Table 12: Voltage characteristics](#)

Table 28. Peripheral current consumption

Peripheral	Typical consumption at 25 °C		Unit
	I_{DD}	I_{DDA}	
ADC ⁽¹⁾	0.53	0.964	mA
CRC	0.10	-	
DBGMCU	0.18	-	
DMA	0.35	-	
GPIOA	0.48	-	
GPIOB	0.58	-	
GPIOC	0.12	-	
GPIOF	0.06	-	
I2C1	0.43	-	
PWR	0.22	-	
SPI1/I2S1	0.63	-	
SYSCFG	0.28	-	
TIM1	1.01	-	
TIM2	1.00	-	
TIM3	0.78	-	
TIM6	0.32	-	
TIM14	0.45	-	
TIM16	0.57	-	
TIM17	0.59	-	
USART1	1.07	-	
WWDG	0.22	-	

1. ADC is in ready state after setting the ADEN bit in the ADC_CR register (ADRDY bit in ADC_ISR is high).

6.3.6 External clock source characteristics

High-speed external user clock generated from an external source

In bypass mode the HSE oscillator is switched off and the input pin is a standard GPIO.

The external clock signal has to respect the I/O characteristics in [Section 6.3.13](#). However, the recommended clock input waveform is shown in [Figure 12: High-speed external clock source AC timing diagram](#).

Table 29. High-speed external user clock characteristics

Symbol	Parameter ⁽¹⁾	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	User external clock source frequency		1	8	32	MHz
V_{HSEH}	OSC_IN input pin high level voltage		$0.7V_{DD}$	-	V_{DD}	V
V_{HSEL}	OSC_IN input pin low level voltage		V_{SS}	-	$0.3V_{DD}$	
$t_{w(HSEH)}$ $t_{w(HSEL)}$	OSC_IN high or low time		15	-	-	ns
$t_r(HSE)$ $t_f(HSE)$	OSC_IN rise or fall time		-	-	20	

1. Guaranteed by design, not tested in production.

Figure 12. High-speed external clock source AC timing diagram

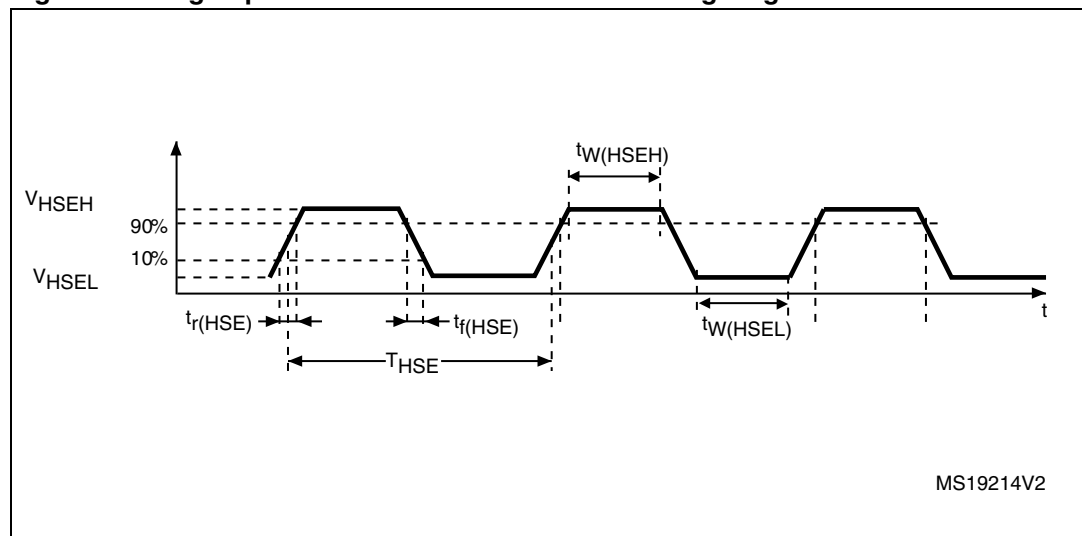
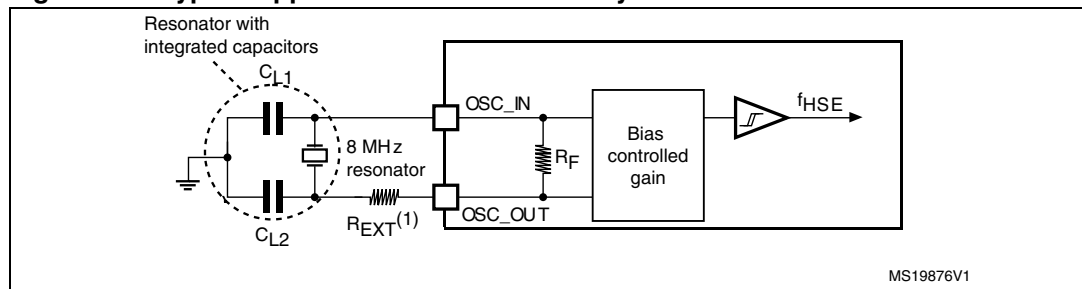


Figure 14. Typical application with an 8 MHz crystal

1. R_{EXT} value depends on the crystal characteristics.

Low-speed external clock generated from a crystal resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in [Table 32](#). In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 32. LSE oscillator characteristics ($f_{LSE} = 32.768$ kHz)

Symbol	Parameter	Conditions ⁽¹⁾	Min ⁽²⁾	Typ	Max ⁽²⁾	Unit
I_{DD}	LSE current consumption	LSEDRV[1:0]=00 lower driving capability	-	0.5	0.9	μA
		LSEDRV[1:0]= 01 medium low driving capability	-	-	1	
		LSEDRV[1:0] = 10 medium high driving capability	-	-	1.3	
		LSEDRV[1:0]=11 higher driving capability	-	-	1.6	
g_m	Oscillator transconductance	LSEDRV[1:0]=00 lower driving capability	5	-	-	$\mu A/V$
		LSEDRV[1:0]= 01 medium low driving capability	8	-	-	
		LSEDRV[1:0] = 10 medium high driving capability	15	-	-	
		LSEDRV[1:0]=11 higher driving capability	25	-	-	
$t_{SU(LSE)}^{(3)}$	Startup time	V_{DD} is stabilized	-	2	-	s

1. Refer to the note and caution paragraphs below the table, and to the application note AN2867 "Oscillator design guide for ST microcontrollers".

2. Guaranteed by design, not tested in production.

3. $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal and it can vary significantly with the crystal manufacturer

Note: For information on selecting the crystal, refer to the application note AN2867 "Oscillator design guide for ST microcontrollers" available from the ST website www.st.com.

Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to +/-8 mA, and sink or source up to +/- 20 mA (with a relaxed V_{OL}/V_{OH}).

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in [Section 6.2](#):

- The sum of the currents sourced by all the I/Os on V_{DD} , plus the maximum Run consumption of the MCU sourced on V_{DD} , cannot exceed the absolute maximum rating I_{VDD} (see [Table 13: Current characteristics](#)).
- The sum of the currents sunk by all the I/Os on V_{SS} plus the maximum Run consumption of the MCU sunk on V_{SS} cannot exceed the absolute maximum rating I_{VSS} (see [Table 13: Current characteristics](#)).

Output voltage levels

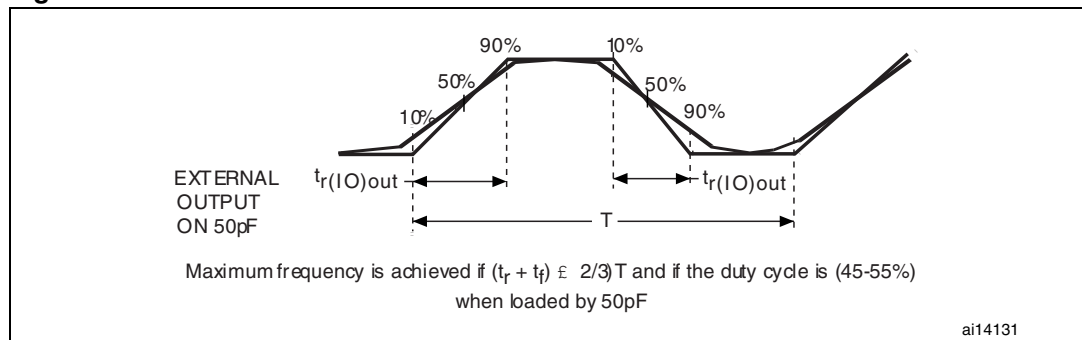
Unless otherwise specified, the parameters given in [Table 46](#) are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in [Table 15: General operating conditions](#). All I/Os are CMOS and TTL compliant (FT, TTA or TC unless otherwise specified).

Table 46. Output voltage characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{OL}^{(1)}$	Output low level voltage for an I/O pin	CMOS port ⁽²⁾ $I_{IO} = +8 \text{ mA}$ $2.7 \text{ V} < V_{DD} < 3.6 \text{ V}$	-	0.4	V
$V_{OH}^{(3)}$	Output high level voltage for an I/O pin		$V_{DD}-0.4$	-	
$V_{OL}^{(1)}$	Output low level voltage for an I/O pin	TTL port ⁽²⁾ $I_{IO} = +8 \text{ mA}$ $2.7 \text{ V} < V_{DD} < 3.6 \text{ V}$	-	0.4	V
$V_{OH}^{(3)}$	Output high level voltage for an I/O pin		2.4	-	
$V_{OL}^{(1)(4)}$	Output low level voltage for an I/O pin	$I_{IO} = +20 \text{ mA}$ $2.7 \text{ V} < V_{DD} < 3.6 \text{ V}$	-	1.3	V
$V_{OH}^{(3)(4)}$	Output high level voltage for an I/O pin		$V_{DD}-1.3$	-	
$V_{OL}^{(1)(4)}$	Output low level voltage for an I/O pin	$I_{IO} = +6 \text{ mA}$ $2 \text{ V} < V_{DD} < 2.7 \text{ V}$	-	0.4	V
$V_{OH}^{(3)(4)}$	Output high level voltage for an I/O pin		$V_{DD}-0.4$	-	
$V_{OLFM+}^{(1)}$	Output low level voltage for an FTf I/O pin in FM+ mode	$I_{IO} = +20 \text{ mA}$ $2.7 \text{ V} < V_{DD} < 3.6 \text{ V}$	-	0.4	V

1. The I_{IO} current sunk by the device must always respect the absolute maximum rating specified in [Table 13: Current characteristics](#) and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS} .
2. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.
3. The I_{IO} current sourced by the device must always respect the absolute maximum rating specified in [Table 13: Current characteristics](#) and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VDD} .
4. Data based on design simulation only. Not tested in production.

Figure 22. I/O AC characteristics definition



6.3.14 NRST pin characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, R_{PU} (see [Table 45: I/O static characteristics](#)).

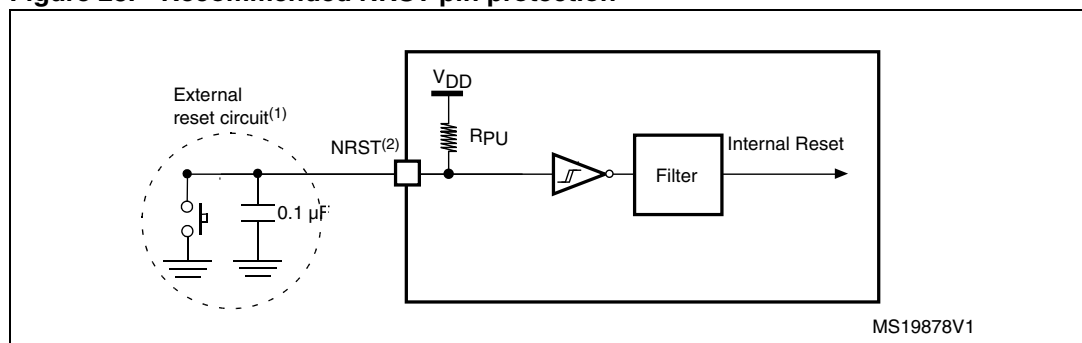
Unless otherwise specified, the parameters given in [Table 48](#) are derived from tests performed under ambient temperature and VDD supply voltage conditions summarized in [Table 15: General operating conditions](#).

Table 48. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}^{(1)}$	NRST input low level voltage		-0.3	-	0.8	V
$V_{IH(NRST)}^{(1)}$	NRST input high level voltage		2	-	$V_{DD}+0.3$	
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis		-	200	-	mV
R_{PU}	Weak pull-up equivalent resistor ⁽²⁾	$V_{IN} = V_{SS}$	25	40	55	k Ω
$V_{F(NRST)}^{(1)}$	NRST input filtered pulse		-	-	100	ns
$V_{NF(NRST)}^{(1)}$	NRST input not filtered pulse		300	-	-	ns

1. Guaranteed by design, not tested in production.
2. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance must be minimum (~10% order).

Figure 23. Recommended NRST pin protection



1. The reset network protects the device against parasitic resets.
2. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in [Table 48](#). Otherwise the reset will not be taken into account by the device.

6.3.16 Temperature sensor characteristics

Table 52. TS characteristics

Symbol	Parameter	Min	Typ	Max	Unit
$T_L^{(1)}$	V_{SENSE} linearity with temperature	-	± 1	± 2	$^{\circ}\text{C}$
Avg_Slope ⁽¹⁾	Average slope	4.0	4.3	4.6	mV/ $^{\circ}\text{C}$
V_{25}	Voltage at 25 $^{\circ}\text{C}$	1.34	1.43	1.52	V
$t_{START}^{(1)}$	Startup time	4	-	10	μs
$T_{S_temp}^{(1)(2)}$	ADC sampling time when reading the temperature	17.1	-	-	μs

1. Guaranteed by design, not tested in production.

2. Shortest sampling time can be determined in the application by multiple iterations.

6.3.17 V_{BAT} monitoring characteristics

Table 53. V_{BAT} monitoring characteristics

Symbol	Parameter	Min	Typ	Max	Unit
R	Resistor bridge for V_{BAT}	-	50	-	$\text{K}\Omega$
Q	Ratio on V_{BAT} measurement	-	2	-	
$E_r^{(1)}$	Error on Q	-1	-	+1	%
$T_{S_vbat}^{(1)(2)}$	ADC sampling time when reading the V_{BAT} 1mV accuracy	5	-	-	μs

1. Guaranteed by design, not tested in production.

2. Shortest sampling time can be determined in the application by multiple iterations.

6.3.18 Timer characteristics

The parameters given in [Table 54](#) are guaranteed by design.

Refer to [Section 6.3.13: I/O port characteristics](#) for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table 54. TIMx⁽¹⁾ characteristics

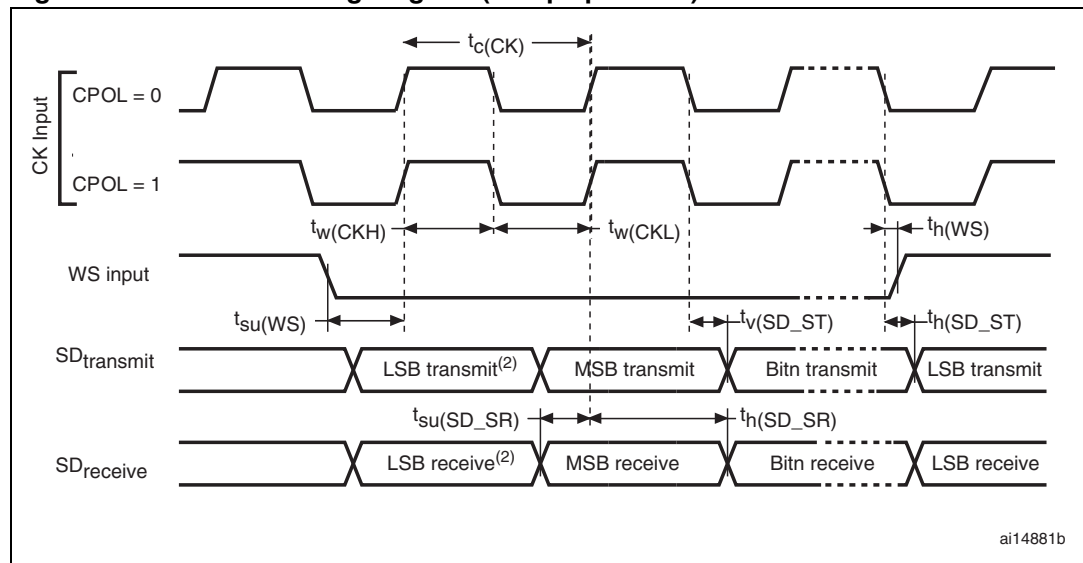
Symbol	Parameter	Conditions	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time		1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK} = 48 \text{ MHz}$	20.8	-	ns
f_{EXT}	Timer external clock frequency on CH1 to CH4		0	$f_{TIMxCLK}/2$	MHz
		$f_{TIMxCLK} = 48 \text{ MHz}$	0	24	MHz
Res_{TIM}	Timer resolution	TIMx (except TIM2)	-	16	bit
		TIM2	-	32	

Table 60. I²S characteristics

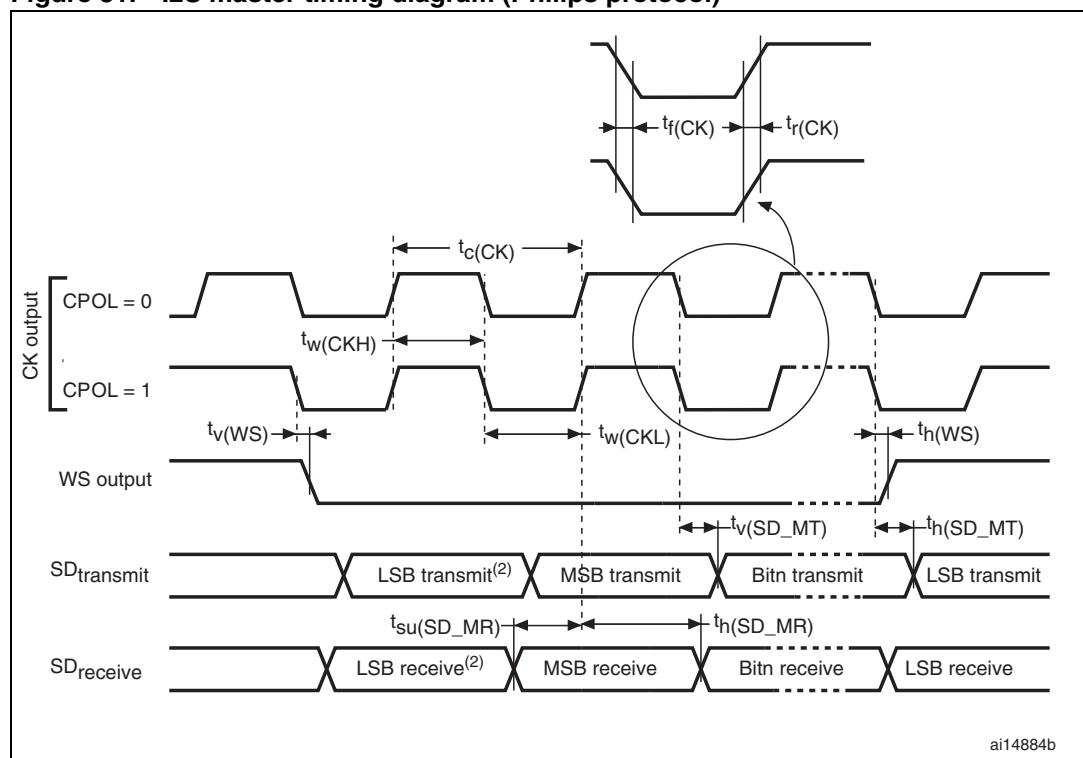
Symbol	Parameter	Conditions	Min	Max	Unit
f_{CK} $1/t_{c(CK)}$	I ² S clock frequency	Master mode (data: 16 bits, Audio frequency = 48 kHz)	1.597	1.601	MHz
		Slave mode	0	6.5	
$t_{r(CK)}$	I ² S clock rise time	Capacitive load $C_L = 15$ pF	-	10	ns
$t_{f(CK)}$	I ² S clock fall time		-	12	
$t_{w(CKH)}^{(1)}$	I2S clock high time	Master $f_{PCLK} = 16$ MHz, audio frequency = 48 kHz	306	-	
$t_{w(CKL)}^{(1)}$	I2S clock low time		312	-	
$t_{v(WS)}^{(1)}$	WS valid time	Master mode	2	-	
$t_{h(WS)}^{(1)}$	WS hold time	Master mode	2	-	
$t_{su(WS)}^{(1)}$	WS setup time	Slave mode	7	-	
$t_{h(WS)}^{(1)}$	WS hold time	Slave mode	0	-	
DuCy(SCK)	I2S slave input clock duty cycle	Slave mode	25	75	%
$t_{su(SD_MR)}^{(1)}$	Data input setup time	Master receiver	6	-	ns
$t_{su(SD_SR)}^{(1)}$	Data input setup time	Slave receiver	2	-	
$t_{h(SD_MR)}^{(1)(2)}$	Data input hold time	Master receiver	4	-	
$t_{h(SD_SR)}^{(1)(2)}$		Slave receiver	0.5	-	
$t_{v(SD_ST)}^{(1)(2)}$	Data output valid time	Slave transmitter (after enable edge)	-	20	
$t_{h(SD_ST)}^{(1)}$	Data output hold time	Slave transmitter (after enable edge)	13	-	
$t_{v(SD_MT)}^{(1)(2)}$	Data output valid time	Master transmitter (after enable edge)	-	4	
$t_{h(SD_MT)}^{(1)}$	Data output hold time	Master transmitter (after enable edge)	0	-	

1. Data based on design simulation and/or characterization results, not tested in production.

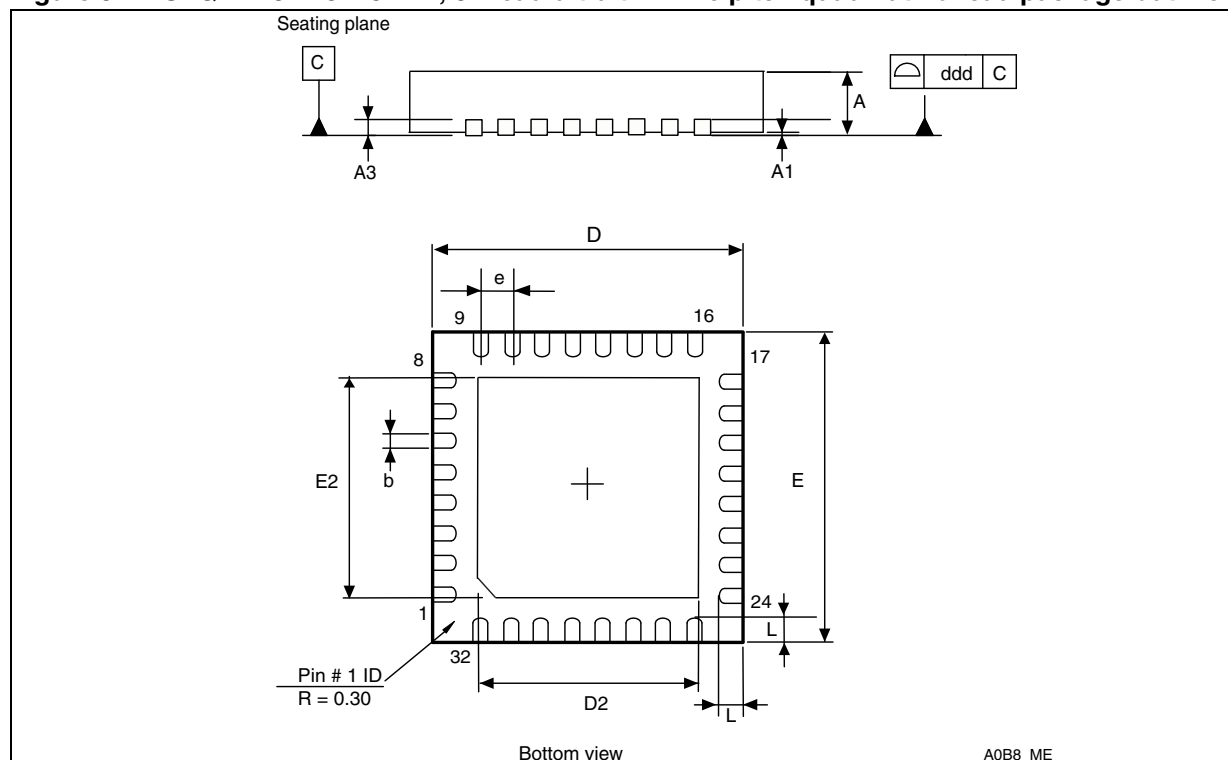
2. Depends on f_{PCLK} . For example, if $f_{PCLK} = 8$ MHz, then $T_{PCLK} = 1/f_{PCLK} = 125$ ns.

Figure 30. I2S slave timing diagram (Philips protocol)

1. Measurement points are done at CMOS levels: $0.3 \times V_{DD}$ and $0.7 \times V_{DD}$.
2. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

Figure 31. I2S master timing diagram (Philips protocol)

1. Data based on characterization results, not tested in production.
2. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

Figure 34. UFQFPN32 - 5 x 5 mm, 32-lead ultra thin fine pitch quad flat no-lead package outline

1. Drawing is not to scale.
2. All leads/pads should also be soldered to the PCB to improve the lead/pad solder joint life.
3. There is an exposed die pad on the underside of the UFQFPN package. This pad is used for the device ground and must be connected. It is referred to as pin 0 in [Table 8: Pin definitions](#).

Table 62. UFQFPN32 – 5 x 5 mm, 32-lead ultra thin fine pitch quad flat no-lead package mechanical data

Dim.	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
A	0.5	0.55	0.6	0.0197	0.0217	0.0236
A1	0.00	0.02	0.05	0	0.0008	0.0020
A3		0.152			0.006	
b	0.18	0.23	0.28	0.0071	0.0091	0.0110
D	4.90	5.00	5.10	0.1929	0.1969	0.2008
D2		3.50			0.1378	
E	4.90	5.00	5.10	0.1929	0.1969	0.2008
E2	3.40	3.50	3.60	0.1339	0.1378	0.1417
e		0.500			0.0197	
L	0.30	0.40	0.50	0.0118	0.0157	0.0197
ddd	0.08			0.0031		

1. Values in inches are converted from mm and rounded to 4 decimal digits.

7.2 Thermal characteristics

The maximum chip junction temperature (T_{Jmax}) must never exceed the values given in [Table 15: General operating conditions on page 39](#).

The maximum chip-junction temperature, T_J max, in degrees Celsius, may be calculated using the following equation:

$$T_J \text{ max} = T_A \text{ max} + (P_D \text{ max} \times \Theta_{JA})$$

Where:

- T_A max is the maximum ambient temperature in °C,
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W,
- P_D max is the sum of P_{INT} max and $P_{I/O}$ max ($P_D \text{ max} = P_{INT} \text{ max} + P_{I/O} \text{ max}$),
- P_{INT} max is the product of I_{DD} and V_{DD} , expressed in Watts. This is the maximum chip internal power.

$P_{I/O}$ max represents the maximum power dissipation on output pins where:

$$P_{I/O} \text{ max} = \Sigma (V_{OL} \times I_{OL}) + \Sigma ((V_{DD} - V_{OH}) \times I_{OH}),$$

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Table 65. Package thermal characteristics

Symbol	Parameter	Value	Unit
Θ_{JA}	Thermal resistance junction-ambient LQFP48 - 7 × 7 mm	55	°C/W
	Thermal resistance junction-ambient UFQFPN32 - 5 × 5 mm	38	
	Thermal resistance junction-ambient UFQFPN28 - 4 × 4 mm	118	
	Thermal resistance junction-ambient TSSOP20	110	

7.2.1 Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org

7.2.2 Selecting the product temperature range

When ordering the microcontroller, the temperature range is specified in the ordering information scheme shown in [Section 8: Part numbering](#).

Each temperature range suffix corresponds to a specific guaranteed ambient temperature at maximum dissipation and, to a specific maximum junction temperature.

As applications do not commonly use the STM32F05xx at maximum dissipation, it is useful to calculate the exact power consumption and junction temperature to determine which temperature range will be best suited to the application.

The following examples show how to calculate the temperature range needed for a given application.

Example 1: High-performance application

Assuming the following application conditions:

Maximum ambient temperature $T_{Amax} = 80\text{ }^{\circ}\text{C}$ (measured according to JESD51-2),
 $I_{DDmax} = 50\text{ mA}$, $V_{DD} = 3.5\text{ V}$, maximum 20 I/Os used at the same time in output at low level with $I_{OL} = 8\text{ mA}$, $V_{OL} = 0.4\text{ V}$ and maximum 8 I/Os used at the same time in output at low level with $I_{OL} = 20\text{ mA}$, $V_{OL} = 1.3\text{ V}$

$$P_{INTmax} = 50\text{ mA} \times 3.5\text{ V} = 175\text{ mW}$$

$$P_{IOmax} = 20 \times 8\text{ mA} \times 0.4\text{ V} + 8 \times 20\text{ mA} \times 1.3\text{ V} = 272\text{ mW}$$

This gives: $P_{INTmax} = 175\text{ mW}$ and $P_{IOmax} = 272\text{ mW}$:

$$P_{Dmax} = 175 + 272 = 447\text{ mW}$$

Using the values obtained in [Table 65](#) T_{Jmax} is calculated as follows:

– For LQFP48, $55\text{ }^{\circ}\text{C/W}$

$$T_{Jmax} = 80\text{ }^{\circ}\text{C} + (55\text{ }^{\circ}\text{C/W} \times 447\text{ mW}) = 80\text{ }^{\circ}\text{C} + 24.585\text{ }^{\circ}\text{C} = 104.585\text{ }^{\circ}\text{C}$$

This is within the range of the suffix 6 version parts ($-40 < T_J < 105\text{ }^{\circ}\text{C}$) see [Table 15: General operating conditions on page 39](#).

In this case, parts must be ordered at least with the temperature range suffix 6 (see [Section 8: Part numbering](#)).

Note: With this given P_{Dmax} we can find the T_{Amax} allowed for a given device temperature range (order code suffix 6 or 7).

$$\text{Suffix 6: } T_{Amax} = T_{Jmax} - (55\text{ }^{\circ}\text{C/W} \times 447\text{ mW}) = 105 - 24.585 = 80.415\text{ }^{\circ}\text{C}$$

$$\text{Suffix 7: } T_{Amax} = T_{Jmax} - (55\text{ }^{\circ}\text{C/W} \times 447\text{ mW}) = 125 - 24.585 = 100.415\text{ }^{\circ}\text{C}$$

Example 2: High-temperature application

Using the same rules, it is possible to address applications that run at high ambient temperatures with a low dissipation, as long as junction temperature T_J remains within the specified range.

Assuming the following application conditions:

Maximum ambient temperature $T_{Amax} = 100\text{ }^{\circ}\text{C}$ (measured according to JESD51-2),
 $I_{DDmax} = 20\text{ mA}$, $V_{DD} = 3.5\text{ V}$, maximum 20 I/Os used at the same time in output at low level with $I_{OL} = 8\text{ mA}$, $V_{OL} = 0.4\text{ V}$

$$P_{INTmax} = 20\text{ mA} \times 3.5\text{ V} = 70\text{ mW}$$

$$P_{IOmax} = 20 \times 8\text{ mA} \times 0.4\text{ V} = 64\text{ mW}$$

This gives: $P_{INTmax} = 70\text{ mW}$ and $P_{IOmax} = 64\text{ mW}$:

$$P_{Dmax} = 70 + 64 = 134\text{ mW}$$

Thus: $P_{Dmax} = 134\text{ mW}$

Using the values obtained in [Table 65](#) T_{Jmax} is calculated as follows:

– For LQFP48, $55\text{ }^{\circ}\text{C/W}$

$$T_{Jmax} = 100\text{ }^{\circ}\text{C} + (55\text{ }^{\circ}\text{C/W} \times 134\text{ mW}) = 100\text{ }^{\circ}\text{C} + 7.37\text{ }^{\circ}\text{C} = 107.37\text{ }^{\circ}\text{C}$$

This is above the range of the suffix 6 version parts ($-40 < T_J < 105\text{ }^{\circ}\text{C}$).

In this case, parts must be ordered at least with the temperature range suffix 7 (see [Section 8: Part numbering](#)) unless we reduce the power dissipation in order to be able to use suffix 6 parts.