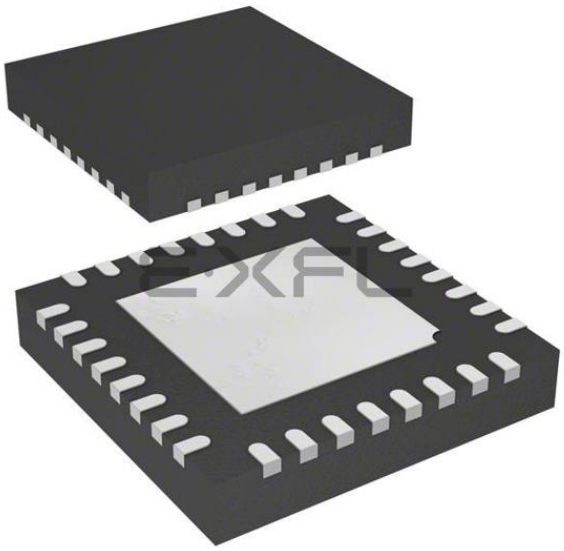

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	DMA, I²S, POR, PWM, WDT
Number of I/O	27
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 10x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-UFQFN Exposed Pad
Supplier Device Package	32-UFQFPN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f050k6u6a

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1 Introduction

This datasheet provides the ordering information and mechanical device characteristics of the STM32F050x4 and STM32F050x6 microcontrollers, hereafter referred to as STM32F050xx.

This datasheet should be read in conjunction with the STM32F0xxxx reference manual (RM0091). The reference manual is available from the STMicroelectronics website www.st.com.

For information on the ARM Cortex™-M0 core, please refer to the Cortex™-M0 Technical Reference Manual, available from the www.arm.com website at the following address: http://infocenter.arm.com/help/index.jsp?topic=/com.arm.doc.ddi0432c/index.html.

3 Functional overview

3.1 ARM® Cortex™-M0 core with embedded Flash and SRAM

The ARM Cortex™-M0 processor is the latest generation of ARM processors for embedded systems. It has been developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced system response to interrupts.

The ARM Cortex™-M0 32-bit RISC processor features exceptional code-efficiency, delivering the high-performance expected from an ARM core in the memory size usually associated with 8- and 16-bit devices.

The STM32F050xx family has an embedded ARM core and is therefore compatible with all ARM tools and software.

Figure 1 shows the general block diagram of the device family.

3.2 Memories

The device has the following features:

- 4 Kbytes of embedded SRAM accessed (read/write) at CPU clock speed with 0 wait states and featuring embedded parity checking with exception generation for fail-critical applications.
- The non-volatile memory is divided into two arrays:
  - 16 to 32 Kbytes of embedded Flash memory for programs and data
  - Option bytes

  The option bytes are used to write-protect the memory (with 4 KB granularity) and/or readout-protect the whole memory with the following options:
  - Level 0: no readout protection
  - Level 1: memory readout protection, the Flash memory cannot be read from or written to if either debug features are connected or boot in RAM is selected
  - Level 2: chip readout protection, debug features (Cortex-M0 serial wire) and boot in RAM selection disabled

3.3 Boot modes

At startup, the boot pin and boot selector option bit are used to select one of three boot options:

- Boot from User Flash
- Boot from System Memory
- Boot from embedded SRAM

The boot loader is located in System Memory. It is used to reprogram the Flash memory by using USART1.

3.4 Cyclic redundancy check calculation unit (CRC)

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code from a 32-bit data word and a CRC-32 (Ethernet) polynomial.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

3.5 Power management

3.5.1 Power supply schemes

- V_{DD} = 2.0 to 3.6 V: external power supply for I/Os and the internal regulator. Provided externally through V_{DD} pins.
- V_{DDA} = 2.0 to 3.6 V: external analog power supply for ADC, Reset blocks, RCs and PLL (minimum voltage to be applied to V_{DDA} is 2.4 V when the ADC is used). The V_{DDA} voltage level must be always greater or equal to the V_{DD} voltage level and must be provided first.
- V_{BAT} = 1.65 to 3.6 V: power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when V_{DD} is not present.

3.5.2 Power supply supervisors

The device has integrated power-on reset (POR) and power-down reset (PDR) circuits. They are always active, and ensure proper operation above a threshold of 2 V. The device remains in reset mode when the monitored supply voltage is below a specified threshold, $V_{POR/PDR}$, without the need for an external reset circuit.

- The POR monitors only the V_{DD} supply voltage. During the startup phase it is required that V_{DDA} should arrive first and be greater than or equal to V_{DD}.
- The PDR monitors both the V_{DD} and V_{DDA} supply voltages, however the V_{DDA} power supply supervisor can be disabled (by programming a dedicated Option bit) to reduce the power consumption if the application design ensures that V_{DDA} is higher than or equal to V_{DD}.

The device features an embedded programmable voltage detector (PVD) that monitors the V_{DD} power supply and compares it to the V_{PVD} threshold. An interrupt can be generated when V_{DD} drops below the V_{PVD} threshold and/or when V_{DD} is higher than the V_{PVD} threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

3.11.5 SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard down counter. It features:

- A 24-bit down counter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0.
- Programmable clock source (HCLK or HCLK/8)

3.12 Real-time clock (RTC) and backup registers

The RTC and the 5 backup registers are supplied through a switch that takes power either on V_{DD} supply when present or through the V_{BAT} pin. The backup registers are five 32-bit registers used to store 20 bytes of user application data when V_{DD} power is not present. They are not reset by a system or power reset, or when the device wakes up from Standby mode.

The RTC is an independent BCD timer/counter. Its main features are the following:

- Calendar with subsecond, seconds, minutes, hours (12 or 24 format), week day, date, month, year, in BCD (binary-coded decimal) format.
- Automatically correction for 28, 29 (leap year), 30, and 31 day of the month.
- Programmable alarm with wake up from Stop and Standby mode capability.
- On-the-fly correction from 1 to 32767 RTC clock pulses. This can be used to synchronize it with a master clock.
- Digital calibration circuit with 1 ppm resolution, to compensate for quartz crystal inaccuracy.
- 2 anti-tamper detection pins with programmable filter. The MCU can be woken up from Stop and Standby modes on tamper event detection.
- Timestamp feature which can be used to save the calendar content. This function can triggered by an event on the timestamp pin, or by a tamper event. The MCU can be woken up from Stop and Standby modes on timestamp event detection.

The RTC clock sources can be:

- A 32.768 kHz external crystal
- A resonator or oscillator
- The internal low-power RC oscillator (typical frequency of 40 kHz)
- The high-speed external clock divided by 32.

3.13 Inter-integrated circuit interface (I^2C)

The I^2C interface (I2C1) can operate in multimaster or slave mode. It can support Standard mode (up to 100 kbit/s), Fast mode (up to 400 kbit/s) and Fast Mode Plus (up to 1 Mbit/s) with 20 mA output drive.

It supports 7-bit and 10-bit addressing modes, multiple 7-bit slave addresses (2 addresses, 1 with configurable mask). It also includes programmable analog and digital noise filters.

Table 6. Comparison of I2C analog and digital filters

	Analog filter	Digital filter
Pulse width of suppressed spikes	≥ 50 ns	Programmable length from 1 to 15 I2C peripheral clocks
Benefits	Available in Stop mode	1. Extra filtering capability vs. standard requirements. 2. Stable length
Drawbacks	Variations depending on temperature, voltage, process	Wakeup from Stop on address match is not available when digital filter is enabled.

In addition, I2C1 provides hardware support for SMBUS 2.0 and PMBUS 1.1: ARP capability, Host notify protocol, hardware CRC (PEC) generation/verification, timeouts verifications and ALERT protocol management. I2C1 also has a clock domain independent from the CPU clock, allowing the I2C1 to wake up the MCU from Stop mode on address match.

The I2C interface can be served by the DMA controller.

3.14 Universal synchronous/asynchronous receiver transmitter (USART)

The device embeds an universal synchronous/asynchronous receiver transmitters (USART1), which communicates at speeds of up to 6 Mbit/s.

It provides hardware management of the CTS, RTS and RS485 DE signals, multiprocessor communication mode, master synchronous communication and single-wire half-duplex communication mode. It also supports SmartCard communication (ISO 7816), IrDA SIR ENDEC, LIN Master/Slave capability, auto baud rate feature and has a clock domain independent from the CPU clock, allowing it to wake up the MCU from Stop mode.

The USART interface can be served by the DMA controller.

Table 11. STM32F050x peripheral register boundary addresses (continued)

Bus	Boundary address	Size	Peripheral
APB	0x4000 7C00 - 0x4000 7FFF	1KB	Reserved
	0x4000 7800 - 0x4000 7BFF	1KB	Reserved
	0x4000 7400 - 0x4000 77FF	1KB	Reserved
	0x4000 7000 - 0x4000 73FF	1KB	PWR
	0x4000 5C00 - 0x4000 6FFF	5KB	Reserved
	0x4000 5800 - 0x4000 5BFF	1KB	Reserved
	0x4000 5400 - 0x4000 57FF	1KB	I2C1
	0x4000 4800 - 0x4000 53FF	3 KB	Reserved
	0x4000 4400 - 0x4000 47FF	1KB	Reserved
	0x4000 3C00 - 0x4000 43FF	2KB	Reserved
	0x4000 3800 - 0x4000 3BFF	1KB	Reserved
	0x4000 3400 - 0x4000 37FF	1KB	Reserved
	0x4000 3000 - 0x4000 33FF	1KB	IWDG
	0x4000 2C00 - 0x4000 2FFF	1KB	WWDG
	0x4000 2800 - 0x4000 2BFF	1KB	RTC
	0x4000 2400 - 0x4000 27FF	1KB	Reserved
	0x4000 2000 - 0x4000 23FF	1KB	TIM14
	0x4000 1400 - 0x4000 1FFF	3KB	Reserved
	0x4000 1000 - 0x4000 13FF	1KB	Reserved
	0x4000 0800 - 0x4000 0FFF	2KB	Reserved
	0x4000 0400 - 0x4000 07FF	1KB	TIM3
	0x4000 0000 - 0x4000 03FF	1KB	TIM2

Table 26. Typical current consumption in Sleep mode, code running from Flash or RAM

Symbol	Parameter	Conditions	f_{HCLK}	Typ		Unit
				Peripherals enabled	Peripherals disabled	
I_{DD}	Supply current in Sleep mode from V_{DD} supply	Running from HSE crystal clock 8 MHz, code executing from Flash or RAM	48 MHz	10.7	2.4	mA
			36 MHz	8.1	1.8	
			32 MHz	7.1	1.6	
			24 MHz	5.5	1.3	
			16 MHz	3.7	0.9	
			8 MHz	1.9	0.5	
			4 MHz	1.5	0.4	
			2 MHz	1.1	0.3	
			1 MHz	0.8	0.3	
			500 kHz	0.6	0.3	
			125 kHz	0.5	0.3	
I_{DDA}	Supply current in Sleep mode from V_{DDA} supply		48 MHz	140	140	µA
			36 MHz	109	109	
			32 MHz	96	96	
			24 MHz	76	76	
			16 MHz	51	51	
			8 MHz	1.7	1.7	
			4 MHz	1.6	1.6	
			2 MHz	1.5	1.5	
			1 MHz	1.1	1.1	
			500 kHz	1.1	1.1	
			125 kHz	1.1	1.1	

On-chip peripheral current consumption

The current consumption of the on-chip peripherals is given in *Table 28*. The MCU is placed under the following conditions:

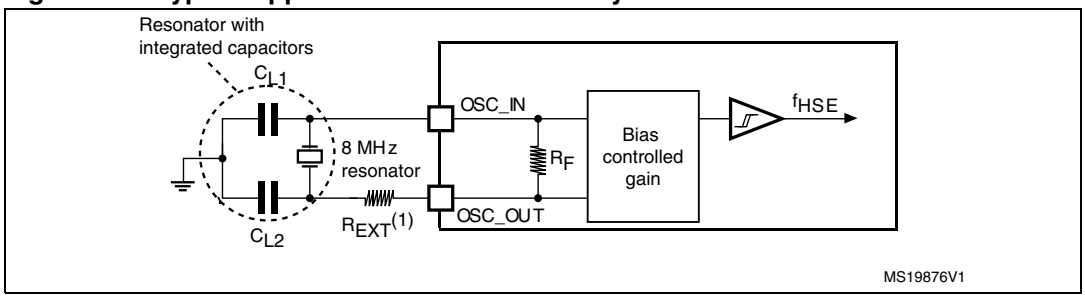
- all I/O pins are in input mode with a static value at V_{DD} or V_{SS} (no load)
- all peripherals are disabled unless otherwise mentioned
- the given value is calculated by measuring the current consumption
  - with all peripherals clocked off
  - with only one peripheral clocked on
- ambient operating temperature and V_{DD} supply voltage conditions summarized in *Table 12: Voltage characteristics*

Table 28. Peripheral current consumption

Peripheral	Typical consumption at 25 °C		Unit
	I_{DD}	I_{DDA}	
ADC(1)	0.53	0.964	mA
CRC	0.10	-	
DBGMCU	0.18	-	
DMA	0.35	-	
GPIOA	0.48	-	
GPIOB	0.58	-	
GPIOC	0.12	-	
GPIOF	0.06	-	
I2C1	0.43	-	
PWR	0.22	-	
SPI1/I2S1	0.63	-	
SYSCFG	0.28		
TIM1	1.01	-	
TIM2	1.00	-	
TIM3	0.78	-	
TIM6	0.32	-	
TIM14	0.45	-	
TIM16	0.57	-	
TIM17	0.59	-	
USART1	1.07	-	
WWDG	0.22	-	

1. ADC is in ready state after setting the ADEN bit in the ADC_CR register (ADRDY bit in ADC_ISR is high).

Figure 14. Typical application with an 8 MHz crystal



1. R_{EXT} value depends on the crystal characteristics.

Low-speed external clock generated from a crystal resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in *Table 32*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 32. LSE oscillator characteristics (f_{LSE} = 32.768 kHz)

Symbol	Parameter	Conditions(1)	Min(2)	Typ	Max(2)	Unit
I_{DD}	LSE current consumption	LSEDRV[1:0]=00 lower driving capability	-	0.5	0.9	µA
		LSEDRV[1:0]= 01 medium low driving capability	-	-	1	
		LSEDRV[1:0] = 10 medium high driving capability	-	-	1.3	
		LSEDRV[1:0]=11 higher driving capability	-	-	1.6	
g_m	Oscillator transconductance	LSEDRV[1:0]=00 lower driving capability	5	-	-	µA/V
		LSEDRV[1:0]= 01 medium low driving capability	8	-	-	
		LSEDRV[1:0] = 10 medium high driving capability	15	-	-	
		LSEDRV[1:0]=11 higher driving capability	25	-	-	
$t_{SU(LSE)}$(3)	Startup time	V_{DD} is stabilized	-	2	-	s

1. Refer to the note and caution paragraphs below the table, and to the application note AN2867 “Oscillator design guide for ST microcontrollers”.
2. Guaranteed by design, not tested in production.
3. $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal and it can vary significantly with the crystal manufacturer

Note: For information on selecting the crystal, refer to the application note AN2867 “Oscillator design guide for ST microcontrollers” available from the ST website www.st.com.

6.3.9 Memory characteristics

Flash memory

The characteristics are given at T_A = –40 to 105 °C unless otherwise specified.

Table 38. Flash memory characteristics

Symbol	Parameter	Conditions	Min	Typ	Max(1)	Unit
t_{prog}	16-bit programming time	T_A = –40 to +105 °C	40	53.5	60	µs
t_{ERASE}	Page (1 KB) erase time	T_A = –40 to +105 °C	20	-	40	ms
t_{ME}	Mass erase time	T_A = –40 to +105 °C	20	-	40	ms
I_{DD}	Supply current	Write mode	-	-	10	mA
		Erase mode	-	-	12	mA

1. Guaranteed by design, not tested in production.

Table 39. Flash memory endurance and data retention

Symbol	Parameter	Conditions	Value	Unit
			Min(1)	
N_{END}	Endurance	T_A = –40 to +85 °C (6 suffix versions) T_A = –40 to +105 °C (7 suffix versions)	10	kcycles
t_{RET}	Data retention	1 kcycle(2) at T_A = 85 °C	30	Years
		1 kcycle(2) at T_A = 105 °C	10	
		10 kcycles(2) at T_A = 55 °C	20	

1. Data based on characterization results, not tested in production.
2. Cycling performed over the whole temperature range.

6.3.10 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports). the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB**: A Burst of Fast Transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in *Table 40*. They are based on the EMS levels and classes defined in application note AN1709.

6.3.11 Electrical sensitivity characteristics

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the JESD22-A114/C101 standard.

Table 42. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Class	Maximum value(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C, conforming to JESD22-A114	2	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = +25 °C, conforming to JESD22-C101	II	500	

1. Data based on characterization results, not tested in production.

Static latch-up

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with EIA/JESD 78A IC latch-up standard.

Table 43. Electrical sensitivities

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	T_A = +105 °C conforming to JESD78A	II level A

6.3.12 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DD} (for standard, 3 V-capable I/O pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

Functional susceptibility to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (more than 5 LSB TUE), out of conventional limits of current injection on adjacent pins (more than –5 µA) or other functional failure (reset occurrence or oscillator frequency deviation, for example).

6.3.13 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in *Table 45* are derived from tests performed under the conditions summarized in *Table 15: General operating conditions*. All I/Os are CMOS and TTL compliant.

Table 45. I/O static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Low level input voltage	TC and TTa I/O	-	-	$0.3\ V_{DD}+0.07^{(1)}$	V
		FT and FTf I/O	-	-	$0.475\ V_{DD}-0.2^{(1)}$	
		BOOT0	-	-	$0.3\ V_{DD}-0.3^{(1)}$	
		All I/Os except BOOT0 pin	-	-	$0.3\ V_{DD}$	
V_{IH}	High level input voltage	TC and TTa I/O	$0.445\ V_{DD}+0.398^{(1)}$	-	-	V
		FT and FTf I/O	$0.5\ V_{DD}+0.2^{(1)}$	-	-	
		BOOT0	$0.2\ V_{DD}+0.95^{(1)}$	-	-	
		All I/Os except BOOT0 pin	$0.7\ V_{DD}$	-	-	
V_{hys}	Schmitt trigger hysteresis	TC and TTa I/O	-	$200^{(1)}$	-	mV
		FT and FTf I/O	-	$100^{(1)}$	-	
		BOOT0	-	$300^{(1)}$	-	
I_{lkg}	Input leakage current (2)	$V_{SS} \le V_{IN} \le V_{DD}$ I/O TC, FT and FTf	-	-	±0.1	µA
		$V_{SS} \le V_{IN} \le V_{DD}$ 2 V$\le V_{DD} \le V_{DDA} \le$3.6 V I/O TTa used in digital mode	-	-	±0.1	
		V_{IN}= 5 V I/O FT and FTf	-	-	10	
		V_{IN}= 3.6 V, 2 V$\le V_{DD} \le V_{IN}$ V_{DDA} = 3.6 V I/O TTa used in digital mode	-	-	1	
		$V_{SS} \le V_{IN} \le V_{DDA}$ 2 V$\le V_{DD} \le V_{DDA} \le$3.6 V I/O TTa used in analog mode	-	-	±0.2	
R_{PU}	Weak pull-up equivalent resistor(3)	$V_{IN} = V_{SS}$	25	40	55	kΩ

All I/Os are CMOS and TTL compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters. The coverage of these requirements is shown in *Figure 18* and *Figure 19* for standard I/Os, and in *Figure 20* and *Figure 21* for 5 V tolerant I/Os. The following curves are design simulation results, not tested in production.

Figure 18. TC and TTa I/O input characteristics - CMOS port

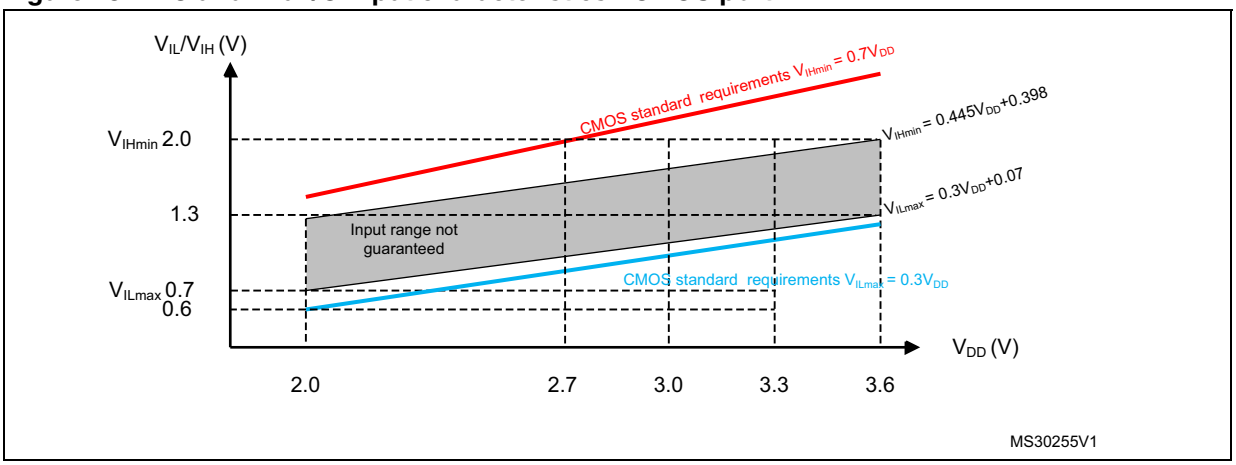
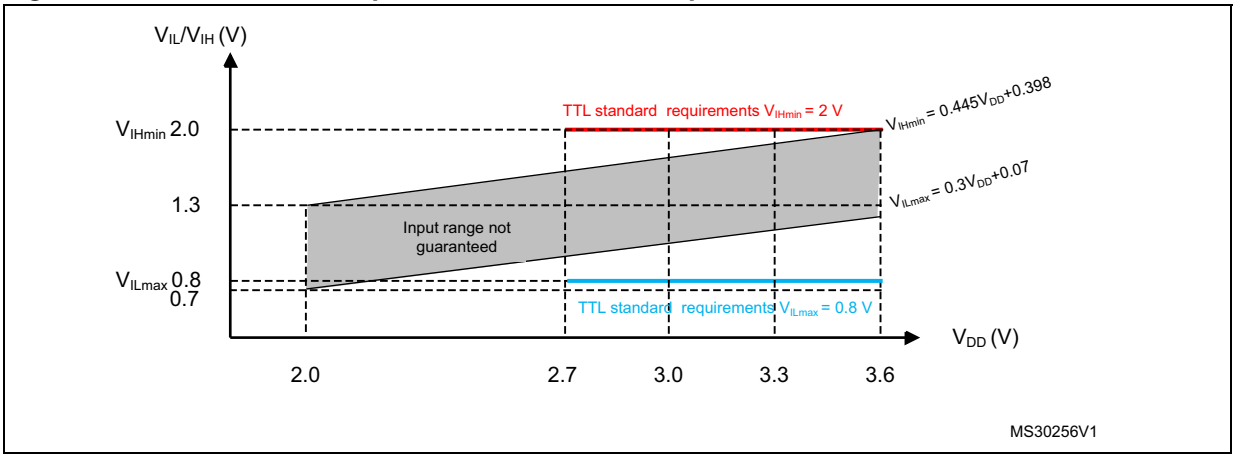


Figure 19. TC and TTa I/O input characteristics - TTL port



Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to +/-8 mA, and sink or source up to +/- 20 mA (with a relaxed V_{OL}/V_{OH}).

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in *Section 6.2*:

- The sum of the currents sourced by all the I/Os on $V_{DD,}$ plus the maximum Run consumption of the MCU sourced on $V_{DD,}$ cannot exceed the absolute maximum rating I_{VDD} (see *Table 13: Current characteristics*).
- The sum of the currents sunk by all the I/Os on V_{SS} plus the maximum Run consumption of the MCU sunk on V_{SS} cannot exceed the absolute maximum rating I_{VSS} (see *Table 13: Current characteristics*).

Output voltage levels

Unless otherwise specified, the parameters given in *Table 46* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 15: General operating conditions*. All I/Os are CMOS and TTL compliant (FT, TTa or TC unless otherwise specified).

Table 46. Output voltage characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}(1)	Output low level voltage for an I/O pin	CMOS port(2) I_{IO} = +8 mA 2.7 V < V_{DD} < 3.6 V	-	0.4	V
V_{OH}(3)	Output high level voltage for an I/O pin		V_{DD}–0.4	-	
V_{OL} (1)	Output low level voltage for an I/O pin	TTL port(2) I_{IO} =+ 8mA 2.7 V < V_{DD} < 3.6 V	-	0.4	V
V_{OH} (3)	Output high level voltage for an I/O pin		2.4	-	
V_{OL}(1)(4)	Output low level voltage for an I/O pin	I_{IO} = +20 mA 2.7 V < V_{DD} < 3.6 V	-	1.3	V
V_{OH}(3)(4)	Output high level voltage for an I/O pin		V_{DD}–1.3	-	
V_{OL}(1)(4)	Output low level voltage for an I/O pin	I_{IO} = +6 mA 2 V < V_{DD} < 2.7 V	-	0.4	V
V_{OH}(3)(4)	Output high level voltage for an I/O pin		V_{DD}–0.4	-	
V_{OLFM+}(1)	Output low level voltage for an FTf I/O pin in FM+ mode	I_{IO} = +20 mA 2.7 V < V_{DD} < 3.6 V	-	0.4	V

1. The I_{IO} current sunk by the device must always respect the absolute maximum rating specified in *Table 13: Current characteristics* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS}.
2. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.
3. The I_{IO} current sourced by the device must always respect the absolute maximum rating specified in *Table 13: Current characteristics* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VDD}.
4. Data based on design simulation only. Not tested in production.

2. ADC Accuracy vs. Negative Injection Current: Injecting negative current on any of the standard (non-robust) analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to standard analog pins which may potentially inject negative current.
Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 6.3.13* does not affect the ADC accuracy.
3. Better performance may be achieved in restricted V_{DDA}, frequency and temperature ranges.
4. Data based on characterization results, not tested in production.

Figure 24. ADC accuracy characteristics

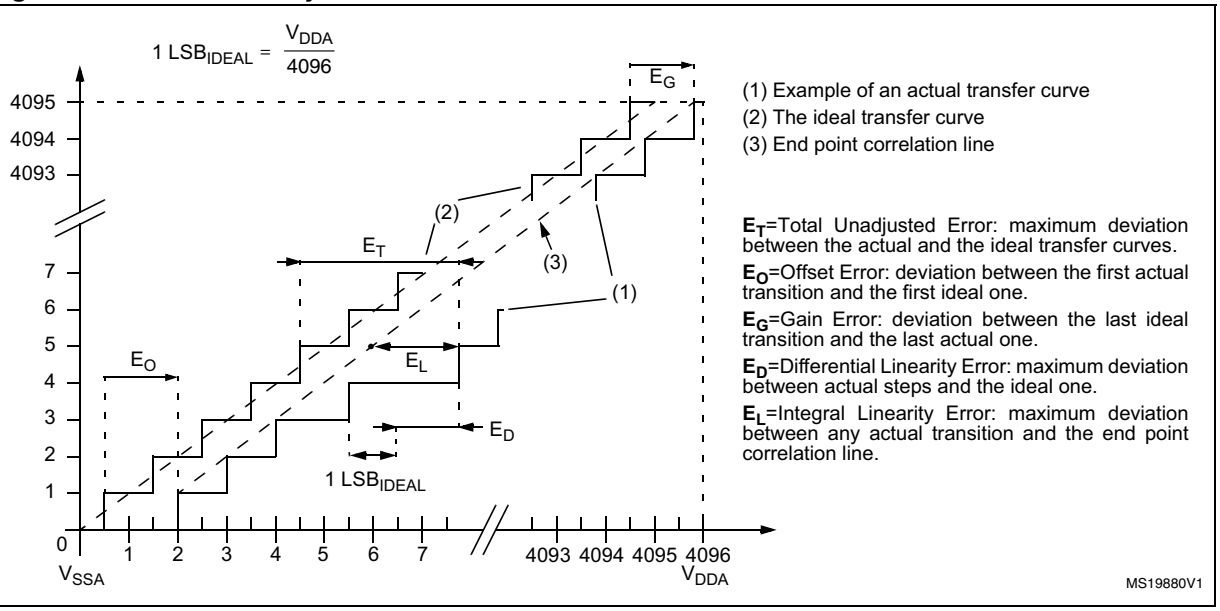
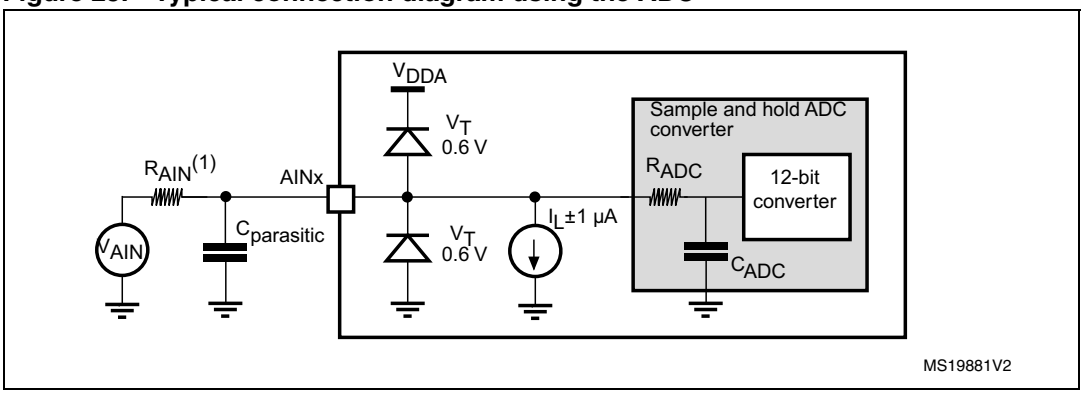


Figure 25. Typical connection diagram using the ADC



1. Refer to *Table 49: ADC characteristics* for the values of R_{AIN}, R_{ADC} and C_{ADC}.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7 pF). A high $C_{parasitic}$ value will downgrade conversion accuracy. To remedy this, f_{ADC} should be reduced.

General PCB design guidelines

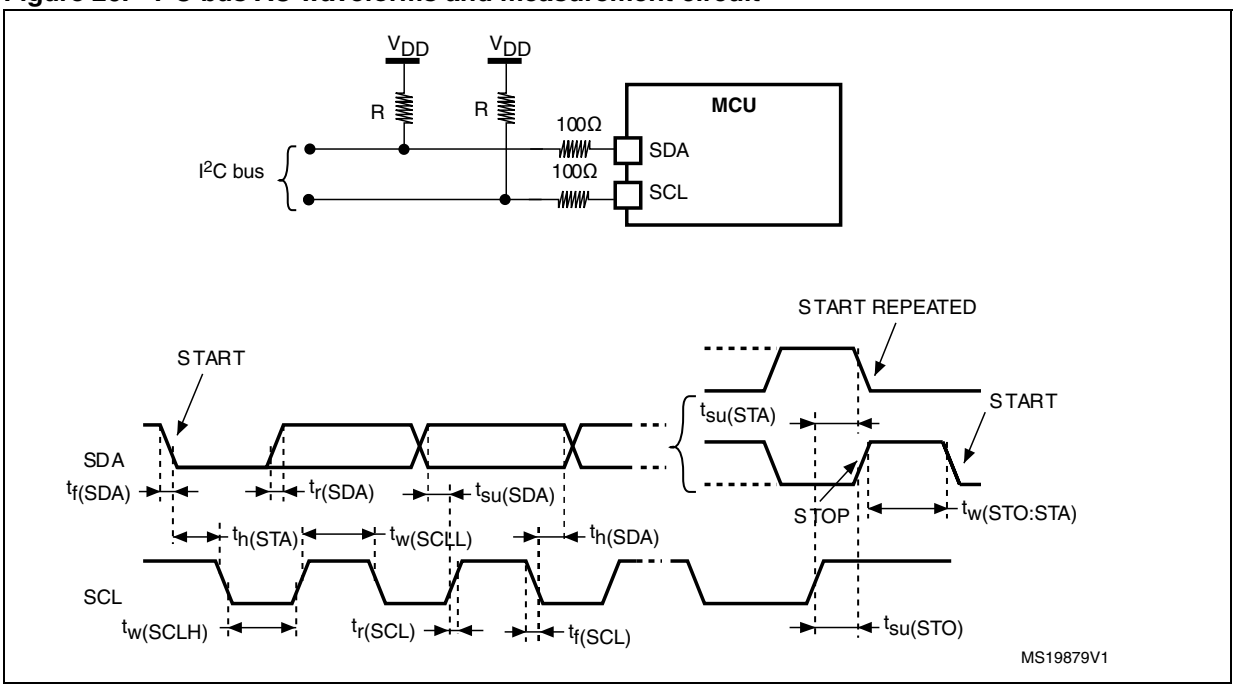
Power supply decoupling should be performed as shown in *Figure 10*. The 10 nF capacitor should be ceramic (good quality) and it should be placed as close as possible to the chip.

Table 58. I2C analog filter characteristics(1)

Symbol	Parameter	Min	Max	Unit
t_{SP}	Pulse width of spikes that are suppressed by the analog filter	50	260	ns

1. Guaranteed by design, not tested in production.

Figure 26. I^2C bus AC waveforms and measurement circuit



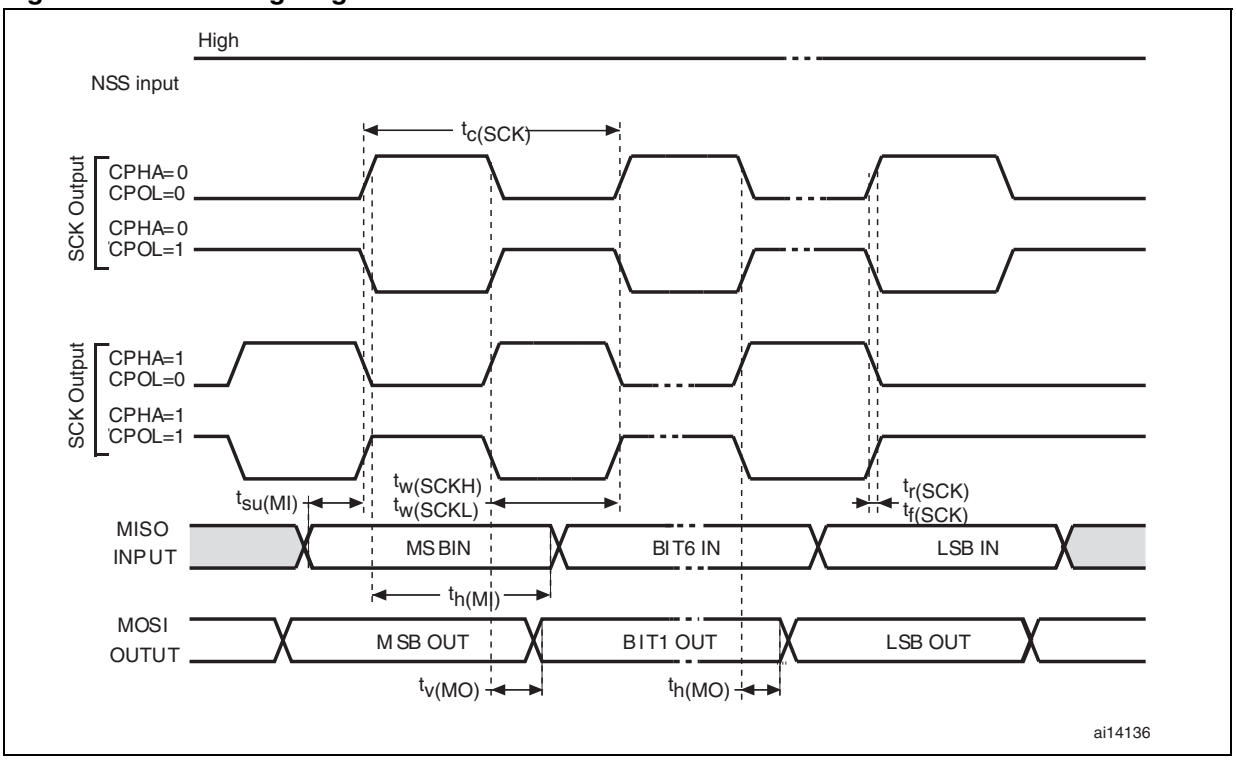
1. Measurement points are done at CMOS levels: 0.3 V_{DD} and 0.7 V_{DD}.

SPI/I^2S characteristics

Unless otherwise specified, the parameters given in *Table 59* for SPI or in *Table 60* for I^2S are derived from tests performed under ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in *Table 15: General operating conditions*.

Refer to *Section 6.3.13: I/O port characteristics* for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO for SPI and WS, CK, SD for I^2S).

Figure 29. SPI timing diagram - master mode(1)



1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

7.2 Thermal characteristics

The maximum chip junction temperature ($T_J$max) must never exceed the values given in *Table 15: General operating conditions on page 39*.

The maximum chip-junction temperature, T_J max, in degrees Celsius, may be calculated using the following equation:

$$T_J \text{ max} = T_A \text{ max} + (P_D \text{ max} \times \Theta_{JA})$$

Where:

- T_A max is the maximum ambient temperature in °C,
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W,
- P_D max is the sum of P_{INT} max and $P_{I/O}$ max (P_D max = P_{INT} max + $P_{I/O}$max),
- P_{INT} max is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.

$P_{I/O}$ max represents the maximum power dissipation on output pins where:

$$P_{I/O} \text{ max} = \Sigma (V_{OL} \times I_{OL}) + \Sigma((V_{DD} - V_{OH}) \times I_{OH}),$$

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Table 65. Package thermal characteristics

Symbol	Parameter	Value	Unit
Θ_{JA}	**Thermal resistance junction-ambient** LQFP48 - 7 × 7 mm	55	°C/W
	Thermal resistance junction-ambient UFQFPN32 - 5 × 5 mm	38	
	Thermal resistance junction-ambient UFQFPN28 - 4 × 4 mm	118	
	Thermal resistance junction-ambient TSSOP20	110	

7.2.1 Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org

7.2.2 Selecting the product temperature range

When ordering the microcontroller, the temperature range is specified in the ordering information scheme shown in *Section 8: Part numbering*.

Each temperature range suffix corresponds to a specific guaranteed ambient temperature at maximum dissipation and, to a specific maximum junction temperature.

As applications do not commonly use the STM32F05xx at maximum dissipation, it is useful to calculate the exact power consumption and junction temperature to determine which temperature range will be best suited to the application.

The following examples show how to calculate the temperature range needed for a given application.

8 Part numbering

For a list of available options (memory, package, and so on) or for further information on any aspect of this device, please contact your nearest ST sales office.

Example: STM32 F 050 C 6 T 6 A x

Device family

STM32 = ARM-based 32-bit microcontroller

Product type

F = General-purpose

Sub-family

050 = STM32F050xx

Pin count

F = 20 pins
G = 28 pins
K = 32 pins
C = 48 pins

Code size

4 = 16 Kbytes of Flash memory
6 = 32 Kbytes of Flash memory

Package

P = TSSOP
U = UFQFPN
T = LQFP

Temperature range

6 = –40 °C to +85 °C
7 = –40 °C to +105 °C

Internal code

A = non-optimized die
Blank = standard die

Options

xxx = programmed parts
TR = tape and real