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Understanding Embedded - FPGAs (Field Programmable Gate Array)

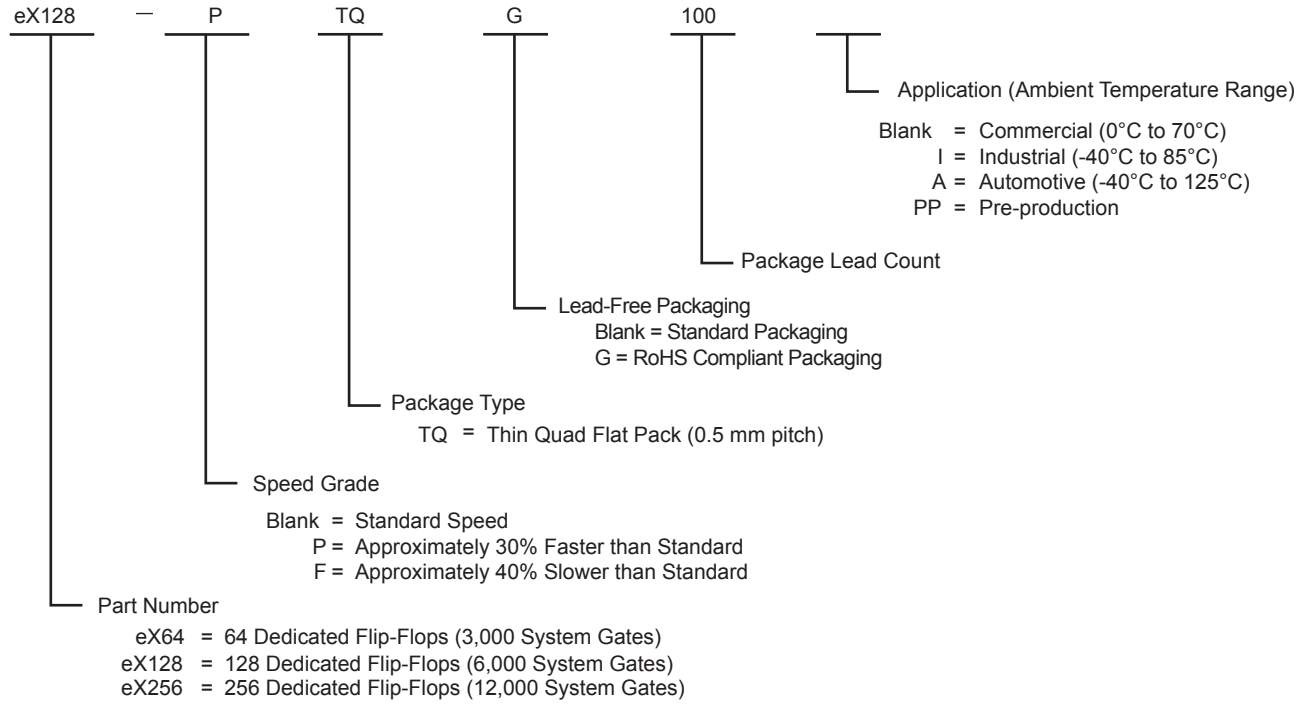
Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	256
Total RAM Bits	-
Number of I/O	46
Number of Gates	6000
Voltage - Supply	2.3V ~ 2.7V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	64-LQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/ex128-ftq64

Ordering Information



eX Device Status

eX Devices	Status
eX64	Production
eX128	Production
eX256	Production

Plastic Device Resources

Device	User I/Os (Including Clock Buffers)	
	TQ64	TQ100
eX64	41	56
eX128	46	70
eX256	—	81

Note: TQ = Thin Quad Flat Pack

1 – eX FPGA Architecture and Characteristics

General Description

The eX family of FPGAs is a low-cost solution for low-power, high-performance designs. The inherent low power attributes of the antifuse technology, coupled with an additional low static power mode, make these devices ideal for power-sensitive applications. Fabricated with an advanced 0.22 mm CMOS antifuse technology, these devices achieve high performance with no power penalty.

eX Family Architecture

Microsemi eX family is implemented on a high-voltage twin-well CMOS process using 0.22 µm design rules. The eX family architecture uses a “sea-of-modules” structure where the entire floor of the device is covered with a grid of logic modules with virtually no chip area lost to interconnect elements or routing. Interconnection among these logic modules is achieved using Microsemi patented metal-to-metal programmable antifuse interconnect elements. The antifuse interconnect is made up of a combination of amorphous silicon and dielectric material with barrier metals and has an "on" state resistance of 25Ω with a capacitance of 1.0fF for low-signal impedance. The antifuses are normally open circuit and, when programmed, form a permanent low-impedance connection. The eX family provides two types of logic modules, the register cell (R-cell) and the combinatorial cell (C-cell).

The R-cell contains a flip-flop featuring asynchronous clear, asynchronous preset, and clock enable (using the S0 and S1 lines) control signals (Figure 1-1). The R-cell registers feature programmable clock polarity selectable on a register-by-register basis. This provides additional flexibility while allowing mapping of synthesized functions into the eX FPGA. The clock source for the R-cell can be chosen from either the hard-wired clock or the routed clock.

The C-cell implements a range of combinatorial functions up to five inputs (Figure 1-2 on page 1-2). Inclusion of the DB input and its associated inverter function enables the implementation of more than 4,000 combinatorial functions in the eX architecture in a single module.

Two C-cells can be combined together to create a flip-flop to imitate an R-cell via the use of the CC macro. This is particularly useful when implementing non-timing-critical paths and when the design engineer is running out of R-cells. More information about the CC macro can be found in the *Maximizing Logic Utilization in eX, SX and SX-A FPGA Devices Using CC Macros* application note.

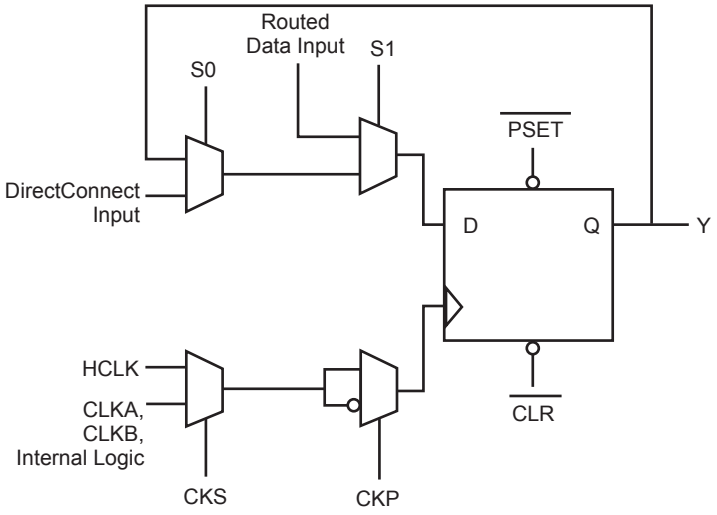


Figure 1-1 • **R-Cell**

Routing Resources

Clusters and SuperClusters can be connected through the use of two innovative local routing resources called FastConnect and DirectConnect, which enable extremely fast and predictable interconnection of modules within Clusters and SuperClusters (Figure 1-4). This routing architecture also dramatically reduces the number of antifuses required to complete a circuit, ensuring the highest possible performance.

DirectConnect is a horizontal routing resource that provides connections from a C-cell to its neighboring R-cell in a given SuperCluster. DirectConnect uses a hard-wired signal path requiring no programmable interconnection to achieve its fast signal propagation time of less than 0.1 ns (–P speed grade).

FastConnect enables horizontal routing between any two logic modules within a given SuperCluster and vertical routing with the SuperCluster immediately below it. Only one programmable connection is used in a FastConnect path, delivering maximum pin-to-pin propagation of 0.3 ns (–P speed grade).

In addition to DirectConnect and FastConnect, the architecture makes use of two globally oriented routing resources known as segmented routing and high-drive routing. The segmented routing structure of Microsemi provides a variety of track lengths for extremely fast routing between SuperClusters. The exact combination of track lengths and antifuses within each path is chosen by the fully automatic place-and-route software to minimize signal propagation delays.

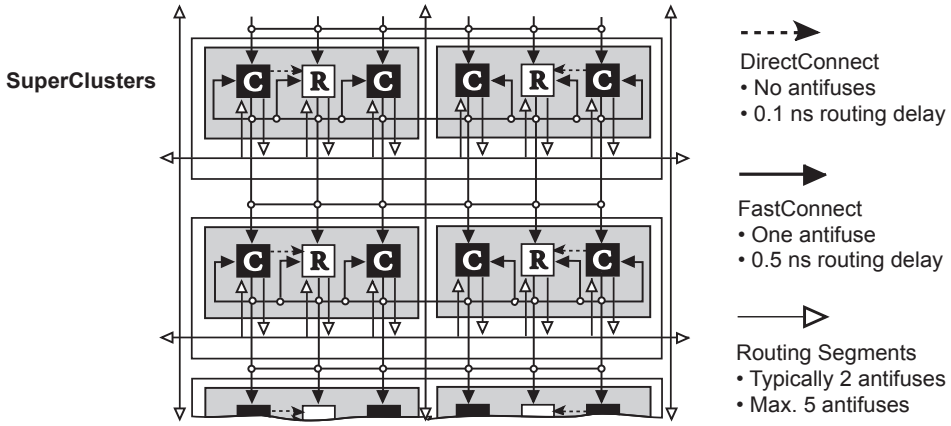


Figure 1-4 • **DirectConnect and FastConnect for SuperClusters**

Clock Resources

eX's high-drive routing structure provides three clock networks. The first clock, called HCLK, is hardwired from the HCLK buffer to the clock select MUX in each R-Cell. HCLK cannot be connected to combinational logic. This provides a fast propagation path for the clock signal, enabling the 3.9 ns clock-to-out (pad-to-pad) performance of the eX devices. The hard-wired clock is tuned to provide a clock skew of less than 0.1 ns worst case. If not used, the HCLK pin must be tied LOW or HIGH and must not be left floating. Figure 1-5 describes the clock circuit used for the constant load HCLK.

HCLK does not function until the fourth clock cycle each time the device is powered up to prevent false output levels due to any possible slow power-on-reset signal and fast start-up clock circuit. To activate HCLK from the first cycle, the TRST pin must be reserved in the Design software and the pin must be tied to GND on the board. (See the "TRST, I/O Boundary Scan Reset Pin" on page 1-32).

The remaining two clocks (CLKA, CLKB) are global routed clock networks that can be sourced from external pins or from internal logic signals (via the CLKINT routed clock buffer) within the eX device. CLKA and CLKB may be connected to sequential cells or to combinational logic. If CLKA or CLKB is sourced from internal logic signals, the external clock pin cannot be used for any other input and must be tied LOW or HIGH and must not float. Figure 1-6 describes the CLKA and CLKB circuit used in eX devices.

Table 1-1 describes the possible connections of the routed clock networks, CLKA and CLKB. Unused clock pins must not be left floating and must be tied to HIGH or LOW.

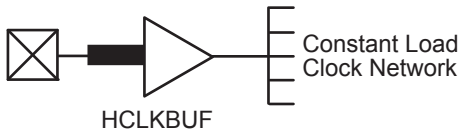


Figure 1-5 • **eX HCLK Clock Pad**

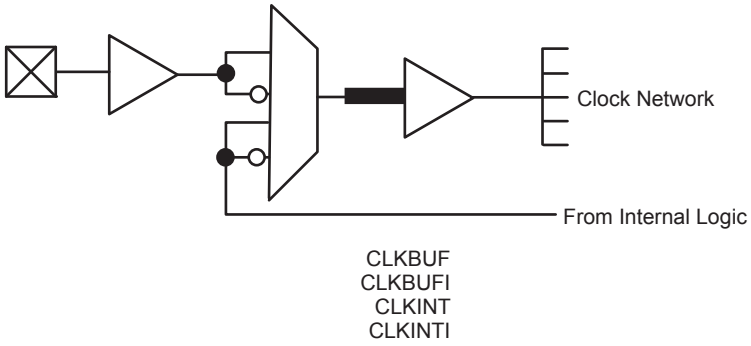


Figure 1-6 • **eX Routed Clock Buffer**

Table 1-1 • **Connections of Routed Clock Networks, CLKA and CLKB**

Module	Pins
C-Cell	A0, A1, B0 and B1
R-Cell	CLKA, CLKB, S0, S1, PSET, and CLR
I/O-Cell	EN

Other Architectural Features

Performance

The combination of architectural features described above enables eX devices to operate with internal clock frequencies exceeding 350 MHz for very fast execution of complex logic functions. The eX family is an optimal platform upon which the functionality previously contained in CPLDs can be integrated. eX devices meet the performance goals of gate arrays, and at the same time, present significant improvements in cost and time to market. Using timing-driven place-and-route tools, designers can achieve highly deterministic device performance.

User Security

Microsemi FuseLock advantage provides the highest level of protection in the FPGA industry against unauthorized modifications. In addition to the inherent strengths of the architecture, special security fuses that are intended to prevent internal probing and overwriting are hidden throughout the fabric of the device. They are located such that they cannot be accessed or bypassed without destroying the rest of the device, making Microsemi antifuse FPGAs highly resistant to both invasive and more subtle noninvasive attacks.

Look for this symbol to ensure your valuable IP is secure. The FuseLock Symbol on the FPGA ensures that the device is safeguarded to cryptographic attacks.

Figure 1-7 • **Fuselock**

For more information, refer to *Implementation of Security in Microsemi Antifuse FPGAs* application note.

I/O Modules

Each I/O on an eX device can be configured as an input, an output, a tristate output, or a bidirectional pin. Even without the inclusion of dedicated I/O registers, these I/Os, in combination with array registers, can achieve clock-to-out (pad-to-pad) timing as fast as 3.9 ns. I/O cells in eX devices do not contain embedded latches or flip-flops and can be inferred directly from HDL code. The device can easily interface with any other device in the system, which in turn enables parallel design of system components and reduces overall design time.

All unused I/Os are configured as tristate outputs by Microsemi's Designer software, for maximum flexibility when designing new boards or migrating existing designs. Each I/O module has an available pull-up or pull-down resistor of approximately 50 kΩ that can configure the I/O in a known state during power-up. Just shortly before V_{CCA} reaches 2.5 V, the resistors are disabled and the I/Os will be controlled by user logic.

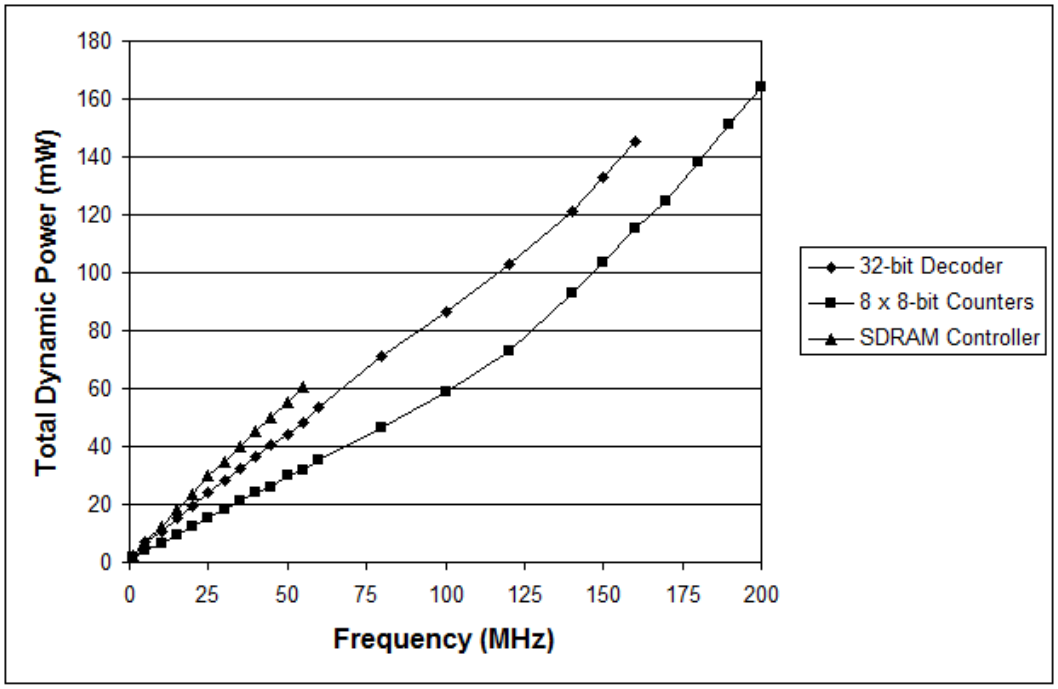


Figure 1-10 • **Total Dynamic Power (mW)**

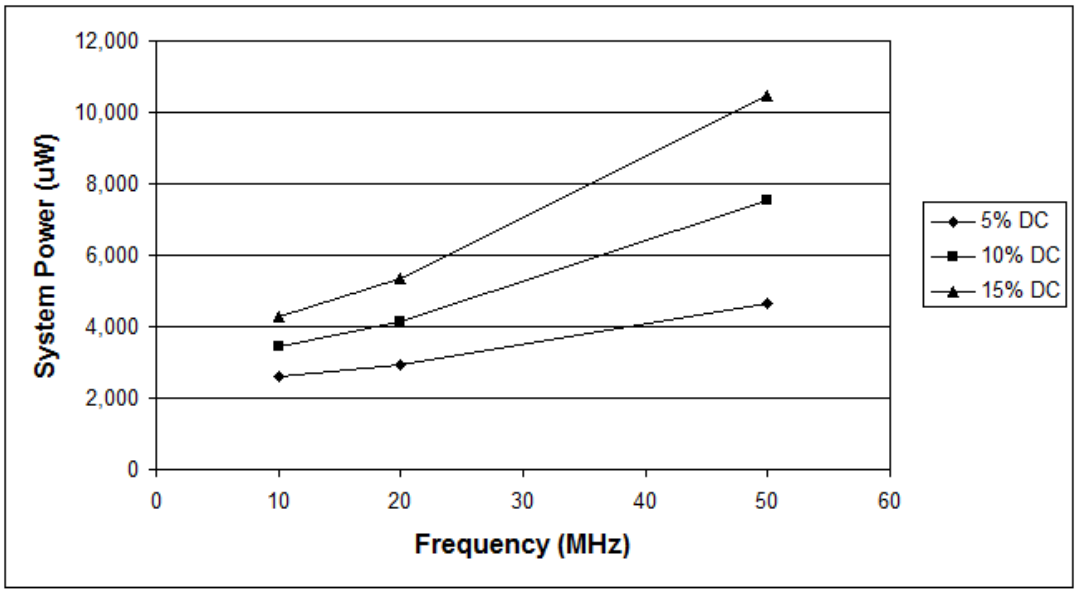


Figure 1-11 • **System Power at 5%, 10%, and 15% Duty Cycle**

Design Considerations

The TDI, TCK, TDO, PRA, and PRB pins should not be used as input or bidirectional ports. Since these pins are active during probing, critical signals input through these pins are not available while probing. In addition, the Security Fuse should not be programmed because doing so disables the probe circuitry. It is recommended to use a series 70Ω termination resistor on every probe connector (TDI, TCK, TMS, TDO, PRA, PRB). The 70Ω series termination is used to prevent data transmission corruption during probing and reading back the checksum.

Table 1-8 • **Device Configuration Options for Probe Capability (TRST pin reserved)**

JTAG Mode	TRST[1]	Security Fuse Programmed	PRA, PRB[2]	TDI, TCK, TDO[2]
Dedicated	LOW	No	User I/O[3]	Probing Unavailable
Flexible	LOW	No	User I/O[3]	User I/O[3]
Dedicated	HIGH	No	Probe Circuit Outputs	Probe Circuit Inputs
Flexible	HIGH	No	Probe Circuit Outputs	Probe Circuit Inputs
–	–	Yes	Probe Circuit Secured	Probe Circuit Secured

Notes:

1. *If TRST pin is not reserved, the device behaves according to TRST = HIGH in the table.*
2. *Avoid using the TDI, TCK, TDO, PRA, and PRB pins as input or bidirectional ports. Since these pins are active during probing, input signals will not pass through these pins and may cause contention.*
3. *If no user signal is assigned to these pins, they will behave as unused I/Os in this mode. Unused pins are automatically tristated by Microsemi Designer software.*

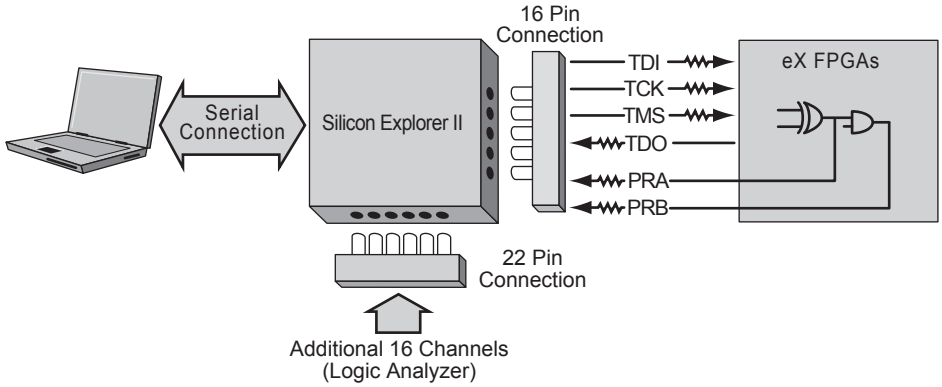


Figure 1-13 • **Silicon Explorer II Probe Setup**

Development Tool Support

The eX family of FPGAs is fully supported by both Libero® Integrated Design Environment and Designer FPGA Development software. Libero IDE is a design management environment that streamlines the design flow. Libero IDE provides an integrated design manager that seamlessly integrates design tools while guiding the user through the design flow, managing all design and log files, and passing necessary design data among tools. Additionally, Libero IDE allows users to integrate both schematic and HDL synthesis into a single flow and verify the entire design in a single environment. Libero IDE includes Synplify® for Microsemi from Synplicity®, ViewDraw for Microsemi from Mentor Graphics, ModelSim® HDL Simulator from Mentor Graphics®, WaveFormer Lite™ from SynaptiCAD™, and Designer software from Microsemi. Refer to the *Libero IDE flow* (located on Microsemi SoC Product Group's website) diagram for more information.

Designer software is a place-and-route tool and provides a comprehensive suite of backend support tools for FPGA development. The Designer software includes timing-driven place-and-route, and a world-class integrated static timing analyzer and constraints editor. With the Designer software, a user can lock his/her design pins before layout while minimally impacting the results of place-and-route. Additionally, the back-annotation flow is compatible with all the major simulators and the simulation results can be cross-probed with Silicon Explorer II, Microsemi integrated verification and logic analysis tool. Another tool included in the Designer software is the SmartGen core generator, which easily creates popular and commonly used logic functions for implementation into your schematic or HDL design. Microsemi's Designer software is compatible with the most popular FPGA design entry and verification tools from companies such as Mentor Graphics, Synplicity, Synopsys, and Cadence Design Systems. The Designer software is available for both the Windows and UNIX operating systems.

The estimation of the dynamic power dissipation is a piece-wise linear summation of the power dissipation of each component.

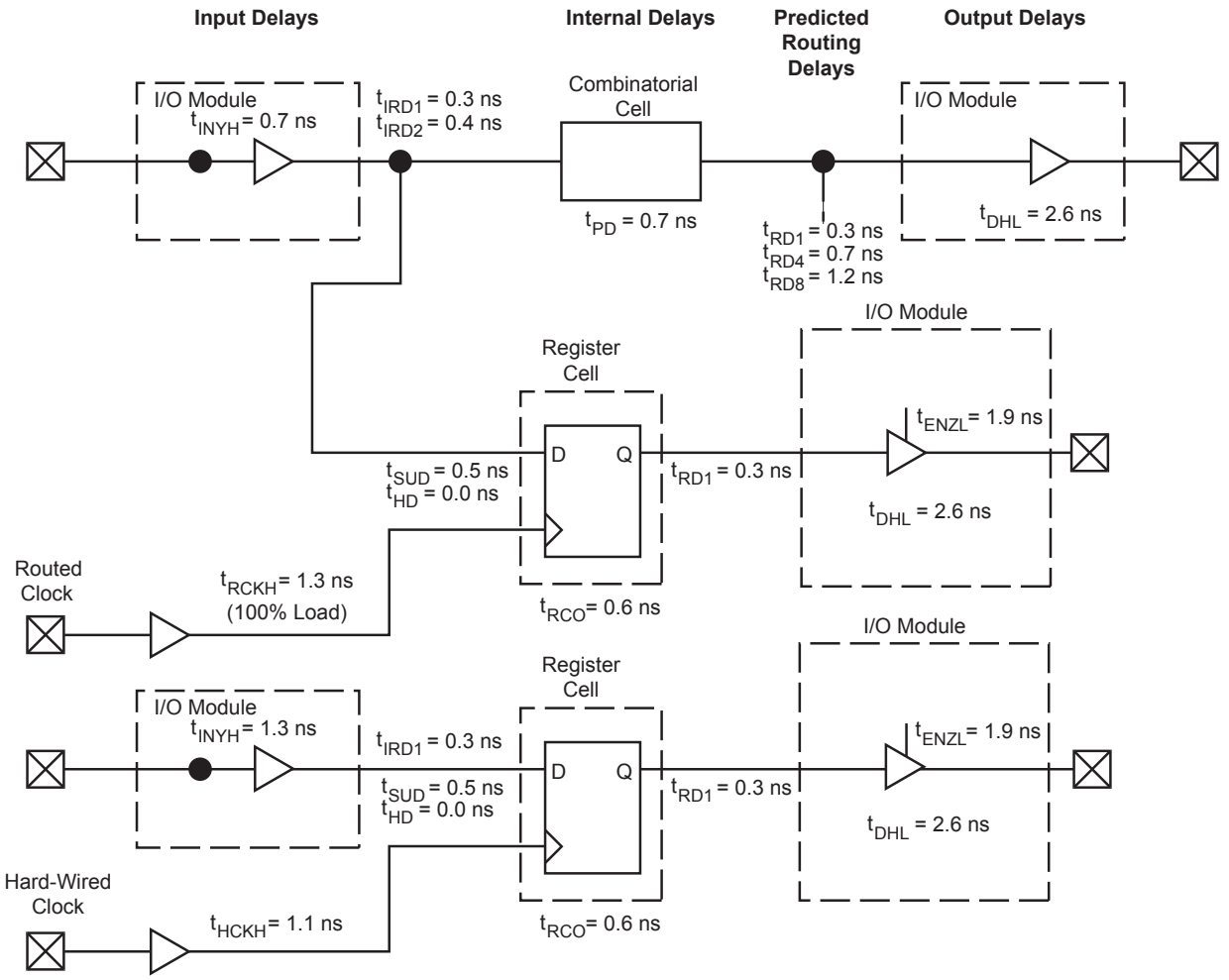
$$\text{Dynamic power dissipation} = VCCA^2 * [(m_c * C_{eqcm} * fm_C)_{\text{Comb Modules}} + (m_s * C_{eqsm} * fm_S)_{\text{Seq Modules}} + (n * C_{eqi} * fn)_{\text{Input Buffers}} + (0.5 * (q1 * C_{eqcr} * fq1) + (r1 * fq1))_{RCLKA} + (0.5 * (q2 * C_{eqcr} * fq2) + (r2 * fq2))_{RCLKB} + (0.5 * (s1 * C_{eqhv} * fs1)+(C_{eqhf} * fs1))_{HCLK}] + V_{CCI}^2 * [(p * (C_{eqo} + C_L) * fp)_{\text{Output Buffers}}]$$

where:

m_c = Number of combinatorial cells switching at frequency fm, typically 20% of C-cells
m_s = Number of sequential cells switching at frequency fm, typically 20% of R-cells
n = Number of input buffers switching at frequency fn, typically number of inputs / 4
p = Number of output buffers switching at frequency fp, typically number of outputs / 4
q1 = Number of R-cells driven by routed array clock A
q2 = Number of R-cells driven by routed array clock B
r1 = Fixed capacitance due to routed array clock A
r2 = Fixed capacitance due to routed array clock B
s1 = Number of R-cells driven by dedicated array clock
C_{eqcm} = Equivalent capacitance of combinatorial modules
C_{eqsm} = Equivalent capacitance of sequential modules
C_{eqi} = Equivalent capacitance of input buffers
C_{eqcr} = Equivalent capacitance of routed array clocks
C_{eqhv} = Variable capacitance of dedicated array clock
C_{eqhf} = Fixed capacitance of dedicated array clock
C_{eqo} = Equivalent capacitance of output buffers
C_L = Average output loading capacitance, typically 10 pF
fm_c = Average C-cell switching frequency, typically F/10
fm_s = Average R-cell switching frequency, typically F/10
fn = Average input buffer switching frequency, typically F/5
fp = Average output buffer switching frequency, typically F/5
fq1 = Frequency of routed clock A
fq2 = Frequency of routed clock B
fs1 = Frequency of dedicated array clock

The eX, SX-A and RTSX-S Power Calculator can be used to estimate the total power dissipation (static and dynamic) of eX devices: www.microsemi.com/soc/techdocs/calculators.aspx.

eX Timing Model



Note: Values shown for eX128–P, worst-case commercial conditions (5.0 V, 35 pF Pad Load).

Figure 1-14 • **eX Timing Model**

Hardwired Clock

External Setup = $t_{INYH} + t_{IRD1} + t_{SUD} – t_{HCKH}$

= 0.7 + 0.3 + 0.5 – 1.1 = 0.4 ns

Clock-to-Out (Pad-to-Pad), typical

= $t_{HCKH} + t_{RCO} + t_{RD1} + t_{DHL}$

= 1.1 + 0.6 + 0.3 + 2.6 = 4.6 ns

Routed Clock

External Setup = $t_{INYH} + t_{IRD2} + t_{SUD} – t_{RCKH}$

= 0.7 + 0.4 + 0.5 – 1.3= 0.3 ns

Clock-to-Out (Pad-to-Pad), typical

= $t_{RCKH} + t_{RCO} + t_{RD1} + t_{DHL}$

= 1.3+ 0.6 + 0.3 + 2.6 = 4.8 ns

Table 1-19 • eX Family Timing Characteristics
(Worst-Case Commercial Conditions VCCA = 2.3V, VCCI = 2.3 V or 3.0V, T_J = 70°C)

		'–P' Speed		'Std' Speed		'–F' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Dedicated (Hard-Wired) Array Clock Networks								
t_{HCKH}	Input LOW to HIGH (Pad to R-Cell Input)		1.1		1.6		2.3	ns
t_{HCKL}	Input HIGH to LOW (Pad to R-Cell Input)		1.1		1.6		2.3	ns
t_{HPWH}	Minimum Pulse Width HIGH	1.4		2.0		2.8		ns
t_{HPWL}	Minimum Pulse Width LOW	1.4		2.0		2.8		ns
t_{HCKSW}	Maximum Skew		<0.1		<0.1		<0.1	ns
t_{HP}	Minimum Period	2.8		4.0		5.6		ns
f_{HMAX}	Maximum Frequency		357		250		178	MHz
Routed Array Clock Networks								
t_{RCKH}	Input LOW to HIGH (Light Load) (Pad to R-Cell Input) MAX.		1.0		1.4		2.0	ns
t_{RCKL}	Input HIGH to LOW (Light Load) (Pad to R-Cell Input) MAX.		1.0		1.4		2.0	ns
t_{RCKH}	Input LOW to HIGH (50% Load) (Pad to R-Cell Input) MAX.		1.2		1.7		2.4	ns
t_{RCKL}	Input HIGH to LOW (50% Load) (Pad to R-Cell Input) MAX.		1.2		1.7		2.4	ns
t_{RCKH}	Input LOW to HIGH (100% Load) (Pad to R-Cell Input) MAX.		1.4		2.0		2.8	ns
t_{RCKL}	Input HIGH to LOW (100% Load) (Pad to R-Cell Input) MAX.		1.4		2.0		2.8	ns
t_{RPWH}	Min. Pulse Width HIGH	1.4		2.0		2.8		ns
t_{RPWL}	Min. Pulse Width LOW	1.4		2.0		2.8		ns
t_{RCKSW}*	Maximum Skew (Light Load)		0.2		0.3		0.4	ns
t_{RCKSW}*	Maximum Skew (50% Load)		0.2		0.2		0.3	ns
t_{RCKSW}*	Maximum Skew (100% Load)		0.1		0.1		0.2	ns

*Note: *Clock skew improves as the clock network becomes more heavily loaded.*

Table 1-20 • **eX Family Timing Characteristics**
(Worst-Case Commercial Conditions VCCA = 2.3 V, T_J = 70°C)

		–P Speed		Std Speed		–F Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
2.5 V LVCMOS Output Module Timing[1] (VCCI = 2.3 V)								
t_{DLH}	Data-to-Pad LOW to HIGH		3.3		4.7		6.6	ns
t_{DHL}	Data-to-Pad HIGH to LOW		3.5		5.0		7.0	ns
t_{DHLS}	Data-to-Pad HIGH to LOW—Low Slew		11.6		16.6		23.2	ns
t_{ENZL}	Enable-to-Pad, Z to L		2.5		3.6		5.1	ns
t_{ENZLS}	Enable-to-Pad Z to L—Low Slew		11.8		16.9		23.7	ns
t_{ENZH}	Enable-to-Pad, Z to H		3.4		4.9		6.9	ns
t_{ENLZ}	Enable-to-Pad, L to Z		2.1		3.0		4.2	ns
t_{ENHZ}	Enable-to-Pad, H to Z		2.4		5.67		7.94	ns
d_{TLH}	Delta Delay vs. Load LOW to HIGH		0.034		0.046		0.066	ns/pF
d_{THL}	Delta Delay vs. Load HIGH to LOW		0.016		0.022		0.05	ns/pF
d_{THLS}	Delta Delay vs. Load HIGH to LOW—Low Slew		0.05		0.072		0.1	ns/pF
3.3 V LVTTL Output Module Timing[1] (VCCI = 3.0 V)								
t_{DLH}	Data-to-Pad LOW to HIGH		2.8		4.0		5.6	ns
t_{DHL}	Data-to-Pad HIGH to LOW		2.7		3.9		5.4	ns
t_{DHLS}	Data-to-Pad HIGH to LOW—Low Slew		9.7		13.9		19.5	ns
t_{ENZL}	Enable-to-Pad, Z to L		2.2		3.2		4.4	ns
t_{ENZLS}	Enable-to-Pad Z to L—Low Slew		9.7		13.9		19.6	ns
t_{ENZH}	Enable-to-Pad, Z to H		2.8		4.0		5.6	ns
t_{ENLZ}	Enable-to-Pad, L to Z		2.8		4.0		5.6	ns
t_{ENHZ}	Enable-to-Pad, H to Z		2.6		3.8		5.3	ns
d_{TLH}	Delta Delay vs. Load LOW to HIGH		0.02		0.03		0.046	ns/pF
d_{THL}	Delta Delay vs. Load HIGH to LOW		0.016		0.022		0.05	ns/pF
d_{THLS}	Delta Delay vs. Load HIGH to LOW—Low Slew		0.05		0.072		0.1	ns/pF
5.0 V TTL Output Module Timing* (VCCI = 4.75 V)								
t_{DLH}	Data-to-Pad LOW to HIGH		2.0		2.9		4.0	ns
t_{DHL}	Data-to-Pad HIGH to LOW		2.6		3.7		5.2	ns
t_{DHLS}	Data-to-Pad HIGH to LOW—Low Slew		6.8		9.7		13.6	ns
t_{ENZL}	Enable-to-Pad, Z to L		1.9		2.7		3.8	ns
t_{ENZLS}	Enable-to-Pad Z to L—Low Slew		6.8		9.8		13.7	ns
t_{ENZH}	Enable-to-Pad, Z to H		2.1		3.0		4.1	ns
t_{ENLZ}	Enable-to-Pad, L to Z		3.3		4.8		6.6	ns

*Note: *Delays based on 35 pF loading.*

Pin Description

CLKA/B **Routed Clock A and B**

These pins are clock inputs for clock distribution networks. Input levels are compatible with standard TTL or LVTTL specifications. The clock input is buffered prior to clocking the R-cells. If not used, this pin must be set LOW or HIGH on the board. It must not be left floating.

GND **Ground**

LOW supply voltage.

HCLK **Dedicated (Hardwired) Array Clock**

This pin is the clock input for sequential modules. Input levels are compatible with standard TTL or LVTTL specifications. This input is directly wired to each R-cell and offers clock speeds independent of the number of R-cells being driven. If not used, this pin must be set LOW or HIGH on the board. It must not be left floating.

I/O **Input/Output**

The I/O pin functions as an input, output, tristate, or bidirectional buffer. Based on certain configurations, input and output levels are compatible with standard TTL or LVTTL specifications. Unused I/O pins are automatically tristated by the Designer software.

LP **Low Power Pin**

Controls the low power mode of the eX devices. The device is placed in the low power mode by connecting the LP pin to logic HIGH. In low power mode, all I/Os are tristated, all input buffers are turned OFF, and the core of the device is turned OFF. To exit the low power mode, the LP pin must be set LOW. The device enters the low power mode 800 ns after the LP pin is driven to a logic HIGH. It will resume normal operation 200 µs after the LP pin is driven to a logic LOW. LP pin should not be left floating. Under normal operating condition it should be tied to GND via 10 kΩ resistor.

NC **No Connection**

This pin is not connected to circuitry within the device. These pins can be driven to any voltage or can be left floating with no effect on the operation of the device.

PRA/PRB, I/O **Probe A/B**

The Probe pin is used to output data from any user-defined design node within the device. This diagnostic pin can be used independently or in conjunction with the other probe pin to allow real-time diagnostic output of any signal path within the device. The Probe pin can be used as a user-defined I/O when verification has been completed. The pin's probe capabilities can be permanently disabled to protect programmed design confidentiality.

TCK, I/O **Test Clock**

Test clock input for diagnostic probe and device programming. In flexible mode, TCK becomes active when the TMS pin is set LOW (refer to Table 1-4 on page 1-10). This pin functions as an I/O when the boundary scan state machine reaches the "logic reset" state.

TDI, I/O **Test Data Input**

Serial input for boundary scan testing and diagnostic probe. In flexible mode, TDI is active when the TMS pin is set LOW (refer to Table 1-4 on page 1-10). This pin functions as an I/O when the boundary scan state machine reaches the "logic reset" state.

TDO, I/O **Test Data Output**

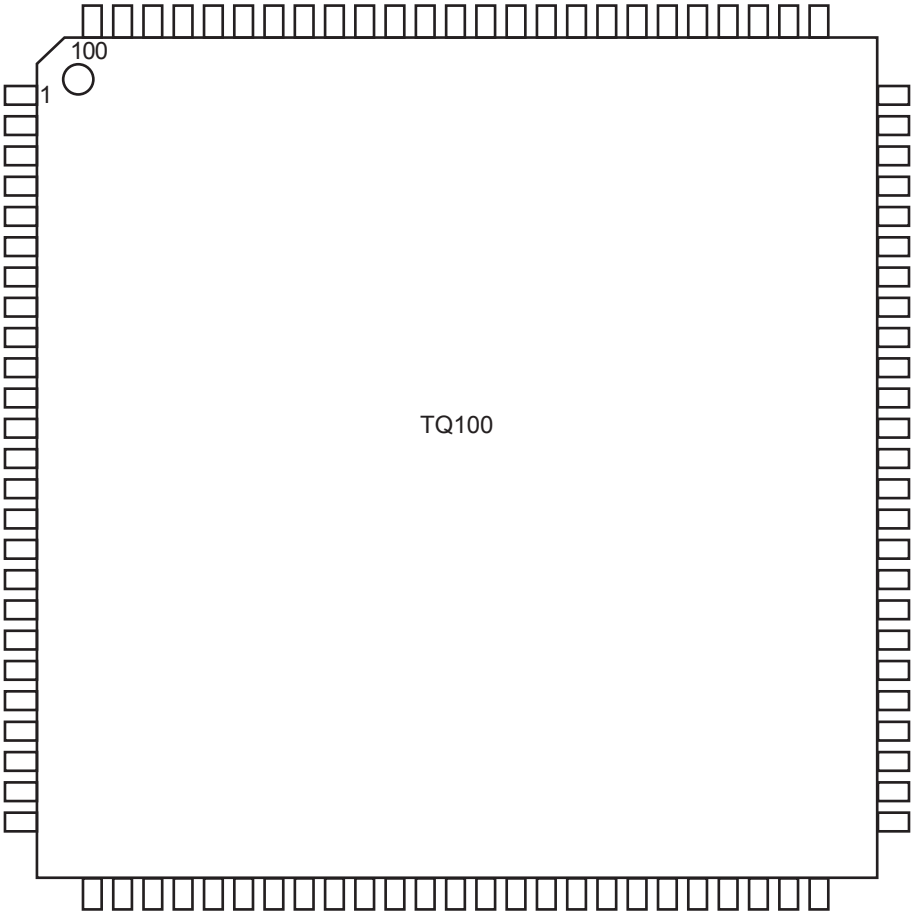
Serial output for boundary scan testing. In flexible mode, TDO is active when the TMS pin is set LOW (refer to Table 1-4 on page 1-10). This pin functions as an I/O when the boundary scan state machine reaches the "logic reset" state. When Silicon Explorer is being used, TDO will act as an output when the "checksum" command is run. It will return to user I/O when "checksum" is complete.

TQ64		
Pin Number	eX64 Function	eX128 Function
1	GND	GND
2	TDI, I/O	TDI, I/O
3	I/O	I/O
4	TMS	TMS
5	GND	GND
6	VCCI	VCCI
7	I/O	I/O
8	I/O	I/O
9	NC	I/O
10	NC	I/O
11	TRST, I/O	TRST, I/O
12	I/O	I/O
13	NC	I/O
14	GND	GND
15	I/O	I/O
16	I/O	I/O
17	I/O	I/O
18	I/O	I/O
19	VCCI	VCCI
20	I/O	I/O
21	PRB, I/O	PRB, I/O
22	VCCA	VCCA
23	GND	GND
24	I/O	I/O
25	HCLK	HCLK
26	I/O	I/O
27	I/O	I/O
28	I/O	I/O
29	I/O	I/O
30	I/O	I/O
31	I/O	I/O
32	TDO, I/O	TDO, I/O

TQ64		
Pin Number	eX64 Function	eX128 Function
33	GND	GND
34	I/O	I/O
35	I/O	I/O
36	VCCA	VCCA
37	VCCI	VCCI
38	I/O	I/O
39	I/O	I/O
40	NC	I/O
41	NC	I/O
42	I/O	I/O
43	I/O	I/O
44	VCCA	VCCA
45*	GND/LP	GND/ LP
46	GND	GND
47	I/O	I/O
48	I/O	I/O
49	I/O	I/O
50	I/O	I/O
51	I/O	I/O
52	VCCI	VCCI
53	I/O	I/O
54	I/O	I/O
55	CLKA	CLKA
56	CLKB	CLKB
57	VCCA	VCCA
58	GND	GND
59	PRA, I/O	PRA, I/O
60	I/O	I/O
61	VCCI	VCCI
62	I/O	I/O
63	I/O	I/O
64	TCK, I/O	TCK, I/O

*Note: *Please read the LP pin descriptions for restrictions on their use.*

TQ100



Note: For Package Manufacturing and Environmental information, visit Resource center at www.microsemi.com/soc/products/rescenter/package/index.html.

TQ100			
Pin Number	**eX64 Function**	**eX128 Function**	**eX256 Function**
71	I/O	I/O	I/O
72	NC	I/O	I/O
73	NC	NC	I/O
74	NC	NC	I/O
75	NC	NC	I/O
76	NC	I/O	I/O
77	I/O	I/O	I/O
78	I/O	I/O	I/O
79	I/O	I/O	I/O
80	I/O	I/O	I/O
81	I/O	I/O	I/O
82	VCCI	VCCI	VCCI
83	I/O	I/O	I/O
84	I/O	I/O	I/O
85	I/O	I/O	I/O
86	I/O	I/O	I/O
87	CLKA	CLKA	CLKA
88	CLKB	CLKB	CLKB
89	NC	NC	NC
90	VCCA	VCCA	VCCA
91	GND	GND	GND
92	PRA, I/O	PRA, I/O	PRA, I/O
93	I/O	I/O	I/O
94	I/O	I/O	I/O
95	I/O	I/O	I/O
96	I/O	I/O	I/O
97	I/O	I/O	I/O
98	I/O	I/O	I/O
99	I/O	I/O	I/O
100	TCK, I/O	TCK, I/O	TCK, I/O

*Note: *Please read the LP pin descriptions for restrictions on their use.*

Revision	Changes	Page
Advance v0.4	In the Product Profile, the Maximum User I/Os for eX64 was changed to 84.	1-I
	In the Product Profile table, the Maximum User I/Os for eX128 was changed to 100.	1-I
Advance v0.3	The Mechanical Drawings section has been removed from the data sheet. The mechanical drawings are now contained in a separate document, “Package Characteristics and Mechanical Drawings,” available on the Actel web site.	
	A new section describing "Clock Resources"has been added.	1-3
	A new table describing "I/O Features"has been added.	1-6
	The "Pin Description"section has been updated and clarified.	1-31
	The original Electrical Specifications table was separated into two tables (2.5V and 3.3/5.0V). In both tables, several different currents are specified for V_{OH} and V_{OL}.	Page 8 and 9
	A new table listing 2.5V low power specifications and associated power graphs were added.	page 9
	Pin functions for eX256 TQ100 have been added to the "TQ100"table.	2-3
	A CS49 pin drawing and pin assignment table including eX64 and eX128 pin functions have been added.	page 26
	A CS128 pin drawing and pin assignment table including eX64, eX128, and eX256 pin functions have been added.	pages 26-27
	A CS180 pin drawing and pin assignment table for eX256 pin functions have been added.	pages 27, 31
Advance v0.2	The following table note was added to the eX Timing Characteristics table for clarification: Clock skew improves as the clock network becomes more heavily loaded.	pages 14-15

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