E·XFL



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Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	256
Total RAM Bits	-
Number of I/O	46
Number of Gates	6000
Voltage - Supply	2.3V ~ 2.7V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	64-LQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/ex128-ftqg64

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



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Routing Resources

Clusters and SuperClusters can be connected through the use of two innovative local routing resources called FastConnect and DirectConnect, which enable extremely fast and predictable interconnection of modules within Clusters and SuperClusters (Figure 1-4). This routing architecture also dramatically reduces the number of antifuses required to complete a circuit, ensuring the highest possible performance.

DirectConnect is a horizontal routing resource that provides connections from a C-cell to its neighboring R-cell in a given SuperCluster. DirectConnect uses a hard-wired signal path requiring no programmable interconnection to achieve its fast signal propagation time of less than 0.1 ns (–P speed grade).

FastConnect enables horizontal routing between any two logic modules within a given SuperCluster and vertical routing with the SuperCluster immediately below it. Only one programmable connection is used in a FastConnect path, delivering maximum pin-to-pin propagation of 0.3 ns (–P speed grade).

In addition to DirectConnect and FastConnect, the architecture makes use of two globally oriented routing resources known as segmented routing and high-drive routing. The segmented routing structure of Microsemi provides a variety of track lengths for extremely fast routing between SuperClusters. The exact combination of track lengths and antifuses within each path is chosen by the fully automatic place-and-route software to minimize signal propagation delays.



Figure 1-4 • DirectConnect and FastConnect for SuperClusters

Clock Resources

eX's high-drive routing structure provides three clock networks. The first clock, called HCLK, is hardwired from the HCLK buffer to the clock select MUX in each R-Cell. HCLK cannot be connected to combinational logic. This provides a fast propagation path for the clock signal, enabling the 3.9 ns clock-to-out (pad-to-pad) performance of the eX devices. The hard-wired clock is tuned to provide a clock skew of less than 0.1 ns worst case. If not used, the HCLK pin must be tied LOW or HIGH and must not be left floating. Figure 1-5 describes the clock circuit used for the constant load HCLK.

HCLK does not function until the fourth clock cycle each time the device is powered up to prevent false output levels due to any possible slow power-on-reset signal and fast start-up clock circuit. To activate HCLK from the first cycle, the TRST pin must be reserved in the Design software and the pin must be tied to GND on the board. (See the "TRST, I/O Boundary Scan Reset Pin" on page 1-32).

The remaining two clocks (CLKA, CLKB) are global routed clock networks that can be sourced from external pins or from internal logic signals (via the CLKINT routed clock buffer) within the eX device. CLKA and CLKB may be connected to sequential cells or to combinational logic. If CLKA or CLKB is sourced from internal logic signals, the external clock pin cannot be used for any other input and must be tied LOW or HIGH and must not float. Figure 1-6 describes the CLKA and CLKB circuit used in eX devices.



Table 1-1 describes the possible connections of the routed clock networks, CLKA and CLKB. Unused clock pins must not be left floating and must be tied to HIGH or LOW.



Figure 1-5 • eX HCLK Clock Pad



Figure 1-6 • eX Routed Clock Buffer

Table 1-1 • Connections of Routed Clock Networks, CLKA and CLKB

Module	Pins
C-Cell	A0, A1, B0 and B1
R-Cell	CLKA, CLKB, S0, S1, PSET, and CLR
I/O-Cell	EN



Other Architectural Features

Performance

The combination of architectural features described above enables eX devices to operate with internal clock frequencies exceeding 350 MHz for very fast execution of complex logic functions. The eX family is an optimal platform upon which the functionality previously contained in CPLDs can be integrated. eX devices meet the performance goals of gate arrays, and at the same time, present significant improvements in cost and time to market. Using timing-driven place-and-route tools, designers can achieve highly deterministic device performance.

User Security

Microsemi FuseLock advantage provides the highest level of protection in the FPGA industry against unauthorized modifications. In addition to the inherent strengths of the architecture, special security fuses that are intended to prevent internal probing and overwriting are hidden throughout the fabric of the device. They are located such that they cannot be accessed or bypassed without destroying the rest of the device, making Microsemi antifuse FPGAs highly resistant to both invasive and more subtle noninvasive attacks.

Look for this symbol to ensure your valuable IP is secure. The FuseLock Symbol on the FPGA ensures that the device is safeguarded to cryptographic attacks.



Figure 1-7 • Fuselock

For more information, refer to Implementation of Security in Microsemi Antifuse FPGAs application note.

I/O Modules

Each I/O on an eX device can be configured as an input, an output, a tristate output, or a bidirectional pin. Even without the inclusion of dedicated I/O registers, these I/Os, in combination with array registers, can achieve clock-to-out (pad-to-pad) timing as fast as 3.9 ns. I/O cells in eX devices do not contain embedded latches or flip-flops and can be inferred directly from HDL code. The device can easily interface with any other device in the system, which in turn enables parallel design of system components and reduces overall design time.

All unused I/Os are configured as tristate outputs by Microsemi's Designer software, for maximum flexibility when designing new boards or migrating existing designs. Each I/O module has an available pull-up or pull-down resistor of approximately 50 k Ω that can configure the I/O in a known state during power-up. Just shortly before V_{CCA} reaches 2.5 V, the resistors are disabled and the I/Os will be controlled by user logic.



Figure 1-8 to Figure 1-11 on page 1-9 show some sample power characteristics of eX devices.



Notes:

- 1. Device filled with 16-bit counters.
- 2. VCCA, VCCI = 2.7 V, device tested at room temperature.

Figure 1-8 • eX Dynamic Power Consumption – High Frequency



Notes:

- 1. Device filled with 16-bit counters.
- 2. VCCA, VCCI = 2.7 V, device tested at room temperature.

Figure 1-9 • eX Dynamic Power Consumption – Low Frequency



Boundary Scan Testing (BST)

All eX devices are IEEE 1149.1 compliant. eX devices offer superior diagnostic and testing capabilities by providing Boundary Scan Testing (BST) and probing capabilities. These functions are controlled through the special test pins (TMS, TDI, TCK, TDO and TRST). The functionality of each pin is defined by two available modes: Dedicated and Flexible, and is described in Table 1-4. In the dedicated test mode, TCK, TDI, and TDO are dedicated pins and cannot be used as regular I/Os. In flexible mode (default mode), TMS should be set HIGH through a pull-up resistor of 10 k Ω . TMS can be pulled LOW to initiate the test sequence.

Table 1-4 •	Boundary	y Scan Pin	Functionality
-------------	----------	------------	---------------

Dedicated Test Mode	Flexible Mode				
TCK, TDI, TDO are dedicated BST pins	TCK, TDI, TDO are flexible and may be used as I/Os				
No need for pull-up resistor for TMS and TDI	Use a pull-up resistor of 10 k Ω on TMS				

Dedicated Test Mode

In Dedicated mode, all JTAG pins are reserved for BST; designers cannot use them as regular I/Os. An internal pull-up resistor is automatically enabled on both TMS and TDI pins, and the TMS pin will function as defined in the IEEE 1149.1 (JTAG) specification.

To select Dedicated mode, users need to reserve the JTAG pins in Microsemi's Designer software by checking the **Reserve JTAG** box in the Device Selection Wizard (Figure 1-12). JTAG pins comply with LVTTL/TTL I/O specification regardless of whether they are used as a user I/O or a JTAG I/O. Refer to the "3.3 V LVTTL Electrical Specifications" section and "5.0 V TTL Electrical Specifications" section on page 1-18 for detailed specifications.

Dev	vice Selection Wizard - Variations
	Reserve Pins
	Reserve JTAG
	Reserve JTAG Test Reset
	Reserve Probe

Figure 1-12 • Device Selection Wizard

Flexible Mode

In Flexible Mode, TDI, TCK and TDO may be used as either user I/Os or as JTAG input pins. The internal resistors on the TMS and TDI pins are disabled in flexible JTAG mode, and an external 10 k Ω pull-resistor to V_{CCI} is required on the TMS pin.

To select the Flexible mode, users need to clear the check box for **Reserve JTAG** in the Device Selection Wizard in Microsemi's Designer software. The functionality of TDI, TCK, and TDO pins is controlled by the BST TAP controller. The TAP controller receives two control inputs, TMS and TCK. Upon power-up, the TAP controller enters the Test-Logic-Reset state. In this state, TDI, TCK, and TDO function as user I/Os. The TDI, TCK, and TDO pins are transformed from user I/Os into BST pins when the TMS pin is LOW at the first rising edge of TCK. The TDI, TCK, and TDO pins return to user I/Os when TMS is held HIGH for at least five TCK cycles.



Related Documents

Datasheet

eX Automotive Family FPGAs www.microsemi.com/soc/documents/eX_Auto_DS.pdf

Application Notes

Maximizing Logic Utilization in eX, SX and SX-A FPGA Devices Using CC Macros www.microsemi.com/soc/documents/CC_Macro_AN.pdf Implementation of Security in Microsemi Antifuse FPGAs www.microsemi.com/soc/documents/Antifuse_Security_AN.pdf Microsemi eX, SX-A, and RT54SX-S I/Os www.microsemi.com/soc/documents/antifuseIO_AN.pdf Microsemi SX-A and RT54SX-S Devices in Hot-Swap and Cold-Sparing Applications www.microsemi.com/soc/documents/HotSwapColdSparing_AN.pdf Design For Low Power in Microsemi Antifuse FPGAs www.microsemi.com/soc/documents/Low_Power_AN.pdf Programming Antifuse Devices www.microsemi.com/soc/documents/AntifuseProgram_AN.pdf

User Guides

Silicon Sculptor II User's Guide www.microsemi.com/soc/documents/SiliSculptII_Sculpt3_ug.pdf

Miscellaneous

Libero IDE flow www.microsemi.com/soc/products/tools/libero/flow.html



Power Dissipation

Power consumption for eX devices can be divided into two components: static and dynamic.

Static Power Component

The power due to standby current is typically a small component of the overall power. Typical standby current for eX devices is listed in the Table 1-11 on page 1-16. For example, the typical static power for eX128 at 3.3 V V_{CCl} is:

ICC * VCCA = 795 µA x 2.5 V = 1.99 mW

Dynamic Power Component

Power dissipation in CMOS devices is usually dominated by the dynamic power dissipation. This component is frequency-dependent and a function of the logic and the external I/O. Dynamic power dissipation results from charging internal chip capacitance due to PC board traces and load device inputs. An additional component of the dynamic power dissipation is the totem pole current in the CMOS transistor pairs. The net effect can be associated with an equivalent capacitance that can be combined with frequency and voltage to represent dynamic power dissipation.

Dynamic power dissipation = CEQ * VCCA² x F

where:

CEQ = Equivalent capacitance

F = switching frequency

Equivalent capacitance is calculated by measuring ICCA at a specified frequency and voltage for each circuit component of interest. Measurements have been made over a range of frequencies at a fixed value of VCC. Equivalent capacitance is frequency-independent, so the results can be used over a wide range of operating conditions. Equivalent capacitance values are shown below.

CEQ Values for eX Devices

Combinatorial modules (Ceqcm)	1.70 pF
Sequential modules (Ceqsm)	1.70 pF
Input buffers (Ceqi)	1.30 pF
Output buffers (Ceqo)	7.40 pF
Routed array clocks (Ceqcr)	1.05 pF

The variable and fixed capacitance of other device components must also be taken into account when estimating the dynamic power dissipation.

Table 1-12 shows the capacitance of the clock components of eX devices.

Table 1-12 • Capacitance of Clock Components of eX Devices

	eX64	eX128	eX256
Dedicated array clock – variable (Ceqhv)	0.85 pF	0.85 pF	0.85 pF
Dedicated array clock – fixed (Ceqhf)	18.00 pF	20.00 pF	25.00 pF
Routed array clock A (r1)	23.00 pF	28.00 pF	35.00 pF
Routed array clock B (r2)	23.00 pF	28.00 pF	35.00 pF



Thermal Characteristics

The temperature variable in the Designer software refers to the junction temperature, not the ambient temperature. This is an important distinction because the heat generated from dynamic power consumption is usually hotter than the ambient temperature. EQ 1, shown below, can be used to calculate junction temperature.

Junction Temperature = $\Delta T + T_a(1)$

Where:

 T_a = Ambient Temperature

 ΔT = Temperature gradient between junction (silicon) and ambient = θ_{ja} * P

P = Power

 θ_{ja} = Junction to ambient of package. θ_{ja} numbers are located in the "Package Thermal Characteristics" section below.

Package Thermal Characteristics

The device junction-to-case thermal characteristic is θ_{jc} , and the junction-to-ambient air characteristic is θ_{ja} . The thermal characteristics for θ_{ja} are shown with two different air flow rates. $\theta_{jc \ is \ provided \ for \ reference.}$ The maximum junction temperature is 150°C.

The maximum power dissipation allowed for eX devices is a function of θ_{ja} . A sample calculation of the absolute maximum power dissipation allowed for a TQFP 100-pin package at commercial temperature and still air is as follows:

Maximum Power Allowed = $\frac{\text{Max. junction temp. } (^{\circ}\text{C}) - \text{Max. ambient temp. } (^{\circ}\text{C})}{\theta_{ja}(^{\circ}\text{C/W})} = \frac{150^{\circ}\text{C} - 70^{\circ}\text{C}}{33.5^{\circ}\text{C/W}} = 2.39\text{W}$

Package Type	Pin Count	θ _{jc}	Still Air	1.0 m/s 200 ft/min	2.5 m/s 500 ft/min	Units
Thin Quad Flat Pack (TQFP)	64	12.0	42.4	36.3	34.0	°C/W
Thin Quad Flat Pack (TQFP)	100	14.0	33.5	27.4	25.0	°C/W

EQ 1



eX Timing Model



Note: Values shown for eX128–P, worst-case commercial conditions (5.0 V, 35 pF Pad Load). Figure 1-14 • eX Timing Model

Hardwired Clock

External Setup = $t_{INYH} + t_{IRD1} + t_{SUD} - t_{HCKH}$ = 0.7 + 0.3 + 0.5 - 1.1 = 0.4 ns Clock-to-Out (Pad-to-Pad), typical = $t_{HCKH} + t_{RCO} + t_{RD1} + t_{DHL}$

= 1.1 + 0.6 + 0.3 + 2.6 = 4.6 ns

Routed Clock

External Setup = $t_{INYH} + t_{IRD2} + t_{SUD} - t_{RCKH}$ = 0.7 + 0.4 + 0.5 - 1.3= 0.3 ns

Clock-to-Out (Pad-to-Pad), typical

 $= t_{RCKH} + t_{RCO} + t_{RD1} + t_{DHL}$

= 1.3+ 0.6 + 0.3 + 2.6 = 4.8 ns



Output Buffer Delays



Table 1-13 • Output Buffer Delays

AC Test Loads



Figure 1-15 • AC Test Loads



Input Buffer Delays



Table 1-14 • Input Buffer Delays

C-Cell Delays



Table 1-15 • C-Cell Delays



Table 1-18 • eX Family Timing Characteristics (Worst-Case Commercial Conditions VCCA = 2.3 V, VCCI = 4.75 V, T_J = 70°C)

		–P S	peed	Std S	Speed	-F S	Speed	
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Units
Dedicated (H	lard-Wired) Array Clock Networks							
t _{нскн}	Input LOW to HIGH (Pad to R-Cell Input)		1.1		1.6		2.3	ns
t _{HCKL}	Input HIGH to LOW (Pad to R-Cell Input)		1.1		1.6		2.3	ns
t _{HPWH}	Minimum Pulse Width HIGH	1.4		2.0		2.8		ns
t _{HPWL}	Minimum Pulse Width LOW	1.4		2.0		2.8		ns
t _{HCKSW}	Maximum Skew		<0.1		<0.1		<0.1	ns
t _{HP}	Minimum Period	2.8		4.0		5.6		ns
f _{HMAX}	Maximum Frequency		357		250		178	MHz
Routed Array	y Clock Networks							
t _{RCKH}	Input LOW to HIGH (Light Load) (Pad to R-Cell Input) MAX.		1.1		1.6		2.2	ns
t _{RCKL}	Input HIGH to LOW (Light Load) (Pad to R-Cell Input) MAX.		1.0		1.4		2.0	ns
t _{RCKH}	Input LOW to HIGH (50% Load) (Pad to R-Cell Input) MAX.		1.2		1.7		2.4	ns
t _{RCKL}	Input HIGH to LOW (50% Load) (Pad to R-Cell Input) MAX.		1.2		1.7		2.4	ns
t _{RCKH}	Input LOW to HIGH (100% Load) (Pad to R-Cell Input) MAX.		1.3		1.9		2.6	ns
t _{RCKL}	Input HIGH to LOW (100% Load) (Pad to R-Cell Input) MAX.		1.3		1.9		2.6	ns
t _{RPWH}	Min. Pulse Width HIGH	1.5		2.1		3.0		ns
t _{RPWL}	Min. Pulse Width LOW	1.5		2.1		3.0		ns
t _{RCKSW} *	Maximum Skew (Light Load)		0.2		0.3		0.4	ns
t _{RCKSW} *	Maximum Skew (50% Load)		0.1		0.2		0.3	ns
t _{RCKSW} *	Maximum Skew (100% Load)		0.1		0.1		0.2	ns

Note: *Clock skew improves as the clock network becomes more heavily loaded.



		'–P' :	Speed	'Std'	Speed	'–F' \$	Speed	
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Units
Dedicated (H	lard-Wired) Array Clock Networks							
t _{нскн}	Input LOW to HIGH (Pad to R-Cell Input)		1.1		1.6		2.3	ns
t _{HCKL}	Input HIGH to LOW (Pad to R-Cell Input)		1.1		1.6		2.3	ns
t _{HPWH}	Minimum Pulse Width HIGH	1.4		2.0		2.8		ns
t _{HPWL}	Minimum Pulse Width LOW	1.4		2.0		2.8		ns
t _{HCKSW}	Maximum Skew		<0.1		<0.1		<0.1	ns
t _{HP}	Minimum Period	2.8		4.0		5.6		ns
f _{HMAX}	Maximum Frequency		357		250		178	MHz
Routed Array	y Clock Networks							
t _{RCKH}	Input LOW to HIGH (Light Load) (Pad to R-Cell Input) MAX.		1.0		1.4		2.0	ns
t _{RCKL}	Input HIGH to LOW (Light Load) (Pad to R-Cell Input) MAX.		1.0		1.4		2.0	ns
t _{RCKH}	Input LOW to HIGH (50% Load) (Pad to R-Cell Input) MAX.		1.2		1.7		2.4	ns
t _{RCKL}	Input HIGH to LOW (50% Load) (Pad to R-Cell Input) MAX.		1.2		1.7		2.4	ns
t _{RCKH}	Input LOW to HIGH (100% Load) (Pad to R-Cell Input) MAX.		1.4		2.0		2.8	ns
t _{RCKL}	Input HIGH to LOW (100% Load) (Pad to R-Cell Input) MAX.		1.4		2.0		2.8	ns
t _{RPWH}	Min. Pulse Width HIGH	1.4		2.0		2.8		ns
t _{RPWL}	Min. Pulse Width LOW	1.4		2.0		2.8		ns
t _{RCKSW} *	Maximum Skew (Light Load)		0.2		0.3		0.4	ns
t _{RCKSW} *	Maximum Skew (50% Load)		0.2		0.2		0.3	ns
t _{RCKSW} *	Maximum Skew (100% Load)		0.1		0.1		0.2	ns

Table 1-19 • eX Family Timing Characteristics (Worst-Case Commercial Conditions VCCA = 2.3V, VCCI = 2.3 V or 3.0V, T_J = 70°C)

Note: *Clock skew improves as the clock network becomes more heavily loaded.



Pin Description

CLKA/B Routed Clock A and B

These pins are clock inputs for clock distribution networks. Input levels are compatible with standard TTL or LVTTL specifications. The clock input is buffered prior to clocking the R-cells. If not used, this pin must be set LOW or HIGH on the board. It must not be left floating.

GND Ground

LOW supply voltage.

HCLK Dedicated (Hardwired) Array Clock

This pin is the clock input for sequential modules. Input levels are compatible with standard TTL or LVTTL specifications. This input is directly wired to each R-cell and offers clock speeds independent of the number of R-cells being driven. If not used, this pin must be set LOW or HIGH on the board. It must not be left floating.

I/O Input/Output

The I/O pin functions as an input, output, tristate, or bidirectional buffer. Based on certain configurations, input and output levels are compatible with standard TTL or LVTTL specifications. Unused I/O pins are automatically tristated by the Designer software.

LP Low Power Pin

Controls the low power mode of the eX devices. The device is placed in the low power mode by connecting the LP pin to logic HIGH. In low power mode, all I/Os are tristated, all input buffers are turned OFF, and the core of the device is turned OFF. To exit the low power mode, the LP pin must be set LOW. The device enters the low power mode 800 ns after the LP pin is driven to a logic HIGH. It will resume normal operation 200 μ s after the LP pin is driven to a logic LOW. LP pin should not be left floating. Under normal operating condition it should be tied to GND via 10 k Ω resistor.

NC No Connection

This pin is not connected to circuitry within the device. These pins can be driven to any voltage or can be left floating with no effect on the operation of the device.

PRA/PRB, I/O Probe A/B

The Probe pin is used to output data from any user-defined design node within the device. This diagnostic pin can be used independently or in conjunction with the other probe pin to allow real-time diagnostic output of any signal path within the device. The Probe pin can be used as a user-defined I/O when verification has been completed. The pin's probe capabilities can be permanently disabled to protect programmed design confidentiality.

TCK, I/O Test Clock

Test clock input for diagnostic probe and device programming. In flexible mode, TCK becomes active when the TMS pin is set LOW (refer to Table 1-4 on page 1-10). This pin functions as an I/O when the boundary scan state machine reaches the "logic reset" state.

TDI, I/O Test Data Input

Serial input for boundary scan testing and diagnostic probe. In flexible mode, TDI is active when the TMS pin is set LOW (refer to Table 1-4 on page 1-10). This pin functions as an I/O when the boundary scan state machine reaches the "logic reset" state.

TDO, I/O Test Data Output

Serial output for boundary scan testing. In flexible mode, TDO is active when the TMS pin is set LOW (refer to Table 1-4 on page 1-10). This pin functions as an I/O when the boundary scan state machine reaches the "logic reset" state. When Silicon Explorer is being used, TDO will act as an output when the "checksum" command is run. It will return to user I/O when "checksum" is complete.



2 – Package Pin Assignments

TQ64



Note: For Package Manufacturing and Environmental information, visit Resource center at www.microsemi.com/soc/products/rescenter/package/index.html.



TQ100



Note: For Package Manufacturing and Environmental information, visit Resource center at www.microsemi.com/soc/products/rescenter/package/index.html.



	TQ100				
Pin Number	eX64 Function	eX128 Function	eX256 Function		
71	I/O	I/O	I/O		
72	NC	I/O	I/O		
73	NC	NC	I/O		
74	NC	NC	I/O		
75	NC	NC	I/O		
76	NC	I/O	I/O		
77	I/O	I/O	I/O		
78	I/O	I/O	I/O		
79	I/O	I/O	I/O		
80	I/O	I/O	I/O		
81	I/O	I/O	I/O		
82	VCCI	VCCI	VCCI		
83	I/O	I/O	I/O		
84	I/O	I/O	I/O		
85	I/O	I/O	I/O		
86	I/O	I/O	I/O		
87	CLKA	CLKA	CLKA		
88	CLKB	CLKB	CLKB		
89	NC	NC	NC		
90	VCCA	VCCA	VCCA		
91	GND	GND	GND		
92	PRA, I/O	PRA, I/O	PRA, I/O		
93	I/O	I/O	I/O		
94	I/O	I/O	I/O		
95	I/O	I/O	I/O		
96	I/O	I/O	I/O		
97	I/O	I/O	I/O		
98	I/O	I/O	I/O		
99	I/O	I/O	I/O		
100	TCK, I/O	TCK, I/O	TCK, I/O		

Note: *Please read the LP pin descriptions for restrictions on their use.



3 – Datasheet Information

List of Changes

The following table lists critical changes that were made in the current version of the document.

Revision	Changes	Page
Revision 10 (October 2012)	The "User Security" section was revised to clarify that although no existing security measures can give an absolute guarantee, Microsemi FPGAs implement indus standard security (SAR 34677).	
	Package names used in the "Product Profile" section and "Package Pin Assignments" section were revised to match standards given in <i>Package Mechanical Drawings</i> (SAR 34779).	І 2-1
Revision 9 (June 2011)	The versioning system for datasheets has been changed. Datasheets are assigned a revision number that increments each time the datasheet is revised. The "eX Device Status" table indicates the status for each device in the device family.	=
	The Chip Scale packages (CS49, CS128, CS181) are no longer offered for eX devices. They have been removed from the product family information. Pin tables for CSP packages have been removed from the datasheet (SAR 32002).	N/A
Revision 8 (v4.3, June 2006)	The "Ordering Information" was updated with RoHS information. The TQFP measurement was also updated.	Ш
	The "Dedicated Test Mode" was updated.	1-10
	Note 5 was added to the "3.3 V LVTTL Electrical Specifications" and "5.0 V TTL Electrical Specifications" tables	1-18
	The "LP Low Power Pin" description was updated.	1-31
Revision 7 (v4.2, June 2004)	The "eX Timing Model" was updated.	1-22
v4.1	The "Development Tool Support" section was updated.	1-13
	The "Package Thermal Characteristics" section was updated.	1-21
v4.0	The "Product Profile" section was updated.	1-I
	The "Ordering Information" section was updated.	1-II
	The "Temperature Grade Offerings" section is new.	1-111
	The "Speed Grade and Temperature Grade Matrix" section is new.	1-III
	The "eX FPGA Architecture and Characteristics" section was updated.	1-1
	The "Clock Resources" section was updated.	1-3
	Table 1-1 •Connections of Routed Clock Networks, CLKA and CLKB is new.	1-4
	The "User Security" section was updated.	1-5
	The "I/O Modules" section was updated.	1-5
	The "Hot-Swapping" section was updated.	1-6
	The "Power Requirements" section was updated.	1-6
	The "Low Power Mode" section was updated.	1-6
	The "Boundary Scan Testing (BST)" section was updated.	1-10
	The "Dedicated Test Mode" section was updated.	1-10



Revision	Changes	Page
Advance v0.4	Jvance v0.4 In the Product Profile, the Maximum User I/Os for eX64 was changed to 84.	
	In the Product Profile table, the Maximum User I/Os for eX128 was changed to 100.	1-I
Advance v0.3	The Mechanical Drawings section has been removed from the data sheet. The mechanical drawings are now contained in a separate document, "Package Characteristics and Mechanical Drawings," available on the Actel web site.	
	A new section describing "Clock Resources" has been added.	1-3
	A new table describing "I/O Features"has been added.	1-6
	The "Pin Description" section has been updated and clarified.	1-31
	The original Electrical Specifications table was separated into two tables (2.5V and 3.3/5.0V). In both tables, several different currents are specified for V_{OH} and V_{OL} .	Page 8 and 9
	A new table listing 2.5V low power specifications and associated power graphs were added.	page 9
	Pin functions for eX256 TQ100 have been added to the "TQ100"table.	2-3
	A CS49 pin drawing and pin assignment table including eX64 and eX128 pin functions have been added.	page 26
	A CS128 pin drawing and pin assignment table including eX64, eX128, and eX256 pin functions have been added.	pages 26-27
	A CS180 pin drawing and pin assignment table for eX256 pin functions have been added.	pages27, 31
Advance v0.2	The following table note was added to the eX Timing Characteristics table for clarification: Clock skew improves as the clock network becomes more heavily loaded.	pages 14-15