Microchip Technology - EX128-TQ100 Datasheet

Welcome to **E-XFL.COM**

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	256
Total RAM Bits	-
Number of I/O	70
Number of Gates	6000
Voltage - Supply	2.3V ~ 2.7V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	100-LQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/ex128-tq100

Temperature Grade Offerings

Device\ Package	TQ64	TQ100
eX64	C, I, A	C, I, A
eX128	C, I, A	C, I, A
eX256	C, I, A	C, I, A

Note: *C = Commercial*
I = Industrial
A = Automotive

Speed Grade and Temperature Grade Matrix

	–F	Std	–P
C	✓	✓	✓
I		✓	✓
A		✓	

Note: *P = Approximately 30% faster than Standard*
–F = Approximately 40% slower than Standard
Refer to the eX Automotive Family FPGAs *datasheet for details on automotive temperature offerings.*

Contact your local Microsemi representative for device availability.

Table of Contents

eX FPGA Architecture and Characteristics

Package Pin Assignments

Datasheet Information

1 – eX FPGA Architecture and Characteristics

General Description

The eX family of FPGAs is a low-cost solution for low-power, high-performance designs. The inherent low power attributes of the antifuse technology, coupled with an additional low static power mode, make these devices ideal for power-sensitive applications. Fabricated with an advanced 0.22 mm CMOS antifuse technology, these devices achieve high performance with no power penalty.

eX Family Architecture

Microsemi eX family is implemented on a high-voltage twin-well CMOS process using 0.22 µm design rules. The eX family architecture uses a “sea-of-modules” structure where the entire floor of the device is covered with a grid of logic modules with virtually no chip area lost to interconnect elements or routing. Interconnection among these logic modules is achieved using Microsemi patented metal-to-metal programmable antifuse interconnect elements. The antifuse interconnect is made up of a combination of amorphous silicon and dielectric material with barrier metals and has an "on" state resistance of 25Ω with a capacitance of 1.0fF for low-signal impedance. The antifuses are normally open circuit and, when programmed, form a permanent low-impedance connection. The eX family provides two types of logic modules, the register cell (R-cell) and the combinatorial cell (C-cell).

The R-cell contains a flip-flop featuring asynchronous clear, asynchronous preset, and clock enable (using the S0 and S1 lines) control signals (Figure 1-1). The R-cell registers feature programmable clock polarity selectable on a register-by-register basis. This provides additional flexibility while allowing mapping of synthesized functions into the eX FPGA. The clock source for the R-cell can be chosen from either the hard-wired clock or the routed clock.

The C-cell implements a range of combinatorial functions up to five inputs (Figure 1-2 on page 1-2). Inclusion of the DB input and its associated inverter function enables the implementation of more than 4,000 combinatorial functions in the eX architecture in a single module.

Two C-cells can be combined together to create a flip-flop to imitate an R-cell via the use of the CC macro. This is particularly useful when implementing non-timing-critical paths and when the design engineer is running out of R-cells. More information about the CC macro can be found in the *Maximizing Logic Utilization in eX, SX and SX-A FPGA Devices Using CC Macros* application note.

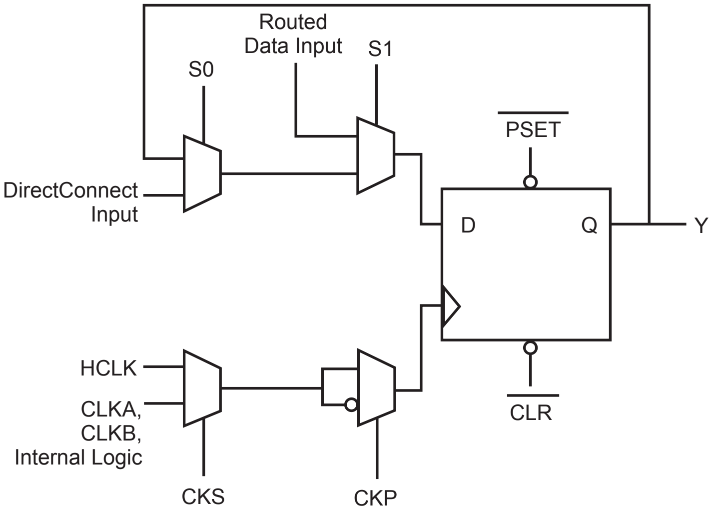


Figure 1-1 • **R-Cell**

Routing Resources

Clusters and SuperClusters can be connected through the use of two innovative local routing resources called FastConnect and DirectConnect, which enable extremely fast and predictable interconnection of modules within Clusters and SuperClusters (Figure 1-4). This routing architecture also dramatically reduces the number of antifuses required to complete a circuit, ensuring the highest possible performance.

DirectConnect is a horizontal routing resource that provides connections from a C-cell to its neighboring R-cell in a given SuperCluster. DirectConnect uses a hard-wired signal path requiring no programmable interconnection to achieve its fast signal propagation time of less than 0.1 ns (–P speed grade).

FastConnect enables horizontal routing between any two logic modules within a given SuperCluster and vertical routing with the SuperCluster immediately below it. Only one programmable connection is used in a FastConnect path, delivering maximum pin-to-pin propagation of 0.3 ns (–P speed grade).

In addition to DirectConnect and FastConnect, the architecture makes use of two globally oriented routing resources known as segmented routing and high-drive routing. The segmented routing structure of Microsemi provides a variety of track lengths for extremely fast routing between SuperClusters. The exact combination of track lengths and antifuses within each path is chosen by the fully automatic place-and-route software to minimize signal propagation delays.

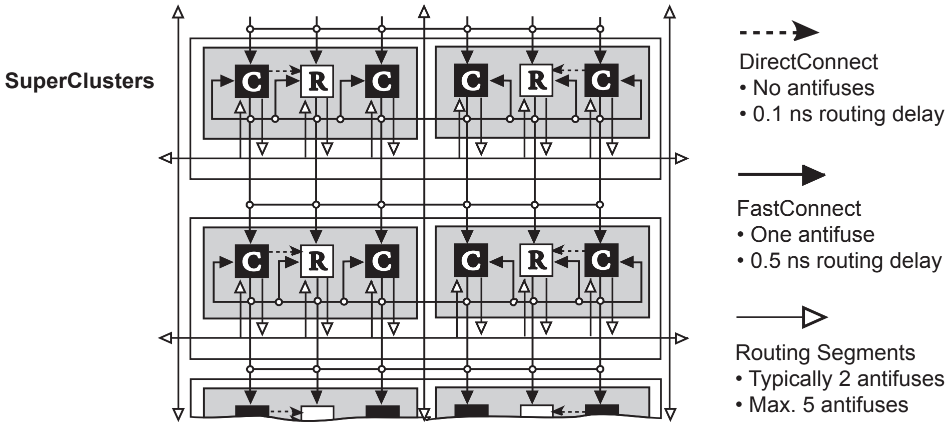


Figure 1-4 • **DirectConnect and FastConnect for SuperClusters**

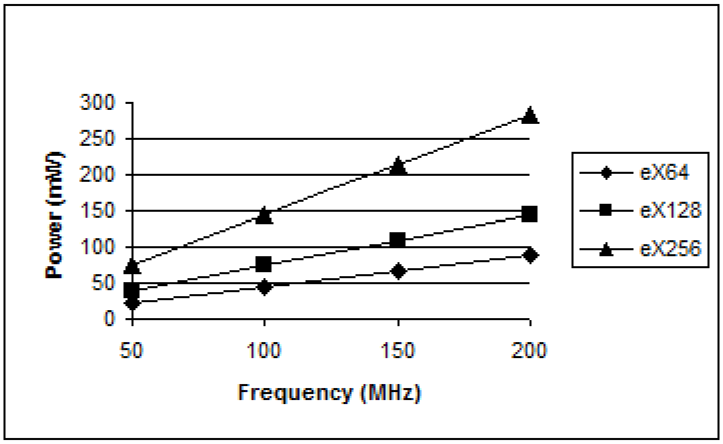
Clock Resources

eX's high-drive routing structure provides three clock networks. The first clock, called HCLK, is hardwired from the HCLK buffer to the clock select MUX in each R-Cell. HCLK cannot be connected to combinational logic. This provides a fast propagation path for the clock signal, enabling the 3.9 ns clock-to-out (pad-to-pad) performance of the eX devices. The hard-wired clock is tuned to provide a clock skew of less than 0.1 ns worst case. If not used, the HCLK pin must be tied LOW or HIGH and must not be left floating. Figure 1-5 describes the clock circuit used for the constant load HCLK.

HCLK does not function until the fourth clock cycle each time the device is powered up to prevent false output levels due to any possible slow power-on-reset signal and fast start-up clock circuit. To activate HCLK from the first cycle, the TRST pin must be reserved in the Design software and the pin must be tied to GND on the board. (See the "TRST, I/O Boundary Scan Reset Pin" on page 1-32).

The remaining two clocks (CLKA, CLKB) are global routed clock networks that can be sourced from external pins or from internal logic signals (via the CLKINT routed clock buffer) within the eX device. CLKA and CLKB may be connected to sequential cells or to combinational logic. If CLKA or CLKB is sourced from internal logic signals, the external clock pin cannot be used for any other input and must be tied LOW or HIGH and must not float. Figure 1-6 describes the CLKA and CLKB circuit used in eX devices.

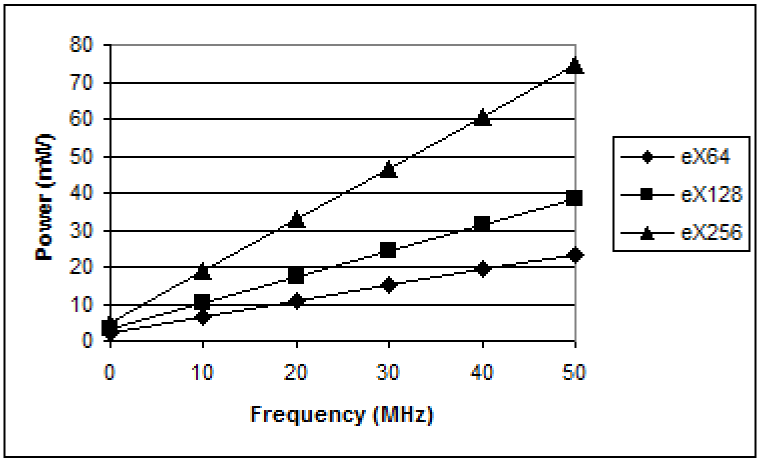
Figure 1-8 to Figure 1-11 on page 1-9 show some sample power characteristics of eX devices.



Notes:

1. *Device filled with 16-bit counters.*
2. *VCCA, VCCI = 2.7 V, device tested at room temperature.*

Figure 1-8 • **eX Dynamic Power Consumption – High Frequency**



Notes:

1. *Device filled with 16-bit counters.*
2. *VCCA, VCCI = 2.7 V, device tested at room temperature.*

Figure 1-9 • **eX Dynamic Power Consumption – Low Frequency**

Boundary Scan Testing (BST)

All eX devices are IEEE 1149.1 compliant. eX devices offer superior diagnostic and testing capabilities by providing Boundary Scan Testing (BST) and probing capabilities. These functions are controlled through the special test pins (TMS, TDI, TCK, TDO and TRST). The functionality of each pin is defined by two available modes: Dedicated and Flexible, and is described in Table 1-4. In the dedicated test mode, TCK, TDI, and TDO are dedicated pins and cannot be used as regular I/Os. In flexible mode (default mode), TMS should be set HIGH through a pull-up resistor of 10 kΩ. TMS can be pulled LOW to initiate the test sequence.

Table 1-4 • **Boundary Scan Pin Functionality**

Dedicated Test Mode	Flexible Mode
TCK, TDI, TDO are dedicated BST pins	TCK, TDI, TDO are flexible and may be used as I/Os
No need for pull-up resistor for TMS and TDI	Use a pull-up resistor of 10 kΩ on TMS

Dedicated Test Mode

In Dedicated mode, all JTAG pins are reserved for BST; designers cannot use them as regular I/Os. An internal pull-up resistor is automatically enabled on both TMS and TDI pins, and the TMS pin will function as defined in the IEEE 1149.1 (JTAG) specification.

To select Dedicated mode, users need to reserve the JTAG pins in Microsemi's Designer software by checking the **Reserve JTAG** box in the Device Selection Wizard (Figure 1-12). JTAG pins comply with LVTTL/TTL I/O specification regardless of whether they are used as a user I/O or a JTAG I/O. Refer to the "3.3 V LVTTL Electrical Specifications" section and "5.0 V TTL Electrical Specifications" section on page 1-18 for detailed specifications.

Device Selection Wizard - Variations

Reserve Pins

☑ Reserve JTAG

☑ Reserve JTAG Test Reset

☑ Reserve Probe

Figure 1-12 • **Device Selection Wizard**

Flexible Mode

In Flexible Mode, TDI, TCK and TDO may be used as either user I/Os or as JTAG input pins. The internal resistors on the TMS and TDI pins are disabled in flexible JTAG mode, and an external 10 kΩ pull-resistor to V_{CCI} is required on the TMS pin.

To select the Flexible mode, users need to clear the check box for **Reserve JTAG** in the Device Selection Wizard in Microsemi's Designer software. The functionality of TDI, TCK, and TDO pins is controlled by the BST TAP controller. The TAP controller receives two control inputs, TMS and TCK. Upon power-up, the TAP controller enters the Test-Logic-Reset state. In this state, TDI, TCK, and TDO function as user I/Os. The TDI, TCK, and TDO pins are transformed from user I/Os into BST pins when the TMS pin is LOW at the first rising edge of TCK. The TDI, TCK, and TDO pins return to user I/Os when TMS is held HIGH for at least five TCK cycles.

Programming

Device programming is supported through Silicon Sculptor series of programmers. In particular, Silicon Sculptor II is a compact, robust, single-site and multi-site device programmer for the PC.

With standalone software, Silicon Sculptor II allows concurrent programming of multiple units from the same PC, ensuring the fastest programming times possible. Each fuse is subsequently verified by Silicon Sculptor II to insure correct programming. In addition, integrity tests ensure that no extra fuses are programmed. Silicon Sculptor II also provides extensive hardware self-testing capability.

The procedure for programming an eX device using Silicon Sculptor II is as follows:

1. Load the *.AFM file
2. Select the device to be programmed
3. Begin programming

When the design is ready to go to production, Microsemi offers device volume-programming services either through distribution partners or via in-house programming from the factory.

For more details on programming eX devices, please refer to the *Programming Antifuse Devices* application note and the *Silicon Sculptor II User's Guide*.

Probing Capabilities

eX devices provide internal probing capability that is accessed with the JTAG pins. The Silicon Explorer II Diagnostic hardware is used to control the TDI, TCK, TMS and TDO pins to select the desired nets for debugging. The user simply assigns the selected internal nets in the Silicon Explorer II software to the PRA/PRB output pins for observation. Probing functionality is activated when the BST pins are in JTAG mode and the TRST pin is driven HIGH or left floating. If the TRST pin is held LOW, the TAP controller will remain in the Test-Logic-Reset state so no probing can be performed. The Silicon Explorer II automatically places the device into JTAG mode, but the user must drive the TRST pin HIGH or allow the internal pull-up resistor to pull TRST HIGH.

When you select the **Reserve Probe Pin** box, as shown in Figure 1-12 on page 1-10, the layout tool reserves the PRA and PRB pins as dedicated outputs for probing. This reserve option is merely a guideline. If the Layout tool requires that the PRA and PRB pins be user I/Os to achieve successful layout, the tool will use these pins for user I/Os. If you assign user I/Os to the PRA and PRB pins and select the **Reserve Probe Pin** option, Designer Layout will override the "Reserve Probe Pin" option and place your user I/Os on those pins.

To allow for probing capabilities, the security fuse must not be programmed. Programming the security fuse will disable the probe circuitry. Table 1-8 on page 1-13 summarizes the possible device configurations for probing once the device leaves the Test-Logic-Reset JTAG state.

Silicon Explorer II Probe

Silicon Explorer II is an integrated hardware and software solution that, in conjunction with Microsemi Designer software tools, allow users to examine any of the internal nets of the device while it is operating in a prototype or a production system. The user can probe into an eX device via the PRA and PRB pins without changing the placement and routing of the design and without using any additional resources. Silicon Explorer II's noninvasive method does not alter timing or loading effects, thus shortening the debug cycle.

Silicon Explorer II does not require re-layout or additional MUXes to bring signals out to an external pin, which is necessary when using programmable logic devices from other suppliers.

Silicon Explorer II samples data at 100 MHz (asynchronous) or 66 MHz (synchronous). Silicon Explorer II attaches to a PC's standard COM port, turning the PC into a fully functional 18-channel logic analyzer. Silicon Explorer II allows designers to complete the design verification process at their desks and reduces verification time from several hours per cycle to a few seconds.

The Silicon Explorer II tool uses the boundary scan ports (TDI, TCK, TMS and TDO) to select the desired nets for verification. The selected internal nets are assigned to the PRA/PRB pins for observation. Figure 1-13 on page 1-13 illustrates the interconnection between Silicon Explorer II and the eX device to perform in-circuit verification.

Design Considerations

The TDI, TCK, TDO, PRA, and PRB pins should not be used as input or bidirectional ports. Since these pins are active during probing, critical signals input through these pins are not available while probing. In addition, the Security Fuse should not be programmed because doing so disables the probe circuitry. It is recommended to use a series 70Ω termination resistor on every probe connector (TDI, TCK, TMS, TDO, PRA, PRB). The 70Ω series termination is used to prevent data transmission corruption during probing and reading back the checksum.

***Table 1-8* • Device Configuration Options for Probe Capability (TRST pin reserved)**

JTAG Mode	TRST[1]	Security Fuse Programmed	PRA, PRB[2]	TDI, TCK, TDO[2]
Dedicated	LOW	No	User I/O[3]	Probing Unavailable
Flexible	LOW	No	User I/O[3]	User I/O[3]
Dedicated	HIGH	No	Probe Circuit Outputs	Probe Circuit Inputs
Flexible	HIGH	No	Probe Circuit Outputs	Probe Circuit Inputs
–	–	Yes	Probe Circuit Secured	Probe Circuit Secured

Notes:

1. *If TRST pin is not reserved, the device behaves according to TRST = HIGH in the table.*
2. *Avoid using the TDI, TCK, TDO, PRA, and PRB pins as input or bidirectional ports. Since these pins are active during probing, input signals will not pass through these pins and may cause contention.*
3. *If no user signal is assigned to these pins, they will behave as unused I/Os in this mode. Unused pins are automatically tristated by Microsemi Designer software.*

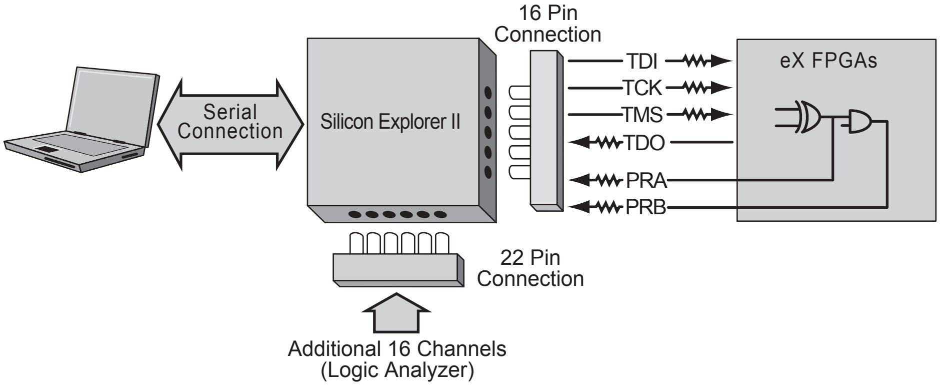


***Figure 1-13* • Silicon Explorer II Probe Setup**

Development Tool Support

The eX family of FPGAs is fully supported by both Libero® Integrated Design Environment and Designer FPGA Development software. Libero IDE is a design management environment that streamlines the design flow. Libero IDE provides an integrated design manager that seamlessly integrates design tools while guiding the user through the design flow, managing all design and log files, and passing necessary design data among tools. Additionally, Libero IDE allows users to integrate both schematic and HDL synthesis into a single flow and verify the entire design in a single environment. Libero IDE includes Synplify® for Microsemi from Synplicity®, ViewDraw for Microsemi from Mentor Graphics, ModelSim® HDL Simulator from Mentor Graphics®, WaveFormer Lite™ from SynaptiCAD™, and Designer software from Microsemi. Refer to the *Libero IDE flow* (located on Microsemi SoC Product Group's website) diagram for more information.

2.5 V / 3.3 V /5.0 V Operating Conditions

Table 1-9* • Absolute Maximum Ratings

Symbol	Parameter	Limits	Units
VCCI	DC Supply Voltage for I/Os	–0.3 to +6.0	V
VCCA	DC Supply Voltage for Array	–0.3 to +3.0	V
VI	Input Voltage	–0.5 to +5.75	V
VO	Output Voltage	–0.5 to $+V_{CCI}$	V
T_{STG}	Storage Temperature	–65 to +150	°C

Note: **Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Devices should not be operated outside the Recommended Operating Conditions.*

***Table 1-10* • Recommended Operating Conditions**

Parameter	Commercial	Industrial	Units
Temperature Range*	0 to +70	–40 to +85	°C
2.5V Power Supply Range (VCCA, VCCI)	2.3 to 2.7	2.3 to 2.7	V
3.3V Power Supply Range (VCCI)	3.0 to 3.6	3.0 to 3.6	V
5.0V Power Supply Range (VCCI)	4.75 to 5.25	4.75 to 5.25	V

Note: **Ambient temperature (T_A).*

***Table 1-11* • Typical eX Standby Current at 25°C**

Product	VCCA= 2.5 V VCCI = 2.5 V	VCCA = 2.5 V VCCI = 3.3 V	VCCA = 2.5 V VCCI = 5.0 V
eX64	397 µA	497 µA	700 µA
eX128	696 µA	795 µA	1,000 µA
eX256	698 µA	796 µA	2,000 µA

Thermal Characteristics

The temperature variable in the Designer software refers to the junction temperature, not the ambient temperature. This is an important distinction because the heat generated from dynamic power consumption is usually hotter than the ambient temperature. EQ 1, shown below, can be used to calculate junction temperature.

EQ 1

Junction Temperature = $\Delta T + T_a(1)$

Where:

T_a = Ambient Temperature

ΔT = Temperature gradient between junction (silicon) and ambient = $\theta_{ja} * P$

P = Power

θ_{ja} = Junction to ambient of package. θ_{ja} numbers are located in the "Package Thermal Characteristics" section below.

Package Thermal Characteristics

The device junction-to-case thermal characteristic is θ_{jc}, and the junction-to-ambient air characteristic is θ_{ja}. The thermal characteristics for θ_{ja} are shown with two different air flow rates. θ_{jc} is provided for reference.

The maximum junction temperature is 150°C.

The maximum power dissipation allowed for eX devices is a function of θ_{ja}. A sample calculation of the absolute maximum power dissipation allowed for a TQFP 100-pin package at commercial temperature and still air is as follows:

$$\text{Maximum Power Allowed} = \frac{\text{Max. junction temp. }(^\circ\text{C}) - \text{Max. ambient temp. }(^\circ\text{C})}{\theta_{ja}(^\circ\text{C/W})} = \frac{150^\circ\text{C} - 70^\circ\text{C}}{33.5^\circ\text{C/W}} = 2.39\text{W}$$

Package Type	Pin Count	θ_{jc}	θ_{ja}			Units
			Still Air	1.0 m/s 200 ft/min	2.5 m/s 500 ft/min	
Thin Quad Flat Pack (TQFP)	64	12.0	42.4	36.3	34.0	°C/W
Thin Quad Flat Pack (TQFP)	100	14.0	33.5	27.4	25.0	°C/W

Input Buffer Delays

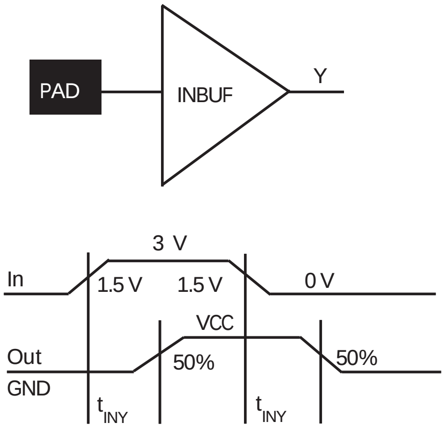


***Table 1-14* • Input Buffer Delays**

C-Cell Delays

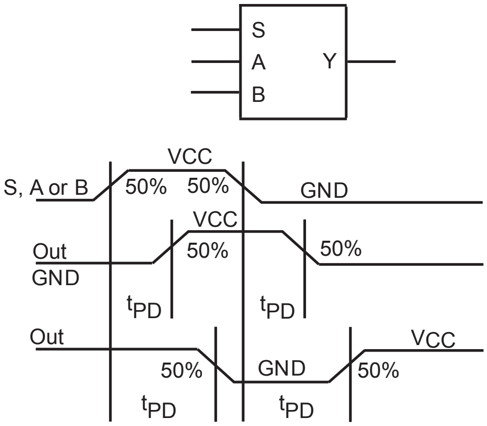


***Table 1-15* • C-Cell Delays**

Cell Timing Characteristics

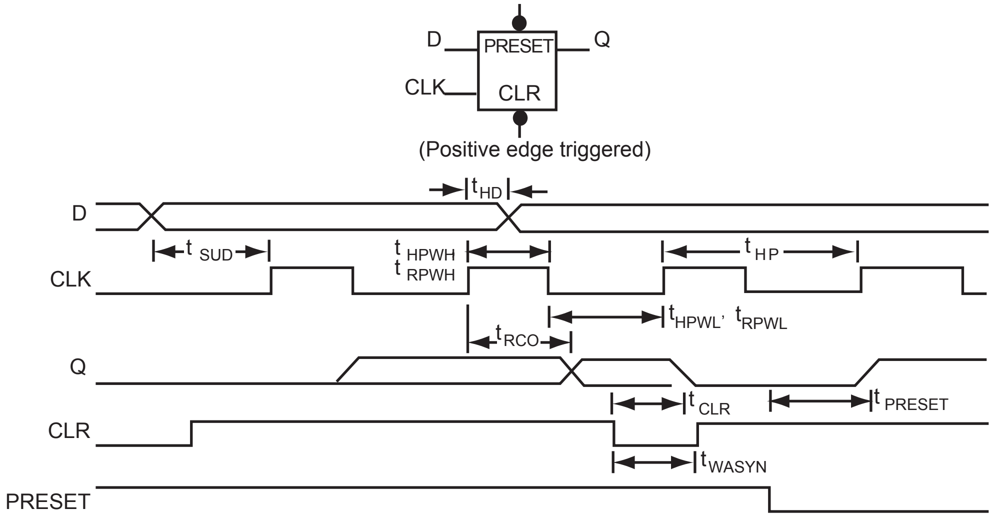


Figure 1-16 **• Flip-Flops**

Table 1-18 **• eX Family Timing Characteristics**
(Worst-Case Commercial Conditions VCCA = 2.3 V, VCCI = 4.75 V, T_J = 70°C)

		–P Speed		Std Speed		–F Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Dedicated (Hard-Wired) Array Clock Networks								
t_{HCKH}	Input LOW to HIGH (Pad to R-Cell Input)		1.1		1.6		2.3	ns
t_{HCKL}	Input HIGH to LOW (Pad to R-Cell Input)		1.1		1.6		2.3	ns
t_{HPWH}	Minimum Pulse Width HIGH	1.4		2.0		2.8		ns
t_{HPWL}	Minimum Pulse Width LOW	1.4		2.0		2.8		ns
t_{HCKSW}	Maximum Skew		<0.1		<0.1		<0.1	ns
t_{HP}	Minimum Period	2.8		4.0		5.6		ns
f_{HMAX}	Maximum Frequency		357		250		178	MHz
Routed Array Clock Networks								
t_{RCKH}	Input LOW to HIGH (Light Load) (Pad to R-Cell Input) MAX.		1.1		1.6		2.2	ns
t_{RCKL}	Input HIGH to LOW (Light Load) (Pad to R-Cell Input) MAX.		1.0		1.4		2.0	ns
t_{RCKH}	Input LOW to HIGH (50% Load) (Pad to R-Cell Input) MAX.		1.2		1.7		2.4	ns
t_{RCKL}	Input HIGH to LOW (50% Load) (Pad to R-Cell Input) MAX.		1.2		1.7		2.4	ns
t_{RCKH}	Input LOW to HIGH (100% Load) (Pad to R-Cell Input) MAX.		1.3		1.9		2.6	ns
t_{RCKL}	Input HIGH to LOW (100% Load) (Pad to R-Cell Input) MAX.		1.3		1.9		2.6	ns
t_{RPWH}	Min. Pulse Width HIGH	1.5		2.1		3.0		ns
t_{RPWL}	Min. Pulse Width LOW	1.5		2.1		3.0		ns
t_{RCKSW}*	Maximum Skew (Light Load)		0.2		0.3		0.4	ns
t_{RCKSW}*	Maximum Skew (50% Load)		0.1		0.2		0.3	ns
t_{RCKSW}*	Maximum Skew (100% Load)		0.1		0.1		0.2	ns

*Note: *Clock skew improves as the clock network becomes more heavily loaded.*

Table 1-19 **• eX Family Timing Characteristics**
(Worst-Case Commercial Conditions VCCA = 2.3V, VCCI = 2.3 V or 3.0V, T_J = 70°C)

		'–P' Speed		'Std' Speed		'–F' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Dedicated (Hard-Wired) Array Clock Networks								
t_{HCKH}	Input LOW to HIGH (Pad to R-Cell Input)		1.1		1.6		2.3	ns
t_{HCKL}	Input HIGH to LOW (Pad to R-Cell Input)		1.1		1.6		2.3	ns
t_{HPWH}	Minimum Pulse Width HIGH	1.4		2.0		2.8		ns
t_{HPWL}	Minimum Pulse Width LOW	1.4		2.0		2.8		ns
t_{HCKSW}	Maximum Skew		<0.1		<0.1		<0.1	ns
t_{HP}	Minimum Period	2.8		4.0		5.6		ns
f_{HMAX}	Maximum Frequency		357		250		178	MHz
Routed Array Clock Networks								
t_{RCKH}	Input LOW to HIGH (Light Load) (Pad to R-Cell Input) MAX.		1.0		1.4		2.0	ns
t_{RCKL}	Input HIGH to LOW (Light Load) (Pad to R-Cell Input) MAX.		1.0		1.4		2.0	ns
t_{RCKH}	Input LOW to HIGH (50% Load) (Pad to R-Cell Input) MAX.		1.2		1.7		2.4	ns
t_{RCKL}	Input HIGH to LOW (50% Load) (Pad to R-Cell Input) MAX.		1.2		1.7		2.4	ns
t_{RCKH}	Input LOW to HIGH (100% Load) (Pad to R-Cell Input) MAX.		1.4		2.0		2.8	ns
t_{RCKL}	Input HIGH to LOW (100% Load) (Pad to R-Cell Input) MAX.		1.4		2.0		2.8	ns
t_{RPWH}	Min. Pulse Width HIGH	1.4		2.0		2.8		ns
t_{RPWL}	Min. Pulse Width LOW	1.4		2.0		2.8		ns
t_{RCKSW}*	Maximum Skew (Light Load)		0.2		0.3		0.4	ns
t_{RCKSW}*	Maximum Skew (50% Load)		0.2		0.2		0.3	ns
t_{RCKSW}*	Maximum Skew (100% Load)		0.1		0.1		0.2	ns

*Note: *Clock skew improves as the clock network becomes more heavily loaded.*

***Table 1-20* • eX Family Timing Characteristics**
(Worst-Case Commercial Conditions VCCA = 2.3 V, T_J = 70°C)

		–P Speed		Std Speed		–F Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
2.5 V LVCMOS Output Module Timing[1] (VCCI = 2.3 V)								
t_{DLH}	Data-to-Pad LOW to HIGH		3.3		4.7		6.6	ns
t_{DHL}	Data-to-Pad HIGH to LOW		3.5		5.0		7.0	ns
t_{DHLS}	Data-to-Pad HIGH to LOW—Low Slew		11.6		16.6		23.2	ns
t_{ENZL}	Enable-to-Pad, Z to L		2.5		3.6		5.1	ns
t_{ENZLS}	Enable-to-Pad Z to L—Low Slew		11.8		16.9		23.7	ns
t_{ENZH}	Enable-to-Pad, Z to H		3.4		4.9		6.9	ns
t_{ENLZ}	Enable-to-Pad, L to Z		2.1		3.0		4.2	ns
t_{ENHZ}	Enable-to-Pad, H to Z		2.4		5.67		7.94	ns
d_{TLH}	Delta Delay vs. Load LOW to HIGH		0.034		0.046		0.066	ns/pF
d_{THL}	Delta Delay vs. Load HIGH to LOW		0.016		0.022		0.05	ns/pF
d_{THLS}	Delta Delay vs. Load HIGH to LOW—Low Slew		0.05		0.072		0.1	ns/pF
3.3 V LVTTL Output Module Timing[1] (VCCI = 3.0 V)								
t_{DLH}	Data-to-Pad LOW to HIGH		2.8		4.0		5.6	ns
t_{DHL}	Data-to-Pad HIGH to LOW		2.7		3.9		5.4	ns
t_{DHLS}	Data-to-Pad HIGH to LOW—Low Slew		9.7		13.9		19.5	ns
t_{ENZL}	Enable-to-Pad, Z to L		2.2		3.2		4.4	ns
t_{ENZLS}	Enable-to-Pad Z to L—Low Slew		9.7		13.9		19.6	ns
t_{ENZH}	Enable-to-Pad, Z to H		2.8		4.0		5.6	ns
t_{ENLZ}	Enable-to-Pad, L to Z		2.8		4.0		5.6	ns
t_{ENHZ}	Enable-to-Pad, H to Z		2.6		3.8		5.3	ns
d_{TLH}	Delta Delay vs. Load LOW to HIGH		0.02		0.03		0.046	ns/pF
d_{THL}	Delta Delay vs. Load HIGH to LOW		0.016		0.022		0.05	ns/pF
d_{THLS}	Delta Delay vs. Load HIGH to LOW—Low Slew		0.05		0.072		0.1	ns/pF
5.0 V TTL Output Module Timing* (VCCI = 4.75 V)								
t_{DLH}	Data-to-Pad LOW to HIGH		2.0		2.9		4.0	ns
t_{DHL}	Data-to-Pad HIGH to LOW		2.6		3.7		5.2	ns
t_{DHLS}	Data-to-Pad HIGH to LOW—Low Slew		6.8		9.7		13.6	ns
t_{ENZL}	Enable-to-Pad, Z to L		1.9		2.7		3.8	ns
t_{ENZLS}	Enable-to-Pad Z to L—Low Slew		6.8		9.8		13.7	ns
t_{ENZH}	Enable-to-Pad, Z to H		2.1		3.0		4.1	ns
t_{ENLZ}	Enable-to-Pad, L to Z		3.3		4.8		6.6	ns

Note: **Delays based on 35 pF loading.*

TMS **Test Mode Select**

The TMS pin controls the use of the IEEE 1149.1 Boundary scan pins (TCK, TDI, TDO, TRST). In flexible mode when the TMS pin is set LOW, the TCK, TDI, and TDO pins are boundary scan pins (refer to Table 1-4 on page 1-10). Once the boundary scan pins are in test mode, they will remain in that mode until the internal boundary scan state machine reaches the "logic reset" state. At this point, the boundary scan pins will be released and will function as regular I/O pins. The "logic reset" state is reached five TCK cycles after the TMS pin is set HIGH. In dedicated test mode, TMS functions as specified in the IEEE 1149.1 specifications.

TRST, I/O **Boundary Scan Reset Pin**

Once it is configured as the JTAG Reset pin, the TRST pin functions as an active-low input to asynchronously initialize or reset the boundary scan circuit. The TRST pin is equipped with an internal pull-up resistor. This pin functions as an I/O when the **Reserve JTAG Reset** Pin is not selected in the Designer software.

VCCI **Supply Voltage**

Supply voltage for I/Os.

VCCA **Supply Voltage**

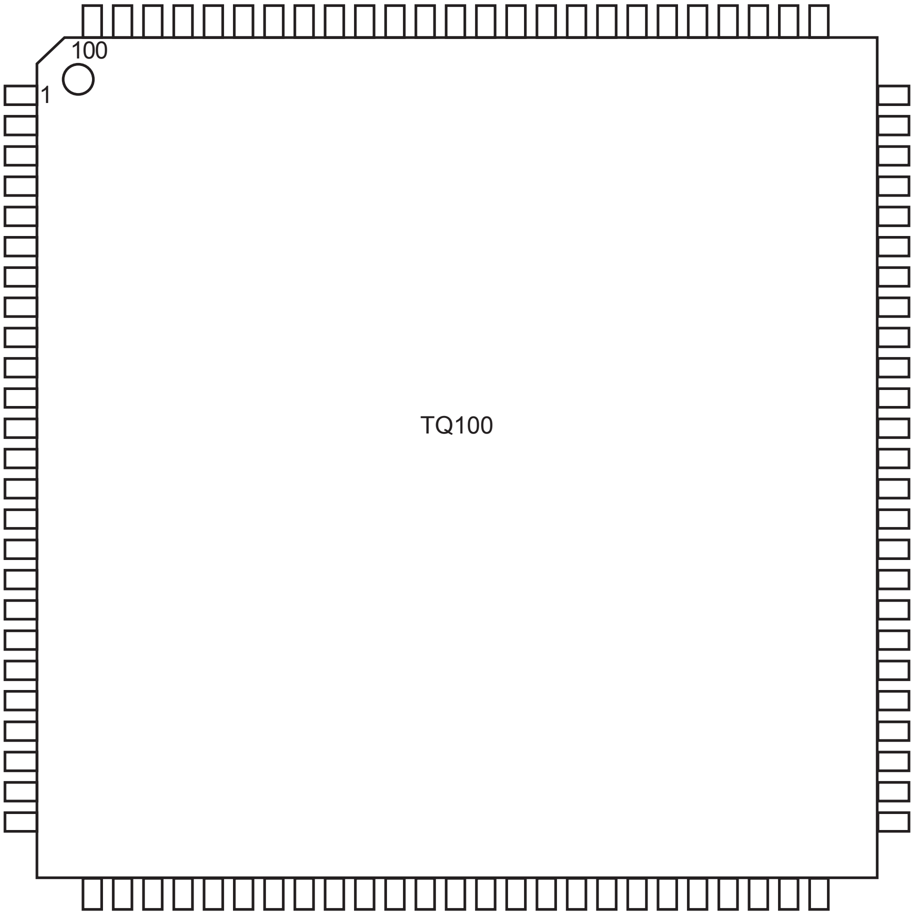
Supply voltage for Array.

TQ64		
Pin Number	eX64 Function	eX128 Function
1	GND	GND
2	TDI, I/O	TDI, I/O
3	I/O	I/O
4	TMS	TMS
5	GND	GND
6	VCCI	VCCI
7	I/O	I/O
8	I/O	I/O
9	NC	I/O
10	NC	I/O
11	TRST, I/O	TRST, I/O
12	I/O	I/O
13	NC	I/O
14	GND	GND
15	I/O	I/O
16	I/O	I/O
17	I/O	I/O
18	I/O	I/O
19	VCCI	VCCI
20	I/O	I/O
21	PRB, I/O	PRB, I/O
22	VCCA	VCCA
23	GND	GND
24	I/O	I/O
25	HCLK	HCLK
26	I/O	I/O
27	I/O	I/O
28	I/O	I/O
29	I/O	I/O
30	I/O	I/O
31	I/O	I/O
32	TDO, I/O	TDO, I/O

TQ64		
Pin Number	eX64 Function	eX128 Function
33	GND	GND
34	I/O	I/O
35	I/O	I/O
36	VCCA	VCCA
37	VCCI	VCCI
38	I/O	I/O
39	I/O	I/O
40	NC	I/O
41	NC	I/O
42	I/O	I/O
43	I/O	I/O
44	VCCA	VCCA
45*	GND/LP	GND/ LP
46	GND	GND
47	I/O	I/O
48	I/O	I/O
49	I/O	I/O
50	I/O	I/O
51	I/O	I/O
52	VCCI	VCCI
53	I/O	I/O
54	I/O	I/O
55	CLKA	CLKA
56	CLKB	CLKB
57	VCCA	VCCA
58	GND	GND
59	PRA, I/O	PRA, I/O
60	I/O	I/O
61	VCCI	VCCI
62	I/O	I/O
63	I/O	I/O
64	TCK, I/O	TCK, I/O

Note: **Please read the LP pin descriptions for restrictions on their use.*

TQ100



Note: For Package Manufacturing and Environmental information, visit Resource center at www.microsemi.com/soc/products/rescenter/package/index.html.

TQ100			
Pin Number	**eX64 Function**	**eX128 Function**	**eX256 Function**
1	GND	GND	GND
2	TDI, I/O	TDI, I/O	TDI, I/O
3	NC	NC	I/O
4	NC	NC	I/O
5	NC	NC	I/O
6	I/O	I/O	I/O
7	TMS	TMS	TMS
8	VCCI	VCCI	VCCI
9	GND	GND	GND
10	NC	I/O	I/O
11	NC	I/O	I/O
12	I/O	I/O	I/O
13	NC	I/O	I/O
14	I/O	I/O	I/O
15	NC	I/O	I/O
16	TRST, I/O	TRST, I/O	TRST, I/O
17	NC	I/O	I/O
18	I/O	I/O	I/O
19	NC	I/O	I/O
20	VCCI	VCCI	VCCI
21	I/O	I/O	I/O
22	NC	I/O	I/O
23	NC	NC	I/O
24	NC	NC	I/O
25	I/O	I/O	I/O
26	I/O	I/O	I/O
27	I/O	I/O	I/O
28	I/O	I/O	I/O
29	I/O	I/O	I/O
30	I/O	I/O	I/O
31	I/O	I/O	I/O
32	I/O	I/O	I/O
33	I/O	I/O	I/O
34	PRB, I/O	PRB, I/O	PRB, I/O
35	VCCA	VCCA	VCCA

TQ100			
Pin Number	**eX64 Function**	**eX128 Function**	**eX256 Function**
36	GND	GND	GND
37	NC	NC	NC
38	I/O	I/O	I/O
39	HCLK	HCLK	HCLK
40	I/O	I/O	I/O
41	I/O	I/O	I/O
42	I/O	I/O	I/O
43	I/O	I/O	I/O
44	VCCI	VCCI	VCCI
45	I/O	I/O	I/O
46	I/O	I/O	I/O
47	I/O	I/O	I/O
48	I/O	I/O	I/O
49	TDO, I/O	TDO, I/O	TDO, I/O
50	NC	I/O	I/O
51	GND	GND	GND
52	NC	NC	I/O
53	NC	NC	I/O
54	NC	NC	I/O
55	I/O	I/O	I/O
56	I/O	I/O	I/O
57	VCCA	VCCA	VCCA
58	VCCI	VCCI	VCCI
59	NC	I/O	I/O
60	I/O	I/O	I/O
61	NC	I/O	I/O
62	I/O	I/O	I/O
63	NC	I/O	I/O
64	I/O	I/O	I/O
65	NC	I/O	I/O
66	I/O	I/O	I/O
67	VCCA	VCCA	VCCA
68	GND/LP	GND/LP	GND/LP
69	GND	GND	GND
70	I/O	I/O	I/O

Note: **Please read the LP pin descriptions for restrictions on their use.*

Revision	Changes	Page
Advance v0.4	In the Product Profile, the Maximum User I/Os for eX64 was changed to 84.	1-I
	In the Product Profile table, the Maximum User I/Os for eX128 was changed to 100.	1-I
Advance v0.3	The Mechanical Drawings section has been removed from the data sheet. The mechanical drawings are now contained in a separate document, “Package Characteristics and Mechanical Drawings,” available on the Actel web site.	
	A new section describing "Clock Resources"has been added.	1-3
	A new table describing "I/O Features"has been added.	1-6
	The "Pin Description"section has been updated and clarified.	1-31
	The original Electrical Specifications table was separated into two tables (2.5V and 3.3/5.0V). In both tables, several different currents are specified for V_{OH} and V_{OL}.	Page 8 and 9
	A new table listing 2.5V low power specifications and associated power graphs were added.	page 9
	Pin functions for eX256 TQ100 have been added to the "TQ100"table.	2-3
	A CS49 pin drawing and pin assignment table including eX64 and eX128 pin functions have been added.	page 26
	A CS128 pin drawing and pin assignment table including eX64, eX128, and eX256 pin functions have been added.	pages 26-27
	A CS180 pin drawing and pin assignment table for eX256 pin functions have been added.	pages 27, 31
Advance v0.2	The following table note was added to the eX Timing Characteristics table for clarification: Clock skew improves as the clock network becomes more heavily loaded.	pages 14-15