Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	256
Total RAM Bits	-
Number of I/O	46
Number of Gates	6000
Voltage - Supply	2.3V ~ 2.7V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 125°C (TA)
Package / Case	64-LQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/ex128-tq64a

Routing Resources

Clusters and SuperClusters can be connected through the use of two innovative local routing resources called FastConnect and DirectConnect, which enable extremely fast and predictable interconnection of modules within Clusters and SuperClusters (Figure 1-4). This routing architecture also dramatically reduces the number of antifuses required to complete a circuit, ensuring the highest possible performance.

DirectConnect is a horizontal routing resource that provides connections from a C-cell to its neighboring R-cell in a given SuperCluster. DirectConnect uses a hard-wired signal path requiring no programmable interconnection to achieve its fast signal propagation time of less than 0.1 ns (–P speed grade).

FastConnect enables horizontal routing between any two logic modules within a given SuperCluster and vertical routing with the SuperCluster immediately below it. Only one programmable connection is used in a FastConnect path, delivering maximum pin-to-pin propagation of 0.3 ns (–P speed grade).

In addition to DirectConnect and FastConnect, the architecture makes use of two globally oriented routing resources known as segmented routing and high-drive routing. The segmented routing structure of Microsemi provides a variety of track lengths for extremely fast routing between SuperClusters. The exact combination of track lengths and antifuses within each path is chosen by the fully automatic place-and-route software to minimize signal propagation delays.

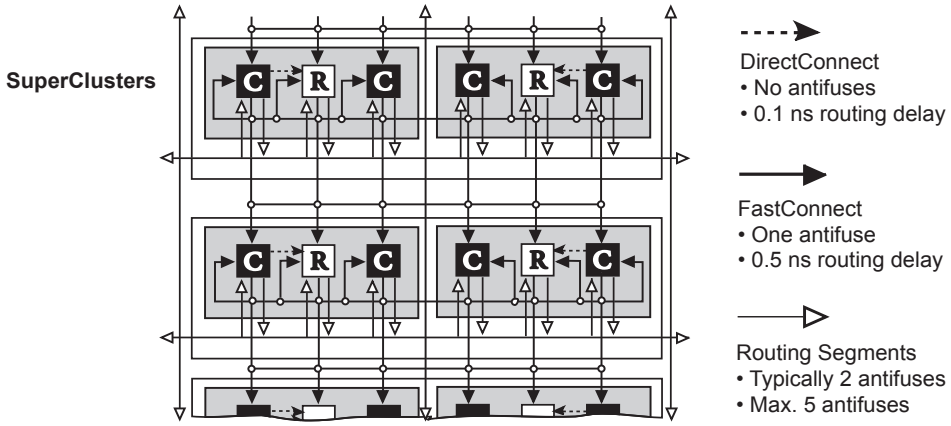


Figure 1-4 • **DirectConnect and FastConnect for SuperClusters**

Clock Resources

eX's high-drive routing structure provides three clock networks. The first clock, called HCLK, is hardwired from the HCLK buffer to the clock select MUX in each R-Cell. HCLK cannot be connected to combinational logic. This provides a fast propagation path for the clock signal, enabling the 3.9 ns clock-to-out (pad-to-pad) performance of the eX devices. The hard-wired clock is tuned to provide a clock skew of less than 0.1 ns worst case. If not used, the HCLK pin must be tied LOW or HIGH and must not be left floating. Figure 1-5 describes the clock circuit used for the constant load HCLK.

HCLK does not function until the fourth clock cycle each time the device is powered up to prevent false output levels due to any possible slow power-on-reset signal and fast start-up clock circuit. To activate HCLK from the first cycle, the TRST pin must be reserved in the Design software and the pin must be tied to GND on the board. (See the "TRST, I/O Boundary Scan Reset Pin" on page 1-32).

The remaining two clocks (CLKA, CLKB) are global routed clock networks that can be sourced from external pins or from internal logic signals (via the CLKINT routed clock buffer) within the eX device. CLKA and CLKB may be connected to sequential cells or to combinational logic. If CLKA or CLKB is sourced from internal logic signals, the external clock pin cannot be used for any other input and must be tied LOW or HIGH and must not float. Figure 1-6 describes the CLKA and CLKB circuit used in eX devices.

Table 1-1 describes the possible connections of the routed clock networks, CLKA and CLKB. Unused clock pins must not be left floating and must be tied to HIGH or LOW.

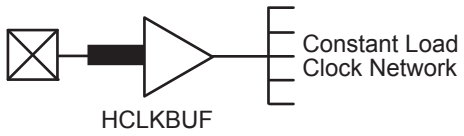


Figure 1-5 • **eX HCLK Clock Pad**

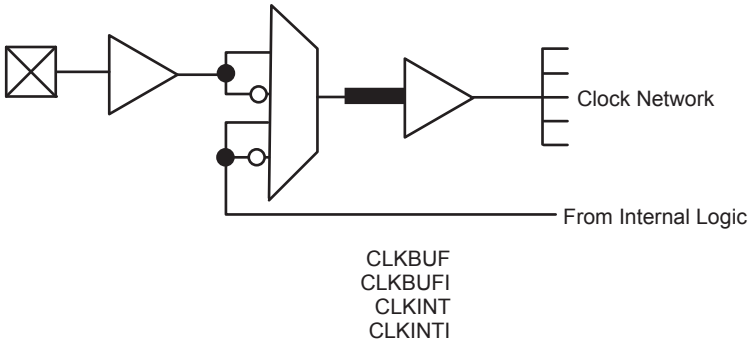


Figure 1-6 • **eX Routed Clock Buffer**

Table 1-1 • **Connections of Routed Clock Networks, CLKA and CLKB**

Module	Pins
C-Cell	A0, A1, B0 and B1
R-Cell	CLKA, CLKB, S0, S1, PSET, and CLR
I/O-Cell	EN

Table 1-2 describes the I/O features of eX devices. For more information on I/Os, refer to *Microsemi eX, SX-A, and RT54SX-S I/Os* application note.

Table 1-2 • **I/O Features**

Function	Description
Input Buffer Threshold Selection	• 5.0V TTL • 3.3V LVTTL • 2.5V LVCMOS2
Nominal Output Drive	• 5.0V TTL/CMOS • 3.3V LVTTL • 2.5V LVCMOS 2
Output Buffer	"Hot-Swap" Capability • I/O on an unpowered device does not sink current • Can be used for "cold sparing" Selectable on an individual I/O basis Individually selectable low-slew option
Power-Up	Individually selectable pull ups and pull downs during power-up (default is to power up in tristate) Enables deterministic power-up of device V_{CCA} and V_{CCI} can be powered in any order

The eX family supports mixed-voltage operation and is designed to tolerate 5.0 V inputs in each case.

A detailed description of the I/O pins in eX devices can be found in "Pin Description" on page 1-31.

Hot-Swapping

eX I/Os are configured to be hot-swappable. During power-up/down (or partial up/down), all I/Os are tristated, provided V_{CCA} ramps up within a diode drop of V_{CCI}. V_{CCA} and V_{CCI} do not have to be stable. during power-up/down, and they do not require a specific power-up or power-down sequence in order to avoid damage to the eX devices. In addition, all outputs can be programmed to have a weak resistor pull-up or pull-down for output tristate at power-up. After the eX device is plugged into an electrically active system, the device will not degrade the reliability of or cause damage to the host system. The device's output pins are driven to a high impedance state until normal chip operating conditions are reached. Please see the application note, *Microsemi SX-A and RT54SX-S Devices in Hot-Swap and Cold-Sparing Applications*, which also applies to the eX devices, for more information on hot swapping.

Power Requirements

Power consumption is extremely low for the eX family due to the low capacitance of the antifuse interconnects. The antifuse architecture does not require active circuitry to hold a charge (as do SRAM or EPROM), making it the lowest-power FPGA architecture available today.

Low Power Mode

The eX family has been designed with a Low Power Mode. This feature, activated with setting the special LP pin to HIGH for a period longer than 800 ns, is particularly useful for battery-operated systems where battery life is a primary concern. In this mode, the core of the device is turned off and the device consumes minimal power with low standby current. In addition, all input buffers are turned off, and all outputs and bidirectional buffers are tristated when the device enters this mode. Since the core of the device is turned off, the states of the registers are lost. The device must be re-initialized when returning to normal operating mode. I/Os can be driven during LP mode. For details, refer to the *Design for Low Power in Microsemi Antifuse FPGAs* application note under the section Using the LP Mode Pin on eX Devices. Clock pins should be driven either HIGH or LOW and should not float; otherwise, they will draw current and burn power. The device must be re-initialized when exiting LP mode.

To exit the LP mode, the LP pin must be driven LOW for over 200 µs to allow for the charge pumps to power-up and device initialization can begin.

Table 1-3 illustrates the standby current of eX devices in LP mode.

Table 1-3 • **Standby Power of eX Devices in LP Mode Typical Conditions, V_{CCA}, V_{CCI} = 2.5 V, T_J = 25° C**

Product	Low Power Standby Current	Units
eX64	100	µA
eX128	111	µA
eX256	134	µA

Table 1-5 describes the different configuration requirements of BST pins and their functionality in different modes.

Table 1-5 • **Boundary-Scan Pin Configurations and Functions**

Mode	Designer "Reserve JTAG" Selection	TAP Controller State
Dedicated (JTAG)	Checked	Any
Flexible (User I/O)	Unchecked	Test-Logic-Reset
Flexible (JTAG)	Unchecked	Any EXCEPT Test-Logic-Reset

TRST Pin

The TRST pin functions as a dedicated Boundary-Scan Reset pin when the **Reserve JTAG Test Reset** option is selected, as shown in Figure 1-12. An internal pull-up resistor is permanently enabled on the TRST pin in this mode. It is recommended to connect this pin to GND in normal operation to keep the JTAG state controller in the Test-Logic-Reset state. When JTAG is being used, it can be left floating or be driven HIGH.

When the **Reserve JTAG Test Reset** option is not selected, this pin will function as a regular I/O. If unused as an I/O in the design, it will be configured as a tristated output.

JTAG Instructions

Table 1-6 lists the supported instructions with the corresponding IR codes for eX devices.

Table 1-6 • **JTAG Instruction Code**

Instructions (IR4: IR0)	Binary Code
EXTEST	00000
SAMPLE / PRELOAD	00001
INTEST	00010
USERCODE	00011
IDCODE	00100
HIGHZ	01110
CLAMP	01111
Diagnostic	10000
BYPASS	11111
Reserved	All others

Table 1-7 lists the codes returned after executing the IDCODE instruction for eX devices. Note that bit 0 is always “1.” Bits 11-1 are always “02F”, which is Microsemi SoC Products Group's manufacturer code.

Table 1-7 • **IDCODE for eX Devices**

Device	Revision	Bits 31-28	Bits 27-12
eX64	0	8	40B2, 42B2
eX128	0	9	40B0, 42B0
eX256	0	9	40B5, 42B5
eX64	1	A	40B2, 42B2
eX128	1	B	40B0, 42B0
eX256	1	B	40B5, 42B5

Design Considerations

The TDI, TCK, TDO, PRA, and PRB pins should not be used as input or bidirectional ports. Since these pins are active during probing, critical signals input through these pins are not available while probing. In addition, the Security Fuse should not be programmed because doing so disables the probe circuitry. It is recommended to use a series 70Ω termination resistor on every probe connector (TDI, TCK, TMS, TDO, PRA, PRB). The 70Ω series termination is used to prevent data transmission corruption during probing and reading back the checksum.

Table 1-8 • **Device Configuration Options for Probe Capability (TRST pin reserved)**

JTAG Mode	TRST[1]	Security Fuse Programmed	PRA, PRB[2]	TDI, TCK, TDO[2]
Dedicated	LOW	No	User I/O[3]	Probing Unavailable
Flexible	LOW	No	User I/O[3]	User I/O[3]
Dedicated	HIGH	No	Probe Circuit Outputs	Probe Circuit Inputs
Flexible	HIGH	No	Probe Circuit Outputs	Probe Circuit Inputs
–	–	Yes	Probe Circuit Secured	Probe Circuit Secured

Notes:

1. *If TRST pin is not reserved, the device behaves according to TRST = HIGH in the table.*
2. *Avoid using the TDI, TCK, TDO, PRA, and PRB pins as input or bidirectional ports. Since these pins are active during probing, input signals will not pass through these pins and may cause contention.*
3. *If no user signal is assigned to these pins, they will behave as unused I/Os in this mode. Unused pins are automatically tristated by Microsemi Designer software.*

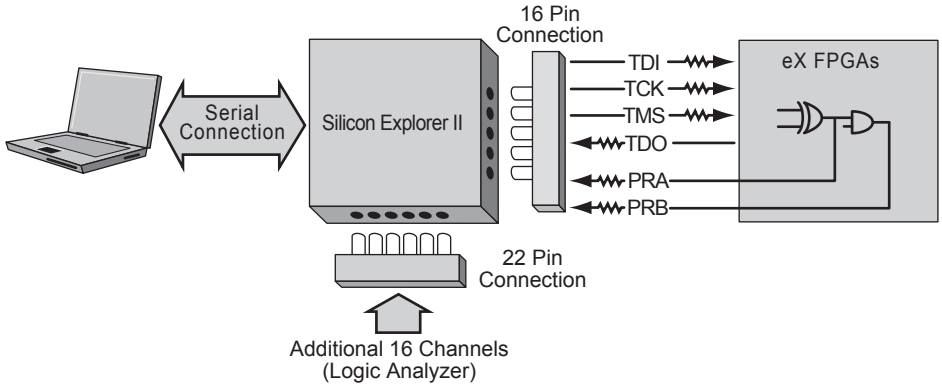


Figure 1-13 • **Silicon Explorer II Probe Setup**

Development Tool Support

The eX family of FPGAs is fully supported by both Libero® Integrated Design Environment and Designer FPGA Development software. Libero IDE is a design management environment that streamlines the design flow. Libero IDE provides an integrated design manager that seamlessly integrates design tools while guiding the user through the design flow, managing all design and log files, and passing necessary design data among tools. Additionally, Libero IDE allows users to integrate both schematic and HDL synthesis into a single flow and verify the entire design in a single environment. Libero IDE includes Synplify® for Microsemi from Synplicity®, ViewDraw for Microsemi from Mentor Graphics, ModelSim® HDL Simulator from Mentor Graphics®, WaveFormer Lite™ from SynaptiCAD™, and Designer software from Microsemi. Refer to the *Libero IDE flow* (located on Microsemi SoC Product Group's website) diagram for more information.

Designer software is a place-and-route tool and provides a comprehensive suite of backend support tools for FPGA development. The Designer software includes timing-driven place-and-route, and a world-class integrated static timing analyzer and constraints editor. With the Designer software, a user can lock his/her design pins before layout while minimally impacting the results of place-and-route. Additionally, the back-annotation flow is compatible with all the major simulators and the simulation results can be cross-probed with Silicon Explorer II, Microsemi integrated verification and logic analysis tool. Another tool included in the Designer software is the SmartGen core generator, which easily creates popular and commonly used logic functions for implementation into your schematic or HDL design. Microsemi's Designer software is compatible with the most popular FPGA design entry and verification tools from companies such as Mentor Graphics, Synplicity, Synopsys, and Cadence Design Systems. The Designer software is available for both the Windows and UNIX operating systems.

Related Documents

Datasheet

eX Automotive Family FPGAs
www.microsemi.com/soc/documents/eX_Auto_DS.pdf

Application Notes

Maximizing Logic Utilization in eX, SX and SX-A FPGA Devices Using CC Macros
www.microsemi.com/soc/documents/CC_Macro_AN.pdf
Implementation of Security in Microsemi Antifuse FPGAs
www.microsemi.com/soc/documents/Antifuse_Security_AN.pdf
Microsemi eX, SX-A, and RT54SX-S I/Os
www.microsemi.com/soc/documents/antifuseIO_AN.pdf
Microsemi SX-A and RT54SX-S Devices in Hot-Swap and Cold-Sparing Applications
www.microsemi.com/soc/documents/HotSwapColdSparing_AN.pdf
Design For Low Power in Microsemi Antifuse FPGAs
www.microsemi.com/soc/documents/Low_Power_AN.pdf
Programming Antifuse Devices
www.microsemi.com/soc/documents/AntifuseProgram_AN.pdf

User Guides

Silicon Sculptor II User's Guide
www.microsemi.com/soc/documents/SiliSculptII_Sculpt3_ug.pdf

Miscellaneous

Libero IDE flow
www.microsemi.com/soc/products/tools/libero/flow.html

2.5 V LVCMOS2 Electrical Specifications

Symbol	Parameter		Commercial Min.	Commercial Max.	Industrial Min.	Industrial Max.	Units
VOH	VCCI = MIN, VI = VIH or VIL	(IOH = –100 mA)	2.1		2.1		V
	VCCI = MIN, VI = VIH or VIL	(IOH = –1 mA)	2.0		2.0		V
	VCCI = MIN, VI = VIH or VIL	(IOH = –2 mA)	1.7		1.7		V
VOL	VCCI = MIN, VI = VIH or VIL	(IOL = 100 mA)		0.2		0.2	V
	VCCI = MIN, VI = VIH or VIL	(IOL = 1mA)		0.4		0.4	V
	VCCI = MIN,VI = VIH or VIL	(IOL = 2 mA)		0.7		0.7	V
VIL	Input Low Voltage, VOUT ≤ VOL (max.)		–0.3	0.7	-0.3	0.7	V
VIH	Input High Voltage, VOUT ≥ VOH (min.)		1.7	VCCI + 0.3	1.7	VCCI + 0.3	V
IIL/ IIH	Input Leakage Current, VIN = VCCI or GND		–10	10	–10	10	µA
IOZ	3-State Output Leakage Current, VOUT = VCCI or GND		–10	10	–10	10	µA
t_R, $t_{F1,2}$	Input Transition Time			10		10	ns
C_{IO}	I/O Capacitance			10		10	pF
ICC[3,4]	Standby Current			1.0		3.0	mA
IV Curve	Can be derived from the IBIS model at www.microsemi.com/soc/custsup/models/ibis.html.						

Notes:

1. *t_R is the transition time from 0.7 V to 1.7 V.*
2. *t_F is the transition time from 1.7 V to 0.7 V.*
3. *I_{CC} max Commercial –F = 5.0 mA*
4. *$I_{CC} = I_{CCI} + I_{CCA}$*

Power Dissipation

Power consumption for eX devices can be divided into two components: static and dynamic.

Static Power Component

The power due to standby current is typically a small component of the overall power. Typical standby current for eX devices is listed in the Table 1-11 on page 1-16. For example, the typical static power for eX128 at 3.3 V V_{CCI} is:

ICC * VCCA = 795 µA x 2.5 V = 1.99 mW

Dynamic Power Component

Power dissipation in CMOS devices is usually dominated by the dynamic power dissipation. This component is frequency-dependent and a function of the logic and the external I/O. Dynamic power dissipation results from charging internal chip capacitance due to PC board traces and load device inputs. An additional component of the dynamic power dissipation is the totem pole current in the CMOS transistor pairs. The net effect can be associated with an equivalent capacitance that can be combined with frequency and voltage to represent dynamic power dissipation.

Dynamic power dissipation = CEQ * $VCCA^2$ x F

where:

CEQ = Equivalent capacitance

F = switching frequency

Equivalent capacitance is calculated by measuring ICCA at a specified frequency and voltage for each circuit component of interest. Measurements have been made over a range of frequencies at a fixed value of VCC. Equivalent capacitance is frequency-independent, so the results can be used over a wide range of operating conditions. Equivalent capacitance values are shown below.

CEQ Values for eX Devices

Combinatorial modules (Ceqcm)	1.70 pF
Sequential modules (Ceqsm)	1.70 pF
Input buffers (Ceqi)	1.30 pF
Output buffers (Ceqo)	7.40 pF
Routed array clocks (Ceqcr)	1.05 pF

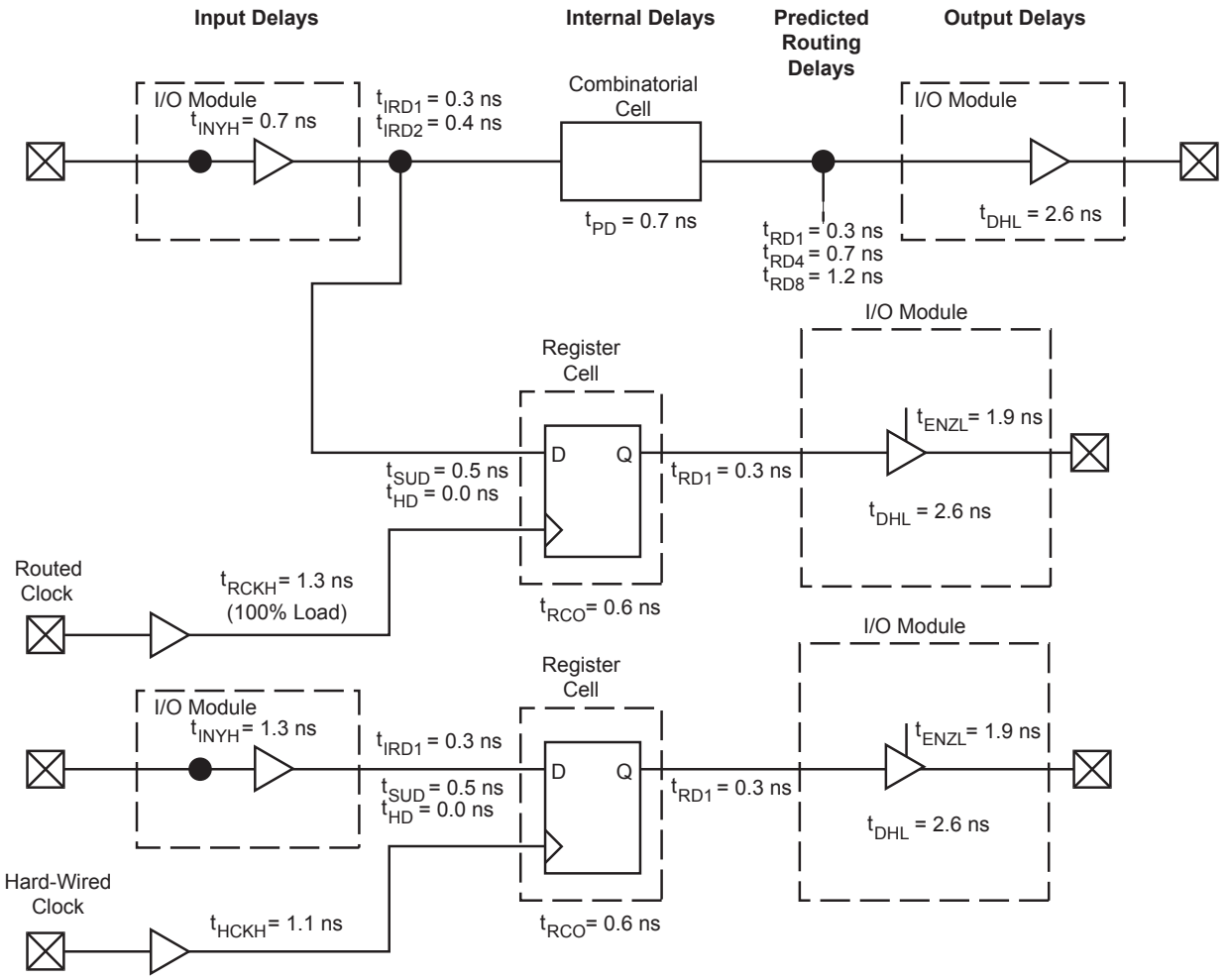
The variable and fixed capacitance of other device components must also be taken into account when estimating the dynamic power dissipation.

Table 1-12 shows the capacitance of the clock components of eX devices.

***Table 1-12* • Capacitance of Clock Components of eX Devices**

	eX64	eX128	eX256
Dedicated array clock – variable (Ceqhv)	0.85 pF	0.85 pF	0.85 pF
Dedicated array clock – fixed (Ceqhf)	18.00 pF	20.00 pF	25.00 pF
Routed array clock A (r1)	23.00 pF	28.00 pF	35.00 pF
Routed array clock B (r2)	23.00 pF	28.00 pF	35.00 pF

eX Timing Model



Note: Values shown for eX128–P, worst-case commercial conditions (5.0 V, 35 pF Pad Load).

Figure 1-14 • **eX Timing Model**

Hardwired Clock

External Setup = $t_{INYH} + t_{IRD1} + t_{SUD} – t_{HCKH}$

= 0.7 + 0.3 + 0.5 – 1.1 = 0.4 ns

Clock-to-Out (Pad-to-Pad), typical

= $t_{HCKH} + t_{RCO} + t_{RD1} + t_{DHL}$

= 1.1 + 0.6 + 0.3 + 2.6 = 4.6 ns

Routed Clock

External Setup = $t_{INYH} + t_{IRD2} + t_{SUD} – t_{RCKH}$

= 0.7 + 0.4 + 0.5 – 1.3= 0.3 ns

Clock-to-Out (Pad-to-Pad), typical

= $t_{RCKH} + t_{RCO} + t_{RD1} + t_{DHL}$

= 1.3+ 0.6 + 0.3 + 2.6 = 4.8 ns

eX Family Timing Characteristics

***Table 1-17* • eX Family Timing Characteristics**
(Worst-Case Commercial Conditions, VCCA = 2.3 V, T_J = 70°C)

		–P Speed		Std Speed		–F Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
C-Cell Propagation Delays[1]								
t_{PD}	Internal Array Module		0.7		1.0		1.4	ns
Predicted Routing Delays[2]								
t_{DC}	FO=1 Routing Delay, DirectConnect		0.1		0.1		0.2	ns
t_{FC}	FO=1 Routing Delay, FastConnect		0.3		0.5		0.7	ns
t_{RD1}	FO=1 Routing Delay		0.3		0.5		0.7	ns
t_{RD2}	FO=2 Routing Delay		0.4		0.6		0.8	ns
t_{RD3}	FO=3 Routing Delay		0.5		0.8		1.1	ns
t_{RD4}	FO=4 Routing Delay		0.7		1.0		1.3	ns
t_{RD8}	FO=8 Routing Delay		1.2		1.7		2.4	ns
t_{RD12}	FO=12 Routing Delay		1.7		2.5		3.5	ns
R-Cell Timing								
t_{RCO}	Sequential Clock-to-Q		0.6		0.9		1.3	ns
t_{CLR}	Asynchronous Clear-to-Q		0.6		0.8		1.2	ns
t_{PRESET}	Asynchronous Preset-to-Q		0.7		0.9		1.3	ns
t_{SUD}	Flip-Flop Data Input Set-Up	0.5		0.7		1.0		ns
t_{HD}	Flip-Flop Data Input Hold	0.0		0.0		0.0		ns
t_{WASYN}	Asynchronous Pulse Width	1.3		1.9		2.6		ns
$t_{RECASYN}$	Asynchronous Recovery Time	0.3		0.5		0.7		ns
t_{HASYN}	Asynchronous Hold Time	0.3		0.5		0.7		ns
2.5 V Input Module Propagation Delays								
t_{INYH}	Input Data Pad-to-Y HIGH		0.6		0.9		1.3	ns
t_{INYL}	Input Data Pad-to-Y LOW		0.8		1.1		1.5	ns
3.3 V Input Module Propagation Delays								
t_{INYH}	Input Data Pad-to-Y HIGH		0.7		1.0		1.4	ns
t_{INYL}	Input Data Pad-to-Y LOW		0.9		1.3		1.8	ns
5.0 V Input Module Propagation Delays								
t_{INYH}	Input Data Pad-to-Y HIGH		0.7		1.0		1.4	ns
t_{INYL}	Input Data Pad-to-Y LOW		0.9		1.3		1.8	ns
Input Module Predicted Routing Delays[2]								
t_{IRD1}	FO=1 Routing Delay		0.3		0.4		0.5	ns
t_{IRD2}	FO=2 Routing Delay		0.4		0.6		0.8	ns
t_{IRD3}	FO=3 Routing Delay		0.5		0.8		1.1	ns
t_{IRD4}	FO=4 Routing Delay		0.7		1.0		1.3	ns
t_{IRD8}	FO=8 Routing Delay		1.2		1.7		2.4	ns
t_{IRD12}	FO=12 Routing Delay		1.7		2.5		3.5	ns

Notes:

1. *For dual-module macros, use t_{PD} + t_{RD1} + t_{PDn}, t_{RCO} + t_{RD1} + t_{PDn} or t_{PD1} + t_{RD1} + t_{SUD}, whichever is appropriate.*
2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance.*

Table 1-19 • eX Family Timing Characteristics
(Worst-Case Commercial Conditions VCCA = 2.3V, VCCI = 2.3 V or 3.0V, T_J = 70°C)

		'–P' Speed		'Std' Speed		'–F' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Dedicated (Hard-Wired) Array Clock Networks								
t_{HCKH}	Input LOW to HIGH (Pad to R-Cell Input)		1.1		1.6		2.3	ns
t_{HCKL}	Input HIGH to LOW (Pad to R-Cell Input)		1.1		1.6		2.3	ns
t_{HPWH}	Minimum Pulse Width HIGH	1.4		2.0		2.8		ns
t_{HPWL}	Minimum Pulse Width LOW	1.4		2.0		2.8		ns
t_{HCKSW}	Maximum Skew		<0.1		<0.1		<0.1	ns
t_{HP}	Minimum Period	2.8		4.0		5.6		ns
f_{HMAX}	Maximum Frequency		357		250		178	MHz
Routed Array Clock Networks								
t_{RCKH}	Input LOW to HIGH (Light Load) (Pad to R-Cell Input) MAX.		1.0		1.4		2.0	ns
t_{RCKL}	Input HIGH to LOW (Light Load) (Pad to R-Cell Input) MAX.		1.0		1.4		2.0	ns
t_{RCKH}	Input LOW to HIGH (50% Load) (Pad to R-Cell Input) MAX.		1.2		1.7		2.4	ns
t_{RCKL}	Input HIGH to LOW (50% Load) (Pad to R-Cell Input) MAX.		1.2		1.7		2.4	ns
t_{RCKH}	Input LOW to HIGH (100% Load) (Pad to R-Cell Input) MAX.		1.4		2.0		2.8	ns
t_{RCKL}	Input HIGH to LOW (100% Load) (Pad to R-Cell Input) MAX.		1.4		2.0		2.8	ns
t_{RPWH}	Min. Pulse Width HIGH	1.4		2.0		2.8		ns
t_{RPWL}	Min. Pulse Width LOW	1.4		2.0		2.8		ns
t_{RCKSW}*	Maximum Skew (Light Load)		0.2		0.3		0.4	ns
t_{RCKSW}*	Maximum Skew (50% Load)		0.2		0.2		0.3	ns
t_{RCKSW}*	Maximum Skew (100% Load)		0.1		0.1		0.2	ns

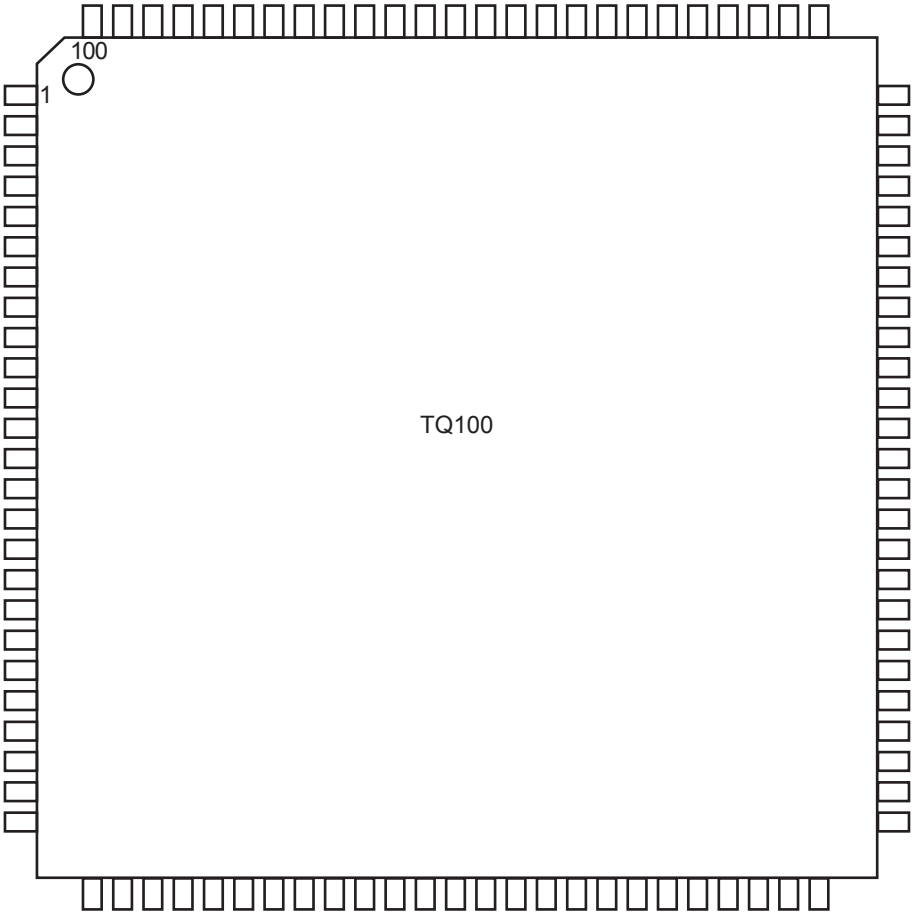
*Note: *Clock skew improves as the clock network becomes more heavily loaded.*

Table 1-20 • **eX Family Timing Characteristics**
(Worst-Case Commercial Conditions VCCA = 2.3 V, T_J = 70°C)

		–P Speed		Std Speed		–F Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
2.5 V LVCMOS Output Module Timing[1] (VCCI = 2.3 V)								
t_{DLH}	Data-to-Pad LOW to HIGH		3.3		4.7		6.6	ns
t_{DHL}	Data-to-Pad HIGH to LOW		3.5		5.0		7.0	ns
t_{DHLS}	Data-to-Pad HIGH to LOW—Low Slew		11.6		16.6		23.2	ns
t_{ENZL}	Enable-to-Pad, Z to L		2.5		3.6		5.1	ns
t_{ENZLS}	Enable-to-Pad Z to L—Low Slew		11.8		16.9		23.7	ns
t_{ENZH}	Enable-to-Pad, Z to H		3.4		4.9		6.9	ns
t_{ENLZ}	Enable-to-Pad, L to Z		2.1		3.0		4.2	ns
t_{ENHZ}	Enable-to-Pad, H to Z		2.4		5.67		7.94	ns
d_{TLH}	Delta Delay vs. Load LOW to HIGH		0.034		0.046		0.066	ns/pF
d_{THL}	Delta Delay vs. Load HIGH to LOW		0.016		0.022		0.05	ns/pF
d_{THLS}	Delta Delay vs. Load HIGH to LOW—Low Slew		0.05		0.072		0.1	ns/pF
3.3 V LVTTL Output Module Timing[1] (VCCI = 3.0 V)								
t_{DLH}	Data-to-Pad LOW to HIGH		2.8		4.0		5.6	ns
t_{DHL}	Data-to-Pad HIGH to LOW		2.7		3.9		5.4	ns
t_{DHLS}	Data-to-Pad HIGH to LOW—Low Slew		9.7		13.9		19.5	ns
t_{ENZL}	Enable-to-Pad, Z to L		2.2		3.2		4.4	ns
t_{ENZLS}	Enable-to-Pad Z to L—Low Slew		9.7		13.9		19.6	ns
t_{ENZH}	Enable-to-Pad, Z to H		2.8		4.0		5.6	ns
t_{ENLZ}	Enable-to-Pad, L to Z		2.8		4.0		5.6	ns
t_{ENHZ}	Enable-to-Pad, H to Z		2.6		3.8		5.3	ns
d_{TLH}	Delta Delay vs. Load LOW to HIGH		0.02		0.03		0.046	ns/pF
d_{THL}	Delta Delay vs. Load HIGH to LOW		0.016		0.022		0.05	ns/pF
d_{THLS}	Delta Delay vs. Load HIGH to LOW—Low Slew		0.05		0.072		0.1	ns/pF
5.0 V TTL Output Module Timing* (VCCI = 4.75 V)								
t_{DLH}	Data-to-Pad LOW to HIGH		2.0		2.9		4.0	ns
t_{DHL}	Data-to-Pad HIGH to LOW		2.6		3.7		5.2	ns
t_{DHLS}	Data-to-Pad HIGH to LOW—Low Slew		6.8		9.7		13.6	ns
t_{ENZL}	Enable-to-Pad, Z to L		1.9		2.7		3.8	ns
t_{ENZLS}	Enable-to-Pad Z to L—Low Slew		6.8		9.8		13.7	ns
t_{ENZH}	Enable-to-Pad, Z to H		2.1		3.0		4.1	ns
t_{ENLZ}	Enable-to-Pad, L to Z		3.3		4.8		6.6	ns

*Note: *Delays based on 35 pF loading.*

TQ100



Note: For Package Manufacturing and Environmental information, visit Resource center at www.microsemi.com/soc/products/rescenter/package/index.html.

TQ100			
Pin Number	eX64 Function	eX128 Function	eX256 Function
1	GND	GND	GND
2	TDI, I/O	TDI, I/O	TDI, I/O
3	NC	NC	I/O
4	NC	NC	I/O
5	NC	NC	I/O
6	I/O	I/O	I/O
7	TMS	TMS	TMS
8	VCCI	VCCI	VCCI
9	GND	GND	GND
10	NC	I/O	I/O
11	NC	I/O	I/O
12	I/O	I/O	I/O
13	NC	I/O	I/O
14	I/O	I/O	I/O
15	NC	I/O	I/O
16	TRST, I/O	TRST, I/O	TRST, I/O
17	NC	I/O	I/O
18	I/O	I/O	I/O
19	NC	I/O	I/O
20	VCCI	VCCI	VCCI
21	I/O	I/O	I/O
22	NC	I/O	I/O
23	NC	NC	I/O
24	NC	NC	I/O
25	I/O	I/O	I/O
26	I/O	I/O	I/O
27	I/O	I/O	I/O
28	I/O	I/O	I/O
29	I/O	I/O	I/O
30	I/O	I/O	I/O
31	I/O	I/O	I/O
32	I/O	I/O	I/O
33	I/O	I/O	I/O
34	PRB, I/O	PRB, I/O	PRB, I/O
35	VCCA	VCCA	VCCA

TQ100			
Pin Number	eX64 Function	eX128 Function	eX256 Function
36	GND	GND	GND
37	NC	NC	NC
38	I/O	I/O	I/O
39	HCLK	HCLK	HCLK
40	I/O	I/O	I/O
41	I/O	I/O	I/O
42	I/O	I/O	I/O
43	I/O	I/O	I/O
44	VCCI	VCCI	VCCI
45	I/O	I/O	I/O
46	I/O	I/O	I/O
47	I/O	I/O	I/O
48	I/O	I/O	I/O
49	TDO, I/O	TDO, I/O	TDO, I/O
50	NC	I/O	I/O
51	GND	GND	GND
52	NC	NC	I/O
53	NC	NC	I/O
54	NC	NC	I/O
55	I/O	I/O	I/O
56	I/O	I/O	I/O
57	VCCA	VCCA	VCCA
58	VCCI	VCCI	VCCI
59	NC	I/O	I/O
60	I/O	I/O	I/O
61	NC	I/O	I/O
62	I/O	I/O	I/O
63	NC	I/O	I/O
64	I/O	I/O	I/O
65	NC	I/O	I/O
66	I/O	I/O	I/O
67	VCCA	VCCA	VCCA
68	GND/LP	GND/LP	GND/LP
69	GND	GND	GND
70	I/O	I/O	I/O

*Note: *Please read the LP pin descriptions for restrictions on their use.*

TQ100			
Pin Number	**eX64 Function**	**eX128 Function**	**eX256 Function**
71	I/O	I/O	I/O
72	NC	I/O	I/O
73	NC	NC	I/O
74	NC	NC	I/O
75	NC	NC	I/O
76	NC	I/O	I/O
77	I/O	I/O	I/O
78	I/O	I/O	I/O
79	I/O	I/O	I/O
80	I/O	I/O	I/O
81	I/O	I/O	I/O
82	VCCI	VCCI	VCCI
83	I/O	I/O	I/O
84	I/O	I/O	I/O
85	I/O	I/O	I/O
86	I/O	I/O	I/O
87	CLKA	CLKA	CLKA
88	CLKB	CLKB	CLKB
89	NC	NC	NC
90	VCCA	VCCA	VCCA
91	GND	GND	GND
92	PRA, I/O	PRA, I/O	PRA, I/O
93	I/O	I/O	I/O
94	I/O	I/O	I/O
95	I/O	I/O	I/O
96	I/O	I/O	I/O
97	I/O	I/O	I/O
98	I/O	I/O	I/O
99	I/O	I/O	I/O
100	TCK, I/O	TCK, I/O	TCK, I/O

*Note: *Please read the LP pin descriptions for restrictions on their use.*

Revision	Changes	Page
Advance v0.4	In the Product Profile, the Maximum User I/Os for eX64 was changed to 84.	1-I
	In the Product Profile table, the Maximum User I/Os for eX128 was changed to 100.	1-I
Advance v0.3	The Mechanical Drawings section has been removed from the data sheet. The mechanical drawings are now contained in a separate document, “Package Characteristics and Mechanical Drawings,” available on the Actel web site.	
	A new section describing "Clock Resources"has been added.	1-3
	A new table describing "I/O Features"has been added.	1-6
	The "Pin Description"section has been updated and clarified.	1-31
	The original Electrical Specifications table was separated into two tables (2.5V and 3.3/5.0V). In both tables, several different currents are specified for V_{OH} and V_{OL}.	Page 8 and 9
	A new table listing 2.5V low power specifications and associated power graphs were added.	page 9
	Pin functions for eX256 TQ100 have been added to the "TQ100"table.	2-3
	A CS49 pin drawing and pin assignment table including eX64 and eX128 pin functions have been added.	page 26
	A CS128 pin drawing and pin assignment table including eX64, eX128, and eX256 pin functions have been added.	pages 26-27
	A CS180 pin drawing and pin assignment table for eX256 pin functions have been added.	pages 27, 31
Advance v0.2	The following table note was added to the eX Timing Characteristics table for clarification: Clock skew improves as the clock network becomes more heavily loaded.	pages 14-15

Datasheet Categories

Categories

In order to provide the latest information to designers, some datasheet parameters are published before data has been fully characterized from silicon devices. The data provided for a given device, as highlighted in the "eX Device Status" table on page II, is designated as either "Product Brief," "Advance," "Preliminary," or "Production." The definitions of these categories are as follows:

Product Brief

The product brief is a summarized version of a datasheet (advance or production) and contains general product information. This document gives an overview of specific device and family information.

Advance

This version contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production. This label only applies to the DC and Switching Characteristics chapter of the datasheet and will only be used when the data has not been fully characterized.

Preliminary

The datasheet contains information based on simulation and/or initial characterization. The information is believed to be correct, but changes are possible.

Production

This version contains information that is considered to be final.

Export Administration Regulations (EAR)

The product described in this datasheet is subject to the Export Administration Regulations (EAR). They could require an approved export license prior to export from the United States. An export includes release of product or disclosure of technology to a foreign national inside or outside the United States.