Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	512
Total RAM Bits	-
Number of I/O	81
Number of Gates	12000
Voltage - Supply	2.3V ~ 2.7V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	100-LQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/ex256-ftq100

Temperature Grade Offerings

Device\ Package	TQ64	TQ100
eX64	C, I, A	C, I, A
eX128	C, I, A	C, I, A
eX256	C, I, A	C, I, A

Note: C = Commercial
I = Industrial
A = Automotive

Speed Grade and Temperature Grade Matrix

	–F	Std	–P
C	✓	✓	✓
I		✓	✓
A		✓	

Note: P = Approximately 30% faster than Standard
–F = Approximately 40% slower than Standard
Refer to the eX Automotive Family FPGAs datasheet for details on automotive temperature offerings.

Contact your local Microsemi representative for device availability.

Table of Contents

Table 1-1 describes the possible connections of the routed clock networks, CLKA and CLKB. Unused clock pins must not be left floating and must be tied to HIGH or LOW.

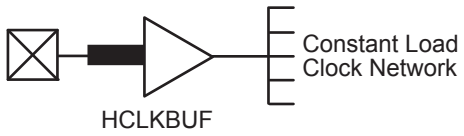


Figure 1-5 • **eX HCLK Clock Pad**

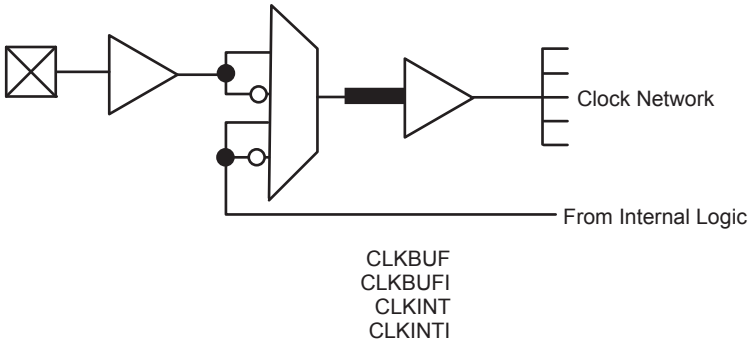


Figure 1-6 • **eX Routed Clock Buffer**

Table 1-1 • **Connections of Routed Clock Networks, CLKA and CLKB**

Module	Pins
C-Cell	A0, A1, B0 and B1
R-Cell	CLKA, CLKB, S0, S1, PSET, and CLR
I/O-Cell	EN

To exit the LP mode, the LP pin must be driven LOW for over 200 µs to allow for the charge pumps to power-up and device initialization can begin.

Table 1-3 illustrates the standby current of eX devices in LP mode.

Table 1-3 • **Standby Power of eX Devices in LP Mode Typical Conditions, V_{CCA}, V_{CCI} = 2.5 V, T_J = 25° C**

Product	Low Power Standby Current	Units
eX64	100	µA
eX128	111	µA
eX256	134	µA

Programming

Device programming is supported through Silicon Sculptor series of programmers. In particular, Silicon Sculptor II is a compact, robust, single-site and multi-site device programmer for the PC.

With standalone software, Silicon Sculptor II allows concurrent programming of multiple units from the same PC, ensuring the fastest programming times possible. Each fuse is subsequently verified by Silicon Sculptor II to insure correct programming. In addition, integrity tests ensure that no extra fuses are programmed. Silicon Sculptor II also provides extensive hardware self-testing capability.

The procedure for programming an eX device using Silicon Sculptor II is as follows:

1. Load the *.AFM file
2. Select the device to be programmed
3. Begin programming

When the design is ready to go to production, Microsemi offers device volume-programming services either through distribution partners or via in-house programming from the factory.

For more details on programming eX devices, please refer to the *Programming Antifuse Devices* application note and the *Silicon Sculptor II User's Guide*.

Probing Capabilities

eX devices provide internal probing capability that is accessed with the JTAG pins. The Silicon Explorer II Diagnostic hardware is used to control the TDI, TCK, TMS and TDO pins to select the desired nets for debugging. The user simply assigns the selected internal nets in the Silicon Explorer II software to the PRA/PRB output pins for observation. Probing functionality is activated when the BST pins are in JTAG mode and the TRST pin is driven HIGH or left floating. If the TRST pin is held LOW, the TAP controller will remain in the Test-Logic-Reset state so no probing can be performed. The Silicon Explorer II automatically places the device into JTAG mode, but the user must drive the TRST pin HIGH or allow the internal pull-up resistor to pull TRST HIGH.

When you select the **Reserve Probe Pin** box, as shown in Figure 1-12 on page 1-10, the layout tool reserves the PRA and PRB pins as dedicated outputs for probing. This reserve option is merely a guideline. If the Layout tool requires that the PRA and PRB pins be user I/Os to achieve successful layout, the tool will use these pins for user I/Os. If you assign user I/Os to the PRA and PRB pins and select the **Reserve Probe Pin** option, Designer Layout will override the "Reserve Probe Pin" option and place your user I/Os on those pins.

To allow for probing capabilities, the security fuse must not be programmed. Programming the security fuse will disable the probe circuitry. Table 1-8 on page 1-13 summarizes the possible device configurations for probing once the device leaves the Test-Logic-Reset JTAG state.

Silicon Explorer II Probe

Silicon Explorer II is an integrated hardware and software solution that, in conjunction with Microsemi Designer software tools, allow users to examine any of the internal nets of the device while it is operating in a prototype or a production system. The user can probe into an eX device via the PRA and PRB pins without changing the placement and routing of the design and without using any additional resources. Silicon Explorer II's noninvasive method does not alter timing or loading effects, thus shortening the debug cycle.

Silicon Explorer II does not require re-layout or additional MUXes to bring signals out to an external pin, which is necessary when using programmable logic devices from other suppliers.

Silicon Explorer II samples data at 100 MHz (asynchronous) or 66 MHz (synchronous). Silicon Explorer II attaches to a PC's standard COM port, turning the PC into a fully functional 18-channel logic analyzer. Silicon Explorer II allows designers to complete the design verification process at their desks and reduces verification time from several hours per cycle to a few seconds.

The Silicon Explorer II tool uses the boundary scan ports (TDI, TCK, TMS and TDO) to select the desired nets for verification. The selected internal nets are assigned to the PRA/PRB pins for observation. Figure 1-13 on page 1-13 illustrates the interconnection between Silicon Explorer II and the eX device to perform in-circuit verification.

Design Considerations

The TDI, TCK, TDO, PRA, and PRB pins should not be used as input or bidirectional ports. Since these pins are active during probing, critical signals input through these pins are not available while probing. In addition, the Security Fuse should not be programmed because doing so disables the probe circuitry. It is recommended to use a series 70Ω termination resistor on every probe connector (TDI, TCK, TMS, TDO, PRA, PRB). The 70Ω series termination is used to prevent data transmission corruption during probing and reading back the checksum.

Table 1-8 • **Device Configuration Options for Probe Capability (TRST pin reserved)**

JTAG Mode	TRST[1]	Security Fuse Programmed	PRA, PRB[2]	TDI, TCK, TDO[2]
Dedicated	LOW	No	User I/O[3]	Probing Unavailable
Flexible	LOW	No	User I/O[3]	User I/O[3]
Dedicated	HIGH	No	Probe Circuit Outputs	Probe Circuit Inputs
Flexible	HIGH	No	Probe Circuit Outputs	Probe Circuit Inputs
–	–	Yes	Probe Circuit Secured	Probe Circuit Secured

Notes:

1. *If TRST pin is not reserved, the device behaves according to TRST = HIGH in the table.*
2. *Avoid using the TDI, TCK, TDO, PRA, and PRB pins as input or bidirectional ports. Since these pins are active during probing, input signals will not pass through these pins and may cause contention.*
3. *If no user signal is assigned to these pins, they will behave as unused I/Os in this mode. Unused pins are automatically tristated by Microsemi Designer software.*

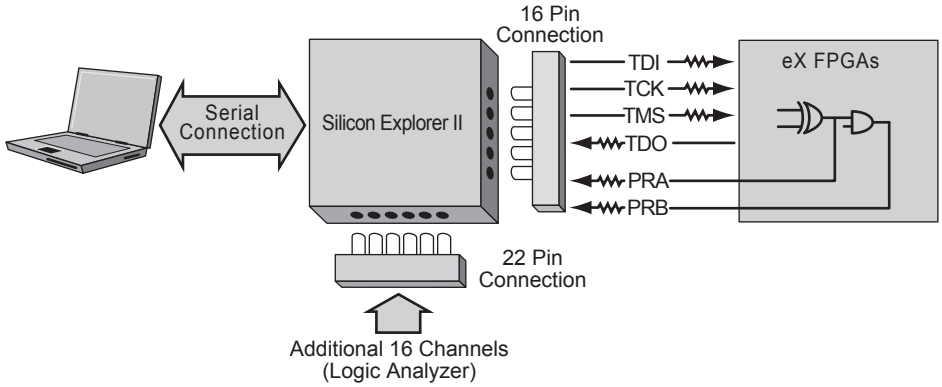


Figure 1-13 • **Silicon Explorer II Probe Setup**

Development Tool Support

The eX family of FPGAs is fully supported by both Libero® Integrated Design Environment and Designer FPGA Development software. Libero IDE is a design management environment that streamlines the design flow. Libero IDE provides an integrated design manager that seamlessly integrates design tools while guiding the user through the design flow, managing all design and log files, and passing necessary design data among tools. Additionally, Libero IDE allows users to integrate both schematic and HDL synthesis into a single flow and verify the entire design in a single environment. Libero IDE includes Synplify® for Microsemi from Synplicity®, ViewDraw for Microsemi from Mentor Graphics, ModelSim® HDL Simulator from Mentor Graphics®, WaveFormer Lite™ from SynaptiCAD™, and Designer software from Microsemi. Refer to the *Libero IDE flow* (located on Microsemi SoC Product Group's website) diagram for more information.

Designer software is a place-and-route tool and provides a comprehensive suite of backend support tools for FPGA development. The Designer software includes timing-driven place-and-route, and a world-class integrated static timing analyzer and constraints editor. With the Designer software, a user can lock his/her design pins before layout while minimally impacting the results of place-and-route. Additionally, the back-annotation flow is compatible with all the major simulators and the simulation results can be cross-probed with Silicon Explorer II, Microsemi integrated verification and logic analysis tool. Another tool included in the Designer software is the SmartGen core generator, which easily creates popular and commonly used logic functions for implementation into your schematic or HDL design. Microsemi's Designer software is compatible with the most popular FPGA design entry and verification tools from companies such as Mentor Graphics, Synplicity, Synopsys, and Cadence Design Systems. The Designer software is available for both the Windows and UNIX operating systems.

2.5 V / 3.3 V /5.0 V Operating Conditions

Table 1-9 • **Absolute Maximum Ratings***

Symbol	Parameter	Limits	Units
VCCI	DC Supply Voltage for I/Os	–0.3 to +6.0	V
VCCA	DC Supply Voltage for Array	–0.3 to +3.0	V
VI	Input Voltage	–0.5 to +5.75	V
VO	Output Voltage	–0.5 to +V_{CCI}	V
T_{STG}	Storage Temperature	–65 to +150	°C

*Note: *Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Devices should not be operated outside the Recommended Operating Conditions.*

Table 1-10 • **Recommended Operating Conditions**

Parameter	Commercial	Industrial	Units
Temperature Range*	0 to +70	–40 to +85	°C
2.5V Power Supply Range (VCCA, VCCI)	2.3 to 2.7	2.3 to 2.7	V
3.3V Power Supply Range (VCCI)	3.0 to 3.6	3.0 to 3.6	V
5.0V Power Supply Range (VCCI)	4.75 to 5.25	4.75 to 5.25	V

*Note: *Ambient temperature (T_A).*

Table 1-11 • **Typical eX Standby Current at 25°C**

Product	VCCA= 2.5 V VCCI = 2.5 V	VCCA = 2.5 V VCCI = 3.3 V	VCCA = 2.5 V VCCI = 5.0 V
eX64	397 µA	497 µA	700 µA
eX128	696 µA	795 µA	1,000 µA
eX256	698 µA	796 µA	2,000 µA

2.5 V LVCMOS2 Electrical Specifications

Symbol	Parameter		Commercial Min.	Commercial Max.	Industrial Min.	Industrial Max.	Units
VOH	VCCI = MIN, VI = VIH or VIL	(IOH = –100 mA)	2.1		2.1		V
	VCCI = MIN, VI = VIH or VIL	(IOH = –1 mA)	2.0		2.0		V
	VCCI = MIN, VI = VIH or VIL	(IOH = –2 mA)	1.7		1.7		V
VOL	VCCI = MIN, VI = VIH or VIL	(IOL = 100 mA)		0.2		0.2	V
	VCCI = MIN, VI = VIH or VIL	(IOL = 1mA)		0.4		0.4	V
	VCCI = MIN,VI = VIH or VIL	(IOL = 2 mA)		0.7		0.7	V
VIL	Input Low Voltage, VOUT ≤ VOL (max.)		–0.3	0.7	-0.3	0.7	V
VIH	Input High Voltage, VOUT ≥ VOH (min.)		1.7	VCCI + 0.3	1.7	VCCI + 0.3	V
IIL/ IIH	Input Leakage Current, VIN = VCCI or GND		–10	10	–10	10	µA
IOZ	3-State Output Leakage Current, VOUT = VCCI or GND		–10	10	–10	10	µA
t_R, $t_{F1,2}$	Input Transition Time			10		10	ns
C_{IO}	I/O Capacitance			10		10	pF
ICC[3,4]	Standby Current			1.0		3.0	mA
IV Curve	Can be derived from the IBIS model at www.microsemi.com/soc/custsup/models/ibis.html.						

Notes:

1. *t_R is the transition time from 0.7 V to 1.7 V.*
2. *t_F is the transition time from 1.7 V to 0.7 V.*
3. *I_{CC} max Commercial –F = 5.0 mA*
4. *$I_{CC} = I_{CCI} + I_{CCA}$*

Power Dissipation

Power consumption for eX devices can be divided into two components: static and dynamic.

Static Power Component

The power due to standby current is typically a small component of the overall power. Typical standby current for eX devices is listed in the Table 1-11 on page 1-16. For example, the typical static power for eX128 at 3.3 V V_{CCI} is:

ICC * VCCA = 795 µA x 2.5 V = 1.99 mW

Dynamic Power Component

Power dissipation in CMOS devices is usually dominated by the dynamic power dissipation. This component is frequency-dependent and a function of the logic and the external I/O. Dynamic power dissipation results from charging internal chip capacitance due to PC board traces and load device inputs. An additional component of the dynamic power dissipation is the totem pole current in the CMOS transistor pairs. The net effect can be associated with an equivalent capacitance that can be combined with frequency and voltage to represent dynamic power dissipation.

Dynamic power dissipation = CEQ * $VCCA^2$ x F

where:

CEQ = Equivalent capacitance

F = switching frequency

Equivalent capacitance is calculated by measuring ICCA at a specified frequency and voltage for each circuit component of interest. Measurements have been made over a range of frequencies at a fixed value of VCC. Equivalent capacitance is frequency-independent, so the results can be used over a wide range of operating conditions. Equivalent capacitance values are shown below.

CEQ Values for eX Devices

Combinatorial modules (Ceqcm)	1.70 pF
Sequential modules (Ceqsm)	1.70 pF
Input buffers (Ceqi)	1.30 pF
Output buffers (Ceqo)	7.40 pF
Routed array clocks (Ceqcr)	1.05 pF

The variable and fixed capacitance of other device components must also be taken into account when estimating the dynamic power dissipation.

Table 1-12 shows the capacitance of the clock components of eX devices.

***Table 1-12* • Capacitance of Clock Components of eX Devices**

	eX64	eX128	eX256
Dedicated array clock – variable (Ceqhv)	0.85 pF	0.85 pF	0.85 pF
Dedicated array clock – fixed (Ceqhf)	18.00 pF	20.00 pF	25.00 pF
Routed array clock A (r1)	23.00 pF	28.00 pF	35.00 pF
Routed array clock B (r2)	23.00 pF	28.00 pF	35.00 pF

eX Family Timing Characteristics

***Table 1-17* • eX Family Timing Characteristics**
(Worst-Case Commercial Conditions, VCCA = 2.3 V, T_J = 70°C)

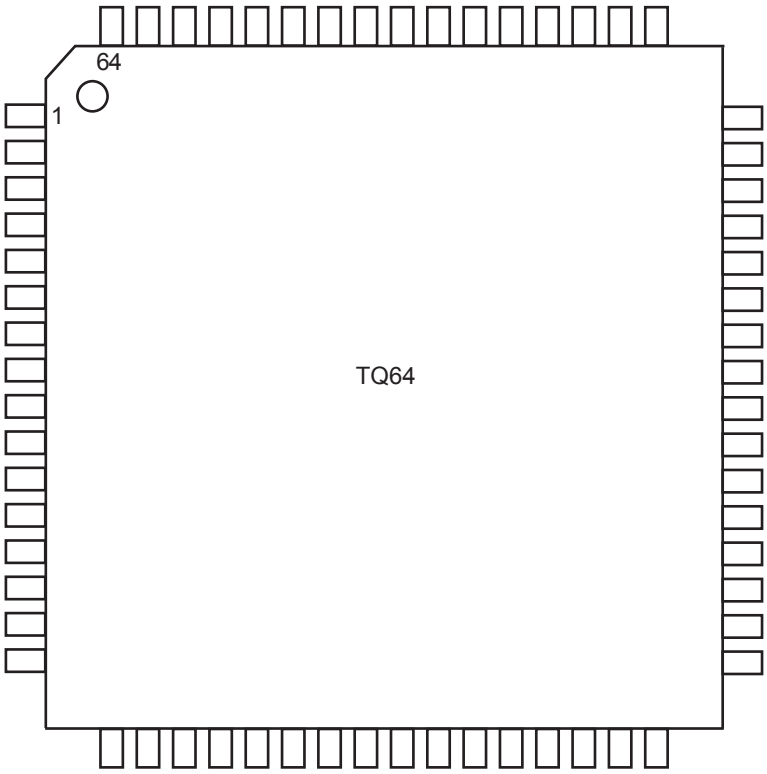
		–P Speed		Std Speed		–F Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
C-Cell Propagation Delays[1]								
t_{PD}	Internal Array Module		0.7		1.0		1.4	ns
Predicted Routing Delays[2]								
t_{DC}	FO=1 Routing Delay, DirectConnect		0.1		0.1		0.2	ns
t_{FC}	FO=1 Routing Delay, FastConnect		0.3		0.5		0.7	ns
t_{RD1}	FO=1 Routing Delay		0.3		0.5		0.7	ns
t_{RD2}	FO=2 Routing Delay		0.4		0.6		0.8	ns
t_{RD3}	FO=3 Routing Delay		0.5		0.8		1.1	ns
t_{RD4}	FO=4 Routing Delay		0.7		1.0		1.3	ns
t_{RD8}	FO=8 Routing Delay		1.2		1.7		2.4	ns
t_{RD12}	FO=12 Routing Delay		1.7		2.5		3.5	ns
R-Cell Timing								
t_{RCO}	Sequential Clock-to-Q		0.6		0.9		1.3	ns
t_{CLR}	Asynchronous Clear-to-Q		0.6		0.8		1.2	ns
t_{PRESET}	Asynchronous Preset-to-Q		0.7		0.9		1.3	ns
t_{SUD}	Flip-Flop Data Input Set-Up	0.5		0.7		1.0		ns
t_{HD}	Flip-Flop Data Input Hold	0.0		0.0		0.0		ns
t_{WASYN}	Asynchronous Pulse Width	1.3		1.9		2.6		ns
$t_{RECASYN}$	Asynchronous Recovery Time	0.3		0.5		0.7		ns
t_{HASYN}	Asynchronous Hold Time	0.3		0.5		0.7		ns
2.5 V Input Module Propagation Delays								
t_{INYH}	Input Data Pad-to-Y HIGH		0.6		0.9		1.3	ns
t_{INYL}	Input Data Pad-to-Y LOW		0.8		1.1		1.5	ns
3.3 V Input Module Propagation Delays								
t_{INYH}	Input Data Pad-to-Y HIGH		0.7		1.0		1.4	ns
t_{INYL}	Input Data Pad-to-Y LOW		0.9		1.3		1.8	ns
5.0 V Input Module Propagation Delays								
t_{INYH}	Input Data Pad-to-Y HIGH		0.7		1.0		1.4	ns
t_{INYL}	Input Data Pad-to-Y LOW		0.9		1.3		1.8	ns
Input Module Predicted Routing Delays[2]								
t_{IRD1}	FO=1 Routing Delay		0.3		0.4		0.5	ns
t_{IRD2}	FO=2 Routing Delay		0.4		0.6		0.8	ns
t_{IRD3}	FO=3 Routing Delay		0.5		0.8		1.1	ns
t_{IRD4}	FO=4 Routing Delay		0.7		1.0		1.3	ns
t_{IRD8}	FO=8 Routing Delay		1.2		1.7		2.4	ns
t_{IRD12}	FO=12 Routing Delay		1.7		2.5		3.5	ns

Notes:

1. *For dual-module macros, use t_{PD} + t_{RD1} + t_{PDn}, t_{RCO} + t_{RD1} + t_{PDn} or t_{PD1} + t_{RD1} + t_{SUD}, whichever is appropriate.*
2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance.*

2 – Package Pin Assignments

TQ64



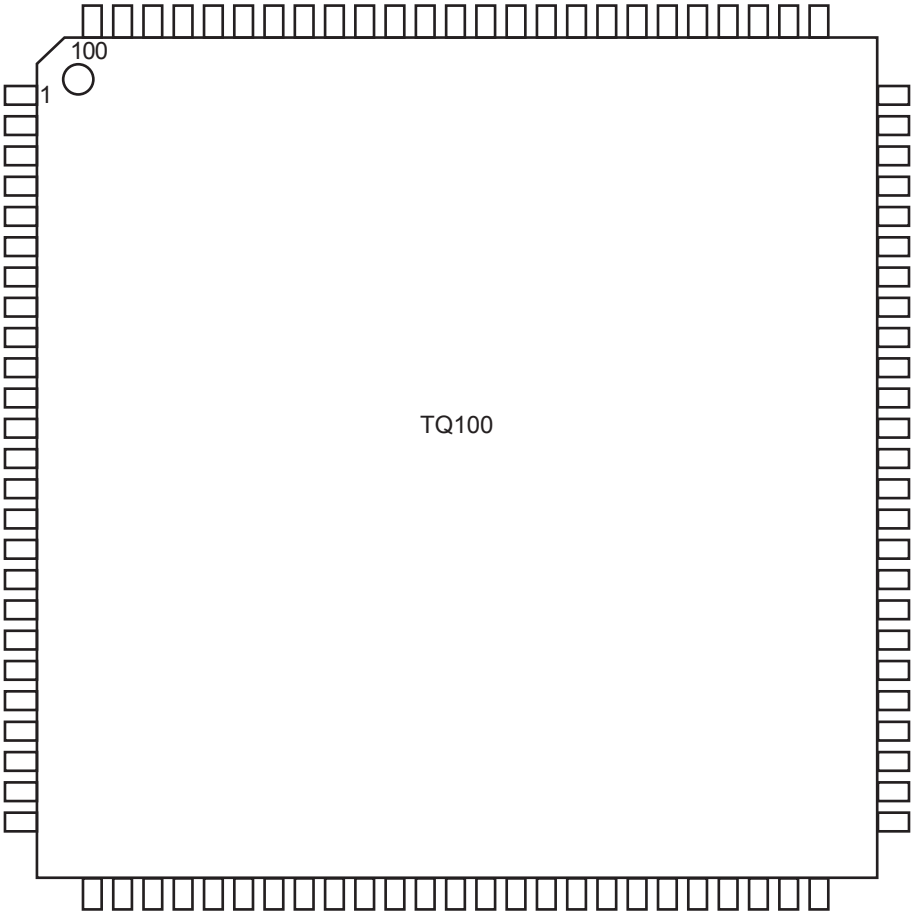
Note: For Package Manufacturing and Environmental information, visit Resource center at www.microsemi.com/soc/products/rescenter/package/index.html.

TQ64		
Pin Number	eX64 Function	eX128 Function
1	GND	GND
2	TDI, I/O	TDI, I/O
3	I/O	I/O
4	TMS	TMS
5	GND	GND
6	VCCI	VCCI
7	I/O	I/O
8	I/O	I/O
9	NC	I/O
10	NC	I/O
11	TRST, I/O	TRST, I/O
12	I/O	I/O
13	NC	I/O
14	GND	GND
15	I/O	I/O
16	I/O	I/O
17	I/O	I/O
18	I/O	I/O
19	VCCI	VCCI
20	I/O	I/O
21	PRB, I/O	PRB, I/O
22	VCCA	VCCA
23	GND	GND
24	I/O	I/O
25	HCLK	HCLK
26	I/O	I/O
27	I/O	I/O
28	I/O	I/O
29	I/O	I/O
30	I/O	I/O
31	I/O	I/O
32	TDO, I/O	TDO, I/O

TQ64		
Pin Number	eX64 Function	eX128 Function
33	GND	GND
34	I/O	I/O
35	I/O	I/O
36	VCCA	VCCA
37	VCCI	VCCI
38	I/O	I/O
39	I/O	I/O
40	NC	I/O
41	NC	I/O
42	I/O	I/O
43	I/O	I/O
44	VCCA	VCCA
45*	GND/LP	GND/ LP
46	GND	GND
47	I/O	I/O
48	I/O	I/O
49	I/O	I/O
50	I/O	I/O
51	I/O	I/O
52	VCCI	VCCI
53	I/O	I/O
54	I/O	I/O
55	CLKA	CLKA
56	CLKB	CLKB
57	VCCA	VCCA
58	GND	GND
59	PRA, I/O	PRA, I/O
60	I/O	I/O
61	VCCI	VCCI
62	I/O	I/O
63	I/O	I/O
64	TCK, I/O	TCK, I/O

*Note: *Please read the LP pin descriptions for restrictions on their use.*

TQ100



Note: For Package Manufacturing and Environmental information, visit Resource center at www.microsemi.com/soc/products/rescenter/package/index.html.

TQ100			
Pin Number	**eX64 Function**	**eX128 Function**	**eX256 Function**
71	I/O	I/O	I/O
72	NC	I/O	I/O
73	NC	NC	I/O
74	NC	NC	I/O
75	NC	NC	I/O
76	NC	I/O	I/O
77	I/O	I/O	I/O
78	I/O	I/O	I/O
79	I/O	I/O	I/O
80	I/O	I/O	I/O
81	I/O	I/O	I/O
82	VCCI	VCCI	VCCI
83	I/O	I/O	I/O
84	I/O	I/O	I/O
85	I/O	I/O	I/O
86	I/O	I/O	I/O
87	CLKA	CLKA	CLKA
88	CLKB	CLKB	CLKB
89	NC	NC	NC
90	VCCA	VCCA	VCCA
91	GND	GND	GND
92	PRA, I/O	PRA, I/O	PRA, I/O
93	I/O	I/O	I/O
94	I/O	I/O	I/O
95	I/O	I/O	I/O
96	I/O	I/O	I/O
97	I/O	I/O	I/O
98	I/O	I/O	I/O
99	I/O	I/O	I/O
100	TCK, I/O	TCK, I/O	TCK, I/O

*Note: *Please read the LP pin descriptions for restrictions on their use.*

3 – Datasheet Information

List of Changes

The following table lists critical changes that were made in the current version of the document.

Revision	Changes	Page
Revision 10 (October 2012)	The "User Security" section was revised to clarify that although no existing security measures can give an absolute guarantee, Microsemi FPGAs implement industry standard security (SAR 34677).	1-5
	Package names used in the "Product Profile" section and "Package Pin Assignments" section were revised to match standards given in *Package Mechanical Drawings* (SAR 34779).	I 2-1
Revision 9 (June 2011)	The versioning system for datasheets has been changed. Datasheets are assigned a revision number that increments each time the datasheet is revised. The "eX Device Status" table indicates the status for each device in the device family.	II
	The Chip Scale packages (CS49, CS128, CS181) are no longer offered for eX devices. They have been removed from the product family information. Pin tables for CSP packages have been removed from the datasheet (SAR 32002).	N/A
Revision 8 (v4.3, June 2006)	The "Ordering Information" was updated with RoHS information. The TQFP measurement was also updated.	II
	The "Dedicated Test Mode" was updated.	1-10
	Note 5 was added to the "3.3 V LVTTL Electrical Specifications" and "5.0 V TTL Electrical Specifications" tables	1-18
	The "LP Low Power Pin" description was updated.	1-31
Revision 7 (v4.2, June 2004)	The "eX Timing Model" was updated.	1-22
v4.1	The "Development Tool Support" section was updated.	1-13
	The "Package Thermal Characteristics" section was updated.	1-21
v4.0	The "Product Profile" section was updated.	1-I
	The "Ordering Information" section was updated.	1-II
	The "Temperature Grade Offerings" section is new.	1-III
	The "Speed Grade and Temperature Grade Matrix" section is new.	1-III
	The "eX FPGA Architecture and Characteristics" section was updated.	1-1
	The "Clock Resources" section was updated.	1-3
	Table 1-1 •Connections of Routed Clock Networks, CLKA and CLKB is new.	1-4
	The "User Security" section was updated.	1-5
	The "I/O Modules" section was updated.	1-5
	The "Hot-Swapping" section was updated.	1-6
	The "Power Requirements" section was updated.	1-6
	The "Low Power Mode" section was updated.	1-6
	The "Boundary Scan Testing (BST)" section was updated.	1-10
	The "Dedicated Test Mode" section was updated.	1-10

Revision	Changes	Page
v4.0 (continued)	The "Flexible Mode" section was updated.	1-10
	Table 1-5 •Boundary-Scan Pin Configurations and Functions is new.	1-11
	The "TRST Pin" section was updated.	1-11
	The "Probing Capabilities" section is new.	1-12
	The "Programming" section was updated.	1-12
	The "Probing Capabilities" section was updated.	1-12
	The "Silicon Explorer II Probe" section was updated.	1-12
	The "Design Considerations" section was updated.	1-13
	The "Development Tool Support" section was updated.	1-13
	The "Absolute Maximum Ratings*" section was updated.	1-16
	The "Temperature and Voltage Derating Factors" section was updated.	1-26
	The "TDI, I/O Test Data Input" section was updated.	1-31
	The "TDO, I/O Test Data Output" section was updated.	1-31
	The "TMS Test Mode Select" section was updated.	1-32
	The "TRST, I/O Boundary Scan Reset Pin" section was updated.	1-32
	All VSV pins were changed to VCCA. The change affected the following pins: 64-Pin TQFP – Pin 36 100-Pin TQFP – Pin 57 49-Pin CSP – Pin D5 128-Pin CSP– Pin H11 and Pin J1 for eX256 180-Pin CSP – Pins J12 and K2	
v3.0	The "Recommended Operating Conditions" section has been changed.	1-16
	The "3.3 V LVTTL Electrical Specifications" section has been updated.	1-18
	The "5.0 V TTL Electrical Specifications" section has been updated.	1-18
	The "Total Dynamic Power (mW)" section is new.	1-9
	The "System Power at 5%, 10%, and 15% Duty Cycle" section is new.	1-9
	The "eX Timing Model" section has been updated.	1-22
v2.0.1	The I/O Features table, Table 1-2 on page 1-6, was updated.	1-6
	The table, "Standby Power of eX Devices in LP Mode Typical Conditions, VCCA, VCCI = 2.5 V, TJ = 25° C" section, was updated.	1-7
	"Typical eX Standby Current at 25°C" section is a new table.	1-16
	The table in the section, "Package Thermal Characteristics" section has been updated for the 49-Pin CSP.	1-21
	The "eX Timing Model" section has been updated.	1-22
	The timing numbers found in, "eX Family Timing Characteristics" section have been updated.	1-27
	The V_{SV} pin has been added to the "Pin Description" section.	1-31
	Please see the following pin tables for the V_{SV} pin and an important footnote including the pin: "TQ64", "TQ100", "128-Pin CSP", and "180-Pin CSP".	2-1, 2-3, 2-6, 2-11
	The figure, "TQ64" section has been updated.	2-1

Revision	Changes	Page
Advance v0.4	In the Product Profile, the Maximum User I/Os for eX64 was changed to 84.	1-I
	In the Product Profile table, the Maximum User I/Os for eX128 was changed to 100.	1-I
Advance v0.3	The Mechanical Drawings section has been removed from the data sheet. The mechanical drawings are now contained in a separate document, “Package Characteristics and Mechanical Drawings,” available on the Actel web site.	
	A new section describing "Clock Resources"has been added.	1-3
	A new table describing "I/O Features"has been added.	1-6
	The "Pin Description"section has been updated and clarified.	1-31
	The original Electrical Specifications table was separated into two tables (2.5V and 3.3/5.0V). In both tables, several different currents are specified for V_{OH} and V_{OL}.	Page 8 and 9
	A new table listing 2.5V low power specifications and associated power graphs were added.	page 9
	Pin functions for eX256 TQ100 have been added to the "TQ100"table.	2-3
	A CS49 pin drawing and pin assignment table including eX64 and eX128 pin functions have been added.	page 26
	A CS128 pin drawing and pin assignment table including eX64, eX128, and eX256 pin functions have been added.	pages 26-27
	A CS180 pin drawing and pin assignment table for eX256 pin functions have been added.	pages 27, 31
Advance v0.2	The following table note was added to the eX Timing Characteristics table for clarification: Clock skew improves as the clock network becomes more heavily loaded.	pages 14-15