



Welcome to [E-XFL.COM](https://www.e-xfl.com)

Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	512
Total RAM Bits	-
Number of I/O	81
Number of Gates	12000
Voltage - Supply	2.3V ~ 2.7V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 125°C (TA)
Package / Case	100-LQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/ex256-tq100a

Temperature Grade Offerings

Device\ Package	TQ64	TQ100
eX64	C, I, A	C, I, A
eX128	C, I, A	C, I, A
eX256	C, I, A	C, I, A

Note: C = Commercial

I = Industrial

A = Automotive

Speed Grade and Temperature Grade Matrix

	–F	Std	–P
C	✓	✓	✓
I		✓	✓
A		✓	

Note: P = Approximately 30% faster than Standard

–F = Approximately 40% slower than Standard

Refer to the [eX Automotive Family FPGAs](#) datasheet for details on automotive temperature offerings.

Contact your local Microsemi representative for device availability.

1 – eX FPGA Architecture and Characteristics

General Description

The eX family of FPGAs is a low-cost solution for low-power, high-performance designs. The inherent low power attributes of the antifuse technology, coupled with an additional low static power mode, make these devices ideal for power-sensitive applications. Fabricated with an advanced 0.22 μm CMOS antifuse technology, these devices achieve high performance with no power penalty.

eX Family Architecture

Microsemi eX family is implemented on a high-voltage twin-well CMOS process using 0.22 μm design rules. The eX family architecture uses a “sea-of-modules” structure where the entire floor of the device is covered with a grid of logic modules with virtually no chip area lost to interconnect elements or routing. Interconnection among these logic modules is achieved using Microsemi patented metal-to-metal programmable antifuse interconnect elements. The antifuse interconnect is made up of a combination of amorphous silicon and dielectric material with barrier metals and has an “on” state resistance of 25Ω with a capacitance of 1.0fF for low-signal impedance. The antifuses are normally open circuit and, when programmed, form a permanent low-impedance connection. The eX family provides two types of logic modules, the register cell (R-cell) and the combinatorial cell (C-cell).

The R-cell contains a flip-flop featuring asynchronous clear, asynchronous preset, and clock enable (using the S0 and S1 lines) control signals ([Figure 1-1](#)). The R-cell registers feature programmable clock polarity selectable on a register-by-register basis. This provides additional flexibility while allowing mapping of synthesized functions into the eX FPGA. The clock source for the R-cell can be chosen from either the hard-wired clock or the routed clock.

The C-cell implements a range of combinatorial functions up to five inputs ([Figure 1-2 on page 1-2](#)). Inclusion of the DB input and its associated inverter function enables the implementation of more than 4,000 combinatorial functions in the eX architecture in a single module.

Two C-cells can be combined together to create a flip-flop to imitate an R-cell via the use of the CC macro. This is particularly useful when implementing non-timing-critical paths and when the design engineer is running out of R-cells. More information about the CC macro can be found in the [Maximizing Logic Utilization in eX, SX and SX-A FPGA Devices Using CC Macros](#) application note.

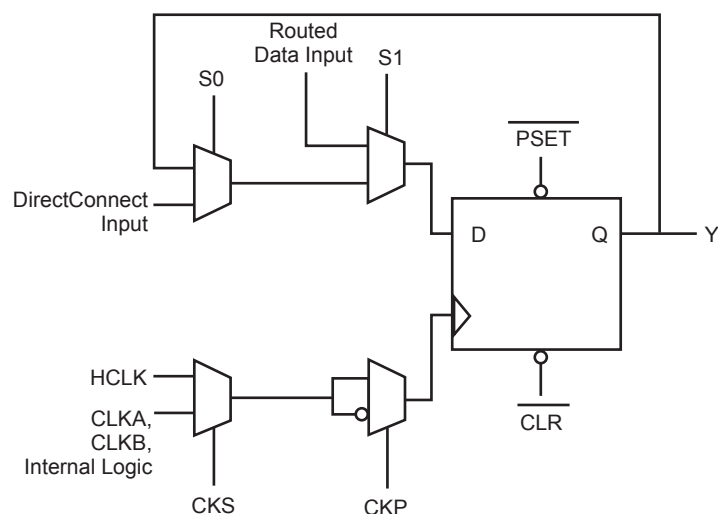


Figure 1-1 • R-Cell

Module Organization

C-cell and R-cell logic modules are arranged into horizontal banks called Clusters, each of which contains two C-cells and one R-cell in a C-R-C configuration.

Clusters are further organized into modules called SuperClusters for improved design efficiency and device performance, as shown in Figure 1-3. Each SuperCluster is a two-wide grouping of Clusters.

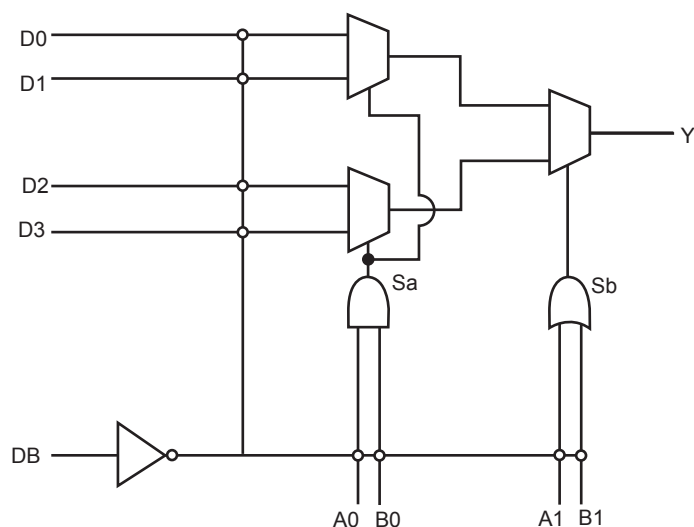


Figure 1-2 • C-Cell

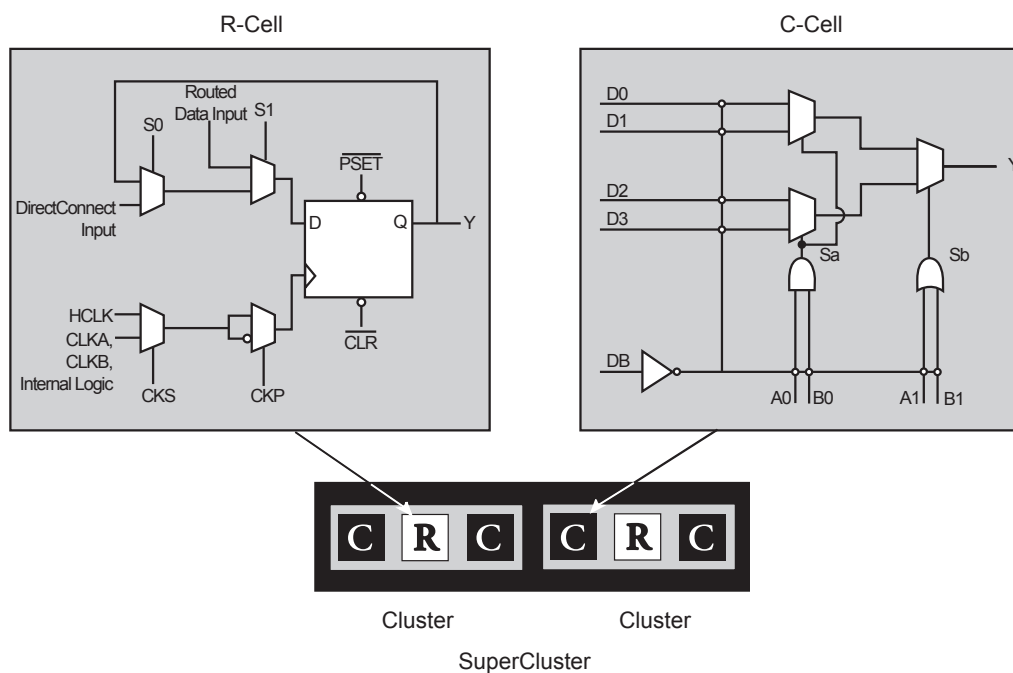


Figure 1-3 • Cluster Organization

Routing Resources

Clusters and SuperClusters can be connected through the use of two innovative local routing resources called FastConnect and DirectConnect, which enable extremely fast and predictable interconnection of modules within Clusters and SuperClusters (Figure 1-4). This routing architecture also dramatically reduces the number of antifuses required to complete a circuit, ensuring the highest possible performance.

DirectConnect is a horizontal routing resource that provides connections from a C-cell to its neighboring R-cell in a given SuperCluster. DirectConnect uses a hard-wired signal path requiring no programmable interconnection to achieve its fast signal propagation time of less than 0.1 ns (–P speed grade).

FastConnect enables horizontal routing between any two logic modules within a given SuperCluster and vertical routing with the SuperCluster immediately below it. Only one programmable connection is used in a FastConnect path, delivering maximum pin-to-pin propagation of 0.3 ns (–P speed grade).

In addition to DirectConnect and FastConnect, the architecture makes use of two globally oriented routing resources known as segmented routing and high-drive routing. The segmented routing structure of Microsemi provides a variety of track lengths for extremely fast routing between SuperClusters. The exact combination of track lengths and antifuses within each path is chosen by the fully automatic place-and-route software to minimize signal propagation delays.

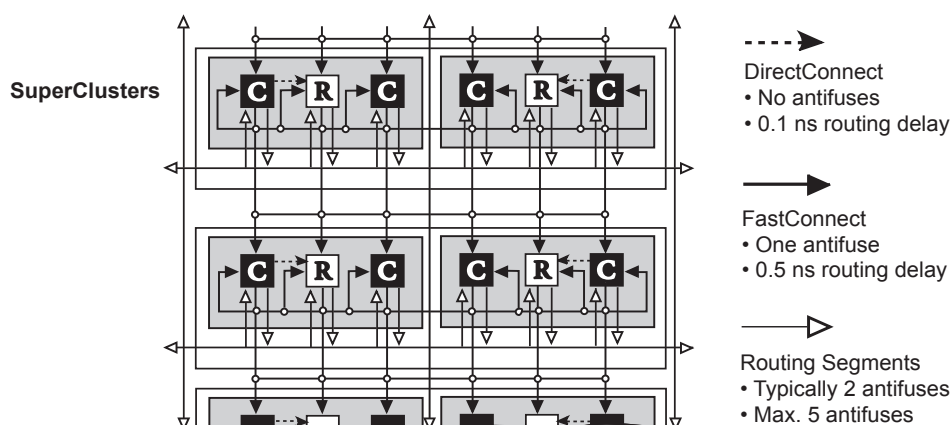


Figure 1-4 • DirectConnect and FastConnect for SuperClusters

Clock Resources

eX's high-drive routing structure provides three clock networks. The first clock, called HCLK, is hardwired from the HCLK buffer to the clock select MUX in each R-Cell. HCLK cannot be connected to combinational logic. This provides a fast propagation path for the clock signal, enabling the 3.9 ns clock-to-out (pad-to-pad) performance of the eX devices. The hard-wired clock is tuned to provide a clock skew of less than 0.1 ns worst case. If not used, the HCLK pin must be tied LOW or HIGH and must not be left floating. Figure 1-5 describes the clock circuit used for the constant load HCLK.

HCLK does not function until the fourth clock cycle each time the device is powered up to prevent false output levels due to any possible slow power-on-reset signal and fast start-up clock circuit. To activate HCLK from the first cycle, the TRST pin must be reserved in the Design software and the pin must be tied to GND on the board. (See the "TRST, I/O Boundary Scan Reset Pin" on page 1-32).

The remaining two clocks (CLKA, CLKB) are global routed clock networks that can be sourced from external pins or from internal logic signals (via the CLKINT routed clock buffer) within the eX device. CLKA and CLKB may be connected to sequential cells or to combinational logic. If CLKA or CLKB is sourced from internal logic signals, the external clock pin cannot be used for any other input and must be tied LOW or HIGH and must not float. Figure 1-6 describes the CLKA and CLKB circuit used in eX devices.

Other Architectural Features

Performance

The combination of architectural features described above enables eX devices to operate with internal clock frequencies exceeding 350 MHz for very fast execution of complex logic functions. The eX family is an optimal platform upon which the functionality previously contained in CPLDs can be integrated. eX devices meet the performance goals of gate arrays, and at the same time, present significant improvements in cost and time to market. Using timing-driven place-and-route tools, designers can achieve highly deterministic device performance.

User Security

Microsemi FuseLock advantage provides the highest level of protection in the FPGA industry against unauthorized modifications. In addition to the inherent strengths of the architecture, special security fuses that are intended to prevent internal probing and overwriting are hidden throughout the fabric of the device. They are located such that they cannot be accessed or bypassed without destroying the rest of the device, making Microsemi antifuse FPGAs highly resistant to both invasive and more subtle noninvasive attacks.

Look for this symbol to ensure your valuable IP is secure. The FuseLock Symbol on the FPGA ensures that the device is safeguarded to cryptographic attacks.



Figure 1-7 • FuseLock

For more information, refer to [Implementation of Security in Microsemi Antifuse FPGAs](#) application note.

I/O Modules

Each I/O on an eX device can be configured as an input, an output, a tristate output, or a bidirectional pin. Even without the inclusion of dedicated I/O registers, these I/Os, in combination with array registers, can achieve clock-to-out (pad-to-pad) timing as fast as 3.9 ns. I/O cells in eX devices do not contain embedded latches or flip-flops and can be inferred directly from HDL code. The device can easily interface with any other device in the system, which in turn enables parallel design of system components and reduces overall design time.

All unused I/Os are configured as tristate outputs by Microsemi's Designer software, for maximum flexibility when designing new boards or migrating existing designs. Each I/O module has an available pull-up or pull-down resistor of approximately 50 k Ω that can configure the I/O in a known state during power-up. Just shortly before V_{CCA} reaches 2.5 V, the resistors are disabled and the I/Os will be controlled by user logic.

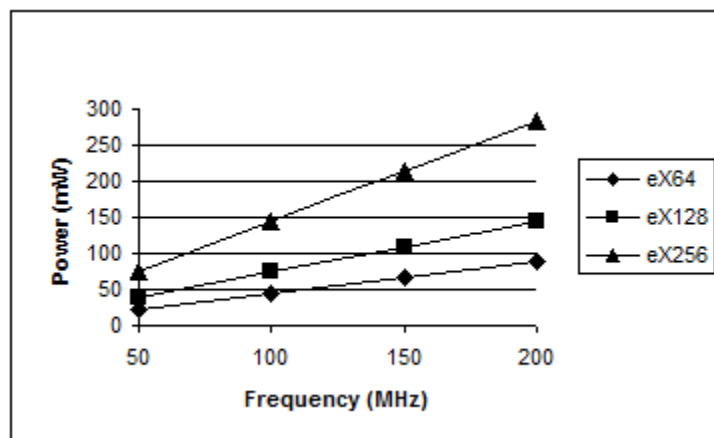
To exit the LP mode, the LP pin must be driven LOW for over 200 μ s to allow for the charge pumps to power-up and device initialization can begin.

Table 1-3 illustrates the standby current of eX devices in LP mode.

Table 1-3 • Standby Power of eX Devices in LP Mode Typical Conditions, V_{CCA} , V_{CCI} = 2.5 V, T_J = 25° C

Product	Low Power Standby Current	Units
eX64	100	μ A
eX128	111	μ A
eX256	134	μ A

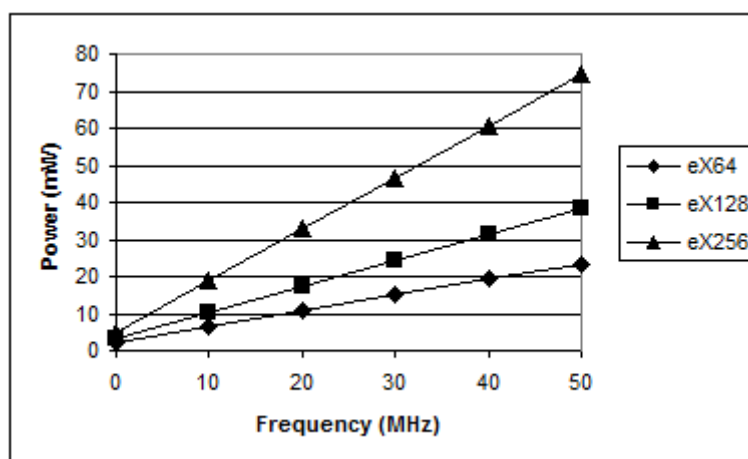
Figure 1-8 to Figure 1-11 on page 1-9 show some sample power characteristics of eX devices.



Notes:

1. Device filled with 16-bit counters.
2. VCCA, VCCI = 2.7 V, device tested at room temperature.

Figure 1-8 • eX Dynamic Power Consumption – High Frequency



Notes:

1. Device filled with 16-bit counters.
2. VCCA, VCCI = 2.7 V, device tested at room temperature.

Figure 1-9 • eX Dynamic Power Consumption – Low Frequency

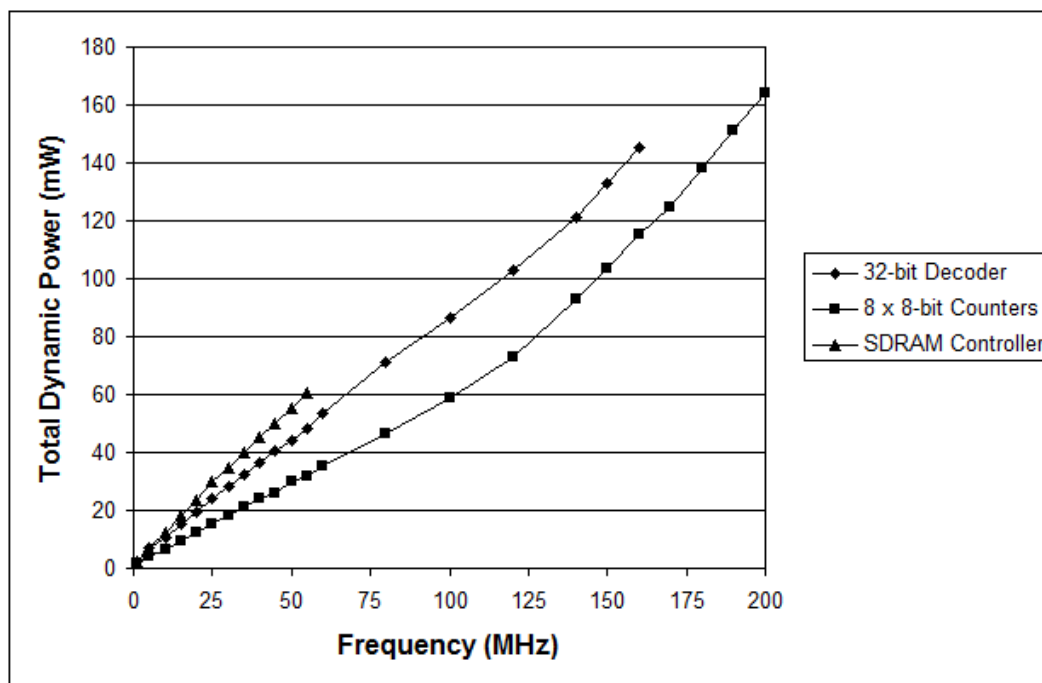


Figure 1-10 • Total Dynamic Power (mW)

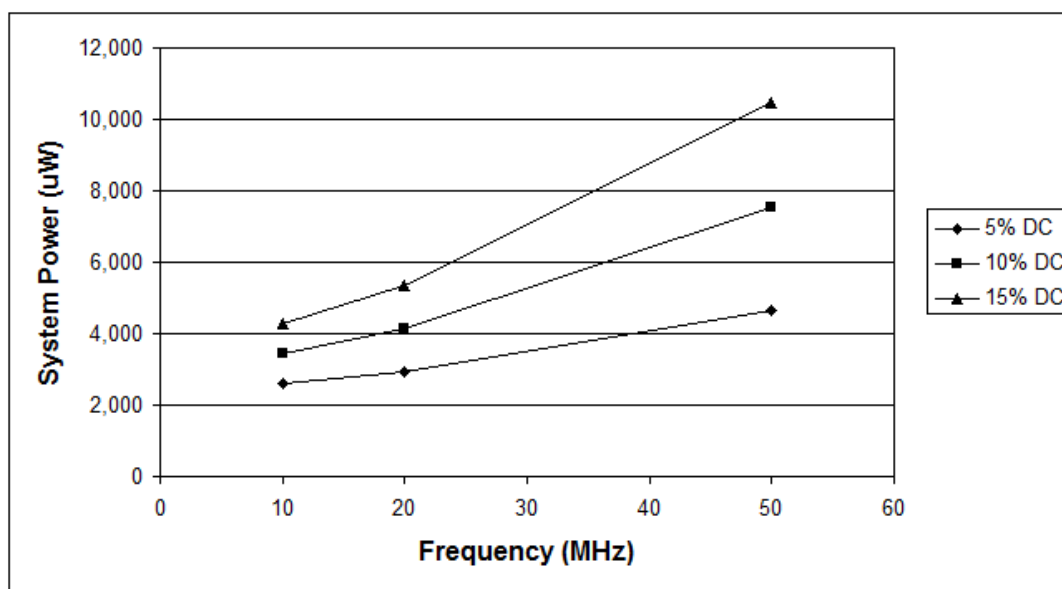


Figure 1-11 • System Power at 5%, 10%, and 15% Duty Cycle

Table 1-5 describes the different configuration requirements of BST pins and their functionality in different modes.

Table 1-5 • Boundary-Scan Pin Configurations and Functions

Mode	Designer "Reserve JTAG" Selection	TAP Controller State
Dedicated (JTAG)	Checked	Any
Flexible (User I/O)	Unchecked	Test-Logic-Reset
Flexible (JTAG)	Unchecked	Any EXCEPT Test-Logic-Reset

TRST Pin

The TRST pin functions as a dedicated Boundary-Scan Reset pin when the **Reserve JTAG Test Reset** option is selected, as shown in Figure 1-12. An internal pull-up resistor is permanently enabled on the TRST pin in this mode. It is recommended to connect this pin to GND in normal operation to keep the JTAG state controller in the Test-Logic-Reset state. When JTAG is being used, it can be left floating or be driven HIGH.

When the **Reserve JTAG Test Reset** option is not selected, this pin will function as a regular I/O. If unused as an I/O in the design, it will be configured as a tristated output.

JTAG Instructions

Table 1-6 lists the supported instructions with the corresponding IR codes for eX devices.

Table 1-6 • JTAG Instruction Code

Instructions (IR4: IR0)	Binary Code
EXTEST	00000
SAMPLE / PRELOAD	00001
INTTEST	00010
USERCODE	00011
IDCODE	00100
HIGHZ	01110
CLAMP	01111
Diagnostic	10000
BYPASS	11111
Reserved	All others

Table 1-7 lists the codes returned after executing the IDCODE instruction for eX devices. Note that bit 0 is always "1." Bits 11-1 are always "02F", which is Microsemi SoC Products Group's manufacturer code.

Table 1-7 • IDCODE for eX Devices

Device	Revision	Bits 31-28	Bits 27-12
eX64	0	8	40B2, 42B2
eX128	0	9	40B0, 42B0
eX256	0	9	40B5, 42B5
eX64	1	A	40B2, 42B2
eX128	1	B	40B0, 42B0
eX256	1	B	40B5, 42B5

Related Documents

Datasheet

eX Automotive Family FPGAs

www.microsemi.com/soc/documents/eX_Auto_DS.pdf

Application Notes

Maximizing Logic Utilization in eX, SX and SX-A FPGA Devices Using CC Macros

www.microsemi.com/soc/documents/CC_Macro_AN.pdf

Implementation of Security in Microsemi Antifuse FPGAs

www.microsemi.com/soc/documents/Antifuse_Security_AN.pdf

Microsemi eX, SX-A, and RT54SX-S I/Os

www.microsemi.com/soc/documents/antifuseIO_AN.pdf

Microsemi SX-A and RT54SX-S Devices in Hot-Swap and Cold-Sparing Applications

www.microsemi.com/soc/documents/HotSwapColdSparing_AN.pdf

Design For Low Power in Microsemi Antifuse FPGAs

www.microsemi.com/soc/documents/Low_Power_AN.pdf

Programming Antifuse Devices

www.microsemi.com/soc/documents/AntifuseProgram_AN.pdf

User Guides

Silicon Sculptor II User's Guide

www.microsemi.com/soc/documents/SiliSculptII_Sculpt3_ug.pdf

Miscellaneous

Libero IDE flow

www.microsemi.com/soc/products/tools/libero/flow.html

2.5 V LVCMOS2 Electrical Specifications

Symbol	Parameter		Commercial		Industrial		Units
			Min.	Max.	Min.	Max.	
VOH	VCCI = MIN, VI = VIH or VIL	(IOH = -100 mA)	2.1		2.1		V
	VCCI = MIN, VI = VIH or VIL	(IOH = -1 mA)	2.0		2.0		V
	VCCI = MIN, VI = VIH or VIL	(IOH = -2 mA)	1.7		1.7		V
VOL	VCCI = MIN, VI = VIH or VIL	(IOL = 100 mA)		0.2		0.2	V
	VCCI = MIN, VI = VIH or VIL	(IOL = 1mA)		0.4		0.4	V
	VCCI = MIN, VI = VIH or VIL	(IOL = 2 mA)		0.7		0.7	V
VIL	Input Low Voltage, VOUT ≤ VOL (max.)		-0.3	0.7	-0.3	0.7	V
VIH	Input High Voltage, VOUT ≥ VOH (min.)		1.7	VCCI + 0.3	1.7	VCCI + 0.3	V
IIL/ IIH	Input Leakage Current, VIN = VCCI or GND		-10	10	-10	10	μA
IOZ	3-State Output Leakage Current, VOUT = VCCI or GND		-10	10	-10	10	μA
t _R , t _{F1,2}	Input Transition Time			10		10	ns
C _{IO}	I/O Capacitance			10		10	pF
ICC ^{3,4}	Standby Current			1.0		3.0	mA
IV Curve	Can be derived from the IBIS model at www.microsemi.com/soc/custsup/models/ibis.html .						

Notes:

1. t_R is the transition time from 0.7 V to 1.7 V.
2. t_F is the transition time from 1.7 V to 0.7 V.
3. I_{CC} max Commercial -F = 5.0 mA
4. $I_{CC} = I_{CCI} + I_{CCA}$

3.3 V LVTTTL Electrical Specifications

Symbol	Parameter		Commercial		Industrial		Units
			Min.	Max.	Min.	Max.	
VOH	VCCI = MIN, VI = VIH or VIL	(IOH = -8 mA)	2.4		2.4		V
VOL	VCCI = MIN, VI = VIH or VIL	(IOL = 12 mA)		0.4		0.4	V
VIL	Input Low Voltage			0.8		0.8	V
VIH	Input High Voltage		2.0	VCCI +0.5	2.0	VCCI +0.5	V
IIL/ IIH	Input Leakage Current, VIN = VCCI or GND		-10	10	-10	10	μA
IOZ	3-State Output Leakage Current, VOUT = VCCI or GND		-10	10	-10	10	μA
t _R , t _{F1,2}	Input Transition Time			10		10	ns
C _{IO}	I/O Capacitance			10		10	pF
ICC ^{3,4}	Standby Current			1.5		10	mA
IV Curve	Can be derived from the IBIS model at www.microsemi.com/soc/custsup/models/ibis.html .						

Notes:

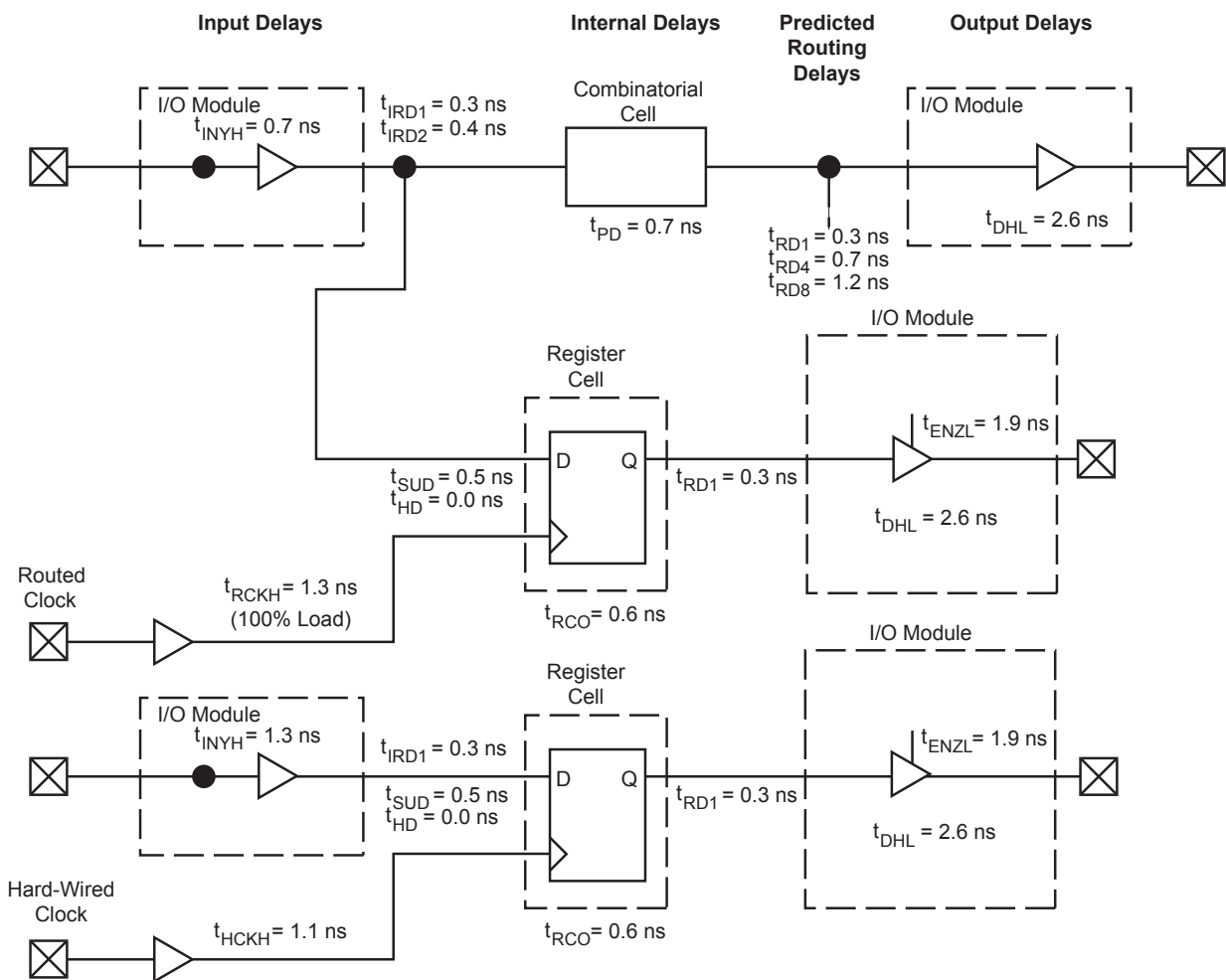
1. t_R is the transition time from 0.8 V to 2.0 V.
2. t_F is the transition time from 2.0 V to 0.8 V.
3. ICC max Commercial -F = 5.0 mA
4. ICC = ICCI + ICCA
5. JTAG pins comply with LVTTTL/TTL I/O specification regardless of whether they are used as a user I/O or a JTAG I/O.

5.0 V TTL Electrical Specifications

Symbol	Parameter		Commercial		Industrial		Units
			Min.	Max.	Min.	Max.	
VOH	VCCI = MIN, VI = VIH or VIL	(IOH = -8 mA)	2.4		2.4		V
VOL	VCCI = MIN, VI = VIH or VIL	(IOL = 12 mA)		0.4		0.4	V
VIL	Input Low Voltage			0.8		0.8	V
VIH	Input High Voltage		2.0	VCCI +0.5	2.0	VCCI +0.5	V
IIL/ IIH	Input Leakage Current, VIN = VCCI or GND		-10	10	-10	10	μA
IOZ	3-State Output Leakage Current, VOUT = VCCI or GND		-10	10	-10	10	μA
t _R , t _{F1,2}	Input Transition Time			10		10	ns
C _{IO}	I/O Capacitance			10		10	pF
ICC ^{3,4}	Standby Current			15		20	mA
IV Curve	Can be derived from the IBIS model at www.microsemi.com/soc/custsup/models/ibis.html .						

Note:

1. t_R is the transition time from 0.8 V to 2.0 V.
2. t_F is the transition time from 2.0 V to 0.8 V.
3. ICC max Commercial -F=20mA
4. ICC = ICCI + ICCA
5. JTAG pins comply with LVTTTL/TTL I/O specification regardless of whether they are used as a user I/O or a JTAG I/O.



Note: Values shown for eX128-P, worst-case commercial conditions (5.0 V, 35 pF Pad Load).

Figure 1-14 • eX Timing Model

Hardwired Clock

$$\text{External Setup} = t_{\text{INYH}} + t_{\text{IRD1}} + t_{\text{SUD}} - t_{\text{HCKH}}$$

$$= 0.7 + 0.3 + 0.5 - 1.1 = 0.4 \text{ ns}$$

Clock-to-Out (Pad-to-Pad), typical

$$= t_{HCKH} + t_{RCO} + t_{RD1} + t_{DHL}$$

$$= 1.1 + 0.6 + 0.3 + 2.6 = 4.6 \text{ ns}$$

Routed Clock

$$\text{External Setup} = t_{\text{INYH}} + t_{\text{IRD2}} + t_{\text{SUD}} - t_{\text{RCKH}}$$

$$= 0.7 + 0.4 + 0.5 - 1.3 = 0.3 \text{ ns}$$

Clock-to-Out (Pad-to-Pad), typical

$$= t_{RCKH} + t_{RCO} + t_{RD1} + t_{DHL}$$

$$= 1.3 + 0.6 + 0.3 + 2.6 = 4.8 \text{ ns}$$

Output Buffer Delays

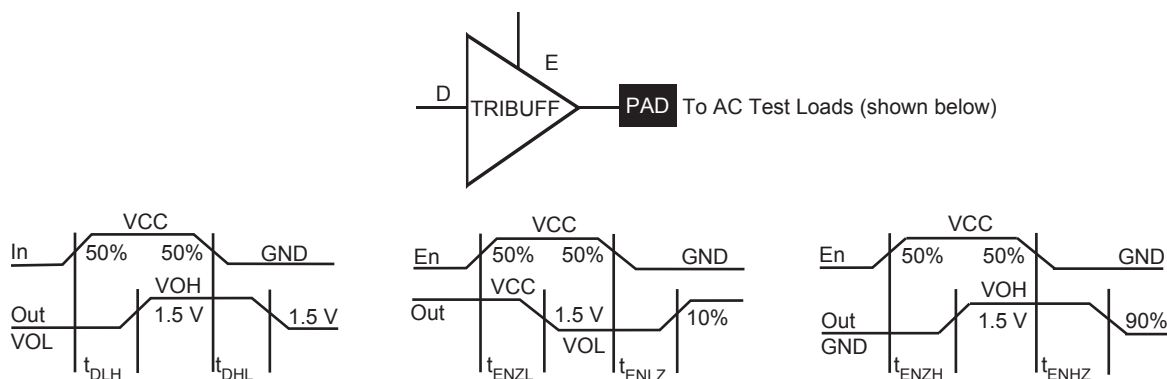


Table 1-13 • Output Buffer Delays

AC Test Loads

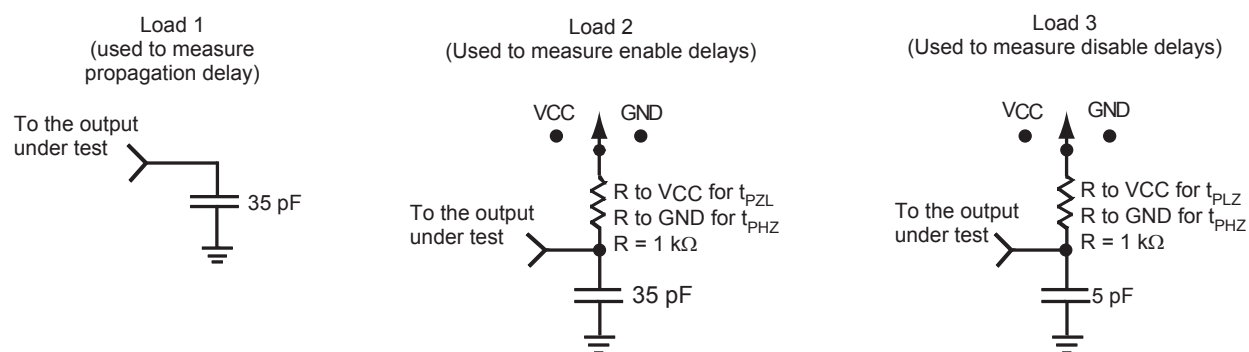


Figure 1-15 • AC Test Loads

Input Buffer Delays

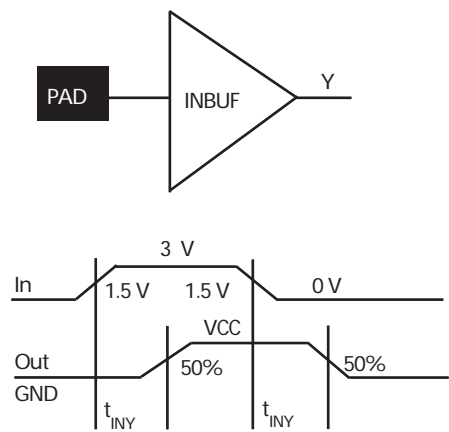


Table 1-14 • Input Buffer Delays

C-Cell Delays

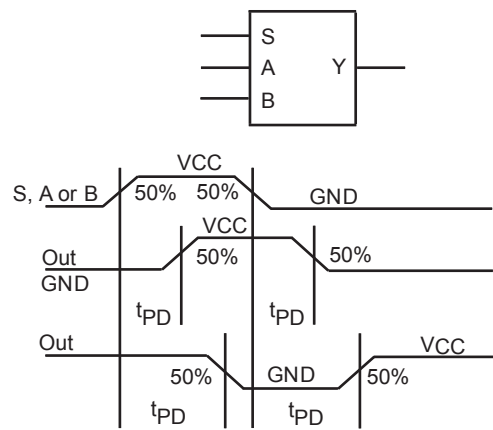


Table 1-15 • C-Cell Delays

Timing Characteristics

Timing characteristics for eX devices fall into three categories: family-dependent, device-dependent, and design-dependent. The input and output buffer characteristics are common to all eX family members. Internal routing delays are device-dependent. Design dependency means actual delays are not determined until after placement and routing of the user's design are complete. Delay values may then be determined by using the Timer utility or performing simulation with post-layout delays.

Critical Nets and Typical Nets

Propagation delays are expressed only for typical nets, which are used for initial design performance evaluation. Critical net delays can then be applied to the most timing critical paths. Critical nets are determined by net property assignment prior to placement and routing. Up to six percent of the nets in a design may be designated as critical.

Long Tracks

Some nets in the design use long tracks. Long tracks are special routing resources that span multiple rows, columns, or modules. Long tracks employ three to five antifuse connections. This increases capacitance and resistance, resulting in longer net delays for macros connected to long tracks. Typically, no more than six percent of nets in a fully utilized device require long tracks. Long tracks contribute approximately 4 ns to 8.4 ns delay. This additional delay is represented statistically in higher fanout routing delays.

Timing Derating

eX devices are manufactured with a CMOS process. Therefore, device performance varies according to temperature, voltage, and process changes. Minimum timing parameters reflect maximum operating voltage, minimum operating temperature, and best-case processing. Maximum timing parameters reflect minimum operating voltage, maximum operating temperature, and worst-case processing.

Temperature and Voltage Derating Factors

Table 1-16 • Temperature and Voltage Derating Factors
(Normalized to Worst-Case Commercial, $T_J = 70^\circ\text{C}$, $V_{CCA} = 2.3\text{V}$)

VCCA	Junction Temperature (T_J)						
	-55	-40	0	25	70	85	125
2.3	0.79	0.80	0.87	0.88	1.00	1.04	1.13
2.5	0.74	0.74	0.81	0.83	0.93	0.97	1.06
2.7	0.69	0.70	0.76	0.78	0.88	0.91	1.00

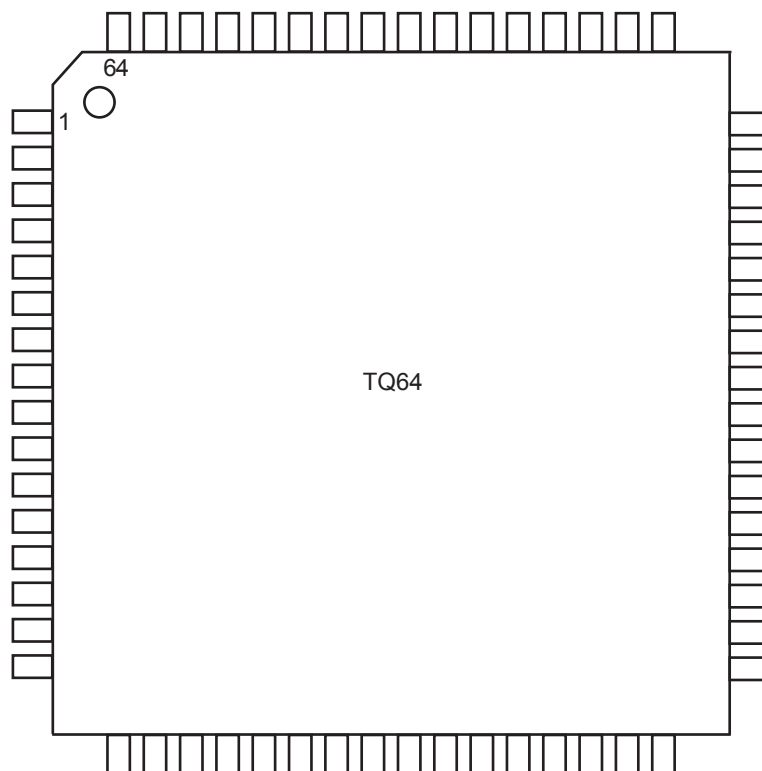
Table 1-19 • eX Family Timing Characteristics
(Worst-Case Commercial Conditions VCCA = 2.3V, VCCI = 2.3 V or 3.0V, T_J = 70°C)

		‘–P’ Speed		‘Std’ Speed		‘–F’ Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Units
Dedicated (Hard-Wired) Array Clock Networks								
t _{HCKH}	Input LOW to HIGH (Pad to R-Cell Input)		1.1		1.6		2.3	ns
t _{HCKL}	Input HIGH to LOW (Pad to R-Cell Input)		1.1		1.6		2.3	ns
t _{HPWH}	Minimum Pulse Width HIGH	1.4		2.0		2.8		ns
t _{HPWL}	Minimum Pulse Width LOW	1.4		2.0		2.8		ns
t _{HCKSW}	Maximum Skew		<0.1		<0.1		<0.1	ns
t _{HP}	Minimum Period	2.8		4.0		5.6		ns
f _{HMAX}	Maximum Frequency		357		250		178	MHz
Routed Array Clock Networks								
t _{RCKH}	Input LOW to HIGH (Light Load) (Pad to R-Cell Input) MAX.		1.0		1.4		2.0	ns
t _{RCKL}	Input HIGH to LOW (Light Load) (Pad to R-Cell Input) MAX.		1.0		1.4		2.0	ns
t _{RCKH}	Input LOW to HIGH (50% Load) (Pad to R-Cell Input) MAX.		1.2		1.7		2.4	ns
t _{RCKL}	Input HIGH to LOW (50% Load) (Pad to R-Cell Input) MAX.		1.2		1.7		2.4	ns
t _{RCKH}	Input LOW to HIGH (100% Load) (Pad to R-Cell Input) MAX.		1.4		2.0		2.8	ns
t _{RCKL}	Input HIGH to LOW (100% Load) (Pad to R-Cell Input) MAX.		1.4		2.0		2.8	ns
t _{RPWH}	Min. Pulse Width HIGH	1.4		2.0		2.8		ns
t _{RPWL}	Min. Pulse Width LOW	1.4		2.0		2.8		ns
t _{RCKSW} *	Maximum Skew (Light Load)		0.2		0.3		0.4	ns
t _{RCKSW} *	Maximum Skew (50% Load)		0.2		0.2		0.3	ns
t _{RCKSW} *	Maximum Skew (100% Load)		0.1		0.1		0.2	ns

Note: *Clock skew improves as the clock network becomes more heavily loaded.

2 – Package Pin Assignments

TQ64



Note: For Package Manufacturing and Environmental information, visit Resource center at www.microsemi.com/soc/products/rescenter/package/index.html.

Revision	Changes	Page
v4.0 (continued)	The "Flexible Mode" section was updated.	1-10
	Table 1-5 •Boundary-Scan Pin Configurations and Functions is new.	1-11
	The "TRST Pin" section was updated.	1-11
	The "Probing Capabilities" section is new.	1-12
	The "Programming" section was updated.	1-12
	The "Probing Capabilities" section was updated.	1-12
	The "Silicon Explorer II Probe" section was updated.	1-12
	The "Design Considerations" section was updated.	1-13
	The "Development Tool Support" section was updated.	1-13
	The "Absolute Maximum Ratings*" section was updated.	1-16
	The "Temperature and Voltage Derating Factors" section was updated.	1-26
	The "TDI, I/O Test Data Input" section was updated.	1-31
	The "TDO, I/O Test Data Output" section was updated.	1-31
	The "TMS Test Mode Select" section was updated.	1-32
	The "TRST, I/O Boundary Scan Reset Pin" section was updated.	1-32
	All VSV pins were changed to VCCA. The change affected the following pins: 64-Pin TQFP – Pin 36 100-Pin TQFP – Pin 57 49-Pin CSP – Pin D5 128-Pin CSP – Pin H11 and Pin J1 for eX256 180-Pin CSP – Pins J12 and K2	
v3.0	The "Recommended Operating Conditions" section has been changed.	1-16
	The "3.3 V LVTTTL Electrical Specifications" section has been updated.	1-18
	The "5.0 V TTL Electrical Specifications" section has been updated.	1-18
	The "Total Dynamic Power (mW)" section is new.	1-9
	The "System Power at 5%, 10%, and 15% Duty Cycle" section is new.	1-9
	The "eX Timing Model" section has been updated.	1-22
v2.0.1	The I/O Features table, Table 1-2 on page 1-6, was updated.	1-6
	The table, "Standby Power of eX Devices in LP Mode Typical Conditions, VCCA, VCCI = 2.5 V, T _J = 25° C" section, was updated.	1-7
	"Typical eX Standby Current at 25°C" section is a new table.	1-16
	The table in the section, "Package Thermal Characteristics" section has been updated for the 49-Pin CSP.	1-21
	The "eX Timing Model" section has been updated.	1-22
	The timing numbers found in, "eX Family Timing Characteristics" section have been updated.	1-27
	The V _{SV} pin has been added to the "Pin Description" section.	1-31
	Please see the following pin tables for the V _{SV} pin and an important footnote including the pin: "TQ64", "TQ100", "128-Pin CSP", and "180-Pin CSP".	2-1, 2-3, 2-6, 2-11
	The figure, "TQ64" section has been updated.	2-1

Revision	Changes	Page
Advance v0.4	In the Product Profile , the Maximum User I/Os for eX64 was changed to 84.	1-I
	In the Product Profile table, the Maximum User I/Os for eX128 was changed to 100.	1-I
Advance v0.3	The Mechanical Drawings section has been removed from the data sheet. The mechanical drawings are now contained in a separate document, "Package Characteristics and Mechanical Drawings," available on the Actel web site.	
	A new section describing " Clock Resources " has been added.	1-3
	A new table describing " I/O Features " has been added.	1-6
	The " Pin Description " section has been updated and clarified.	1-31
	The original Electrical Specifications table was separated into two tables (2.5V and 3.3/5.0V). In both tables, several different currents are specified for V_{OH} and V_{OL} .	Page 8 and 9
	A new table listing 2.5V low power specifications and associated power graphs were added.	page 9
	Pin functions for eX256 TQ100 have been added to the " TQ100 " table.	2-3
	A CS49 pin drawing and pin assignment table including eX64 and eX128 pin functions have been added.	page 26
	A CS128 pin drawing and pin assignment table including eX64, eX128, and eX256 pin functions have been added.	pages 26-27
	A CS180 pin drawing and pin assignment table for eX256 pin functions have been added.	pages 27, 31
Advance v0.2	The following table note was added to the eX Timing Characteristics table for clarification: Clock skew improves as the clock network becomes more heavily loaded.	pages 14-15