Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	512
Total RAM Bits	-
Number of I/O	81
Number of Gates	12000
Voltage - Supply	2.3V ~ 2.7V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 85°C (TA)
Package / Case	100-LQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/ex256-tq100i

Table of Contents

1 – eX FPGA Architecture and Characteristics

General Description

The eX family of FPGAs is a low-cost solution for low-power, high-performance designs. The inherent low power attributes of the antifuse technology, coupled with an additional low static power mode, make these devices ideal for power-sensitive applications. Fabricated with an advanced 0.22 mm CMOS antifuse technology, these devices achieve high performance with no power penalty.

eX Family Architecture

Microsemi eX family is implemented on a high-voltage twin-well CMOS process using 0.22 µm design rules. The eX family architecture uses a “sea-of-modules” structure where the entire floor of the device is covered with a grid of logic modules with virtually no chip area lost to interconnect elements or routing. Interconnection among these logic modules is achieved using Microsemi patented metal-to-metal programmable antifuse interconnect elements. The antifuse interconnect is made up of a combination of amorphous silicon and dielectric material with barrier metals and has an "on" state resistance of 25Ω with a capacitance of 1.0fF for low-signal impedance. The antifuses are normally open circuit and, when programmed, form a permanent low-impedance connection. The eX family provides two types of logic modules, the register cell (R-cell) and the combinatorial cell (C-cell).

The R-cell contains a flip-flop featuring asynchronous clear, asynchronous preset, and clock enable (using the S0 and S1 lines) control signals (Figure 1-1). The R-cell registers feature programmable clock polarity selectable on a register-by-register basis. This provides additional flexibility while allowing mapping of synthesized functions into the eX FPGA. The clock source for the R-cell can be chosen from either the hard-wired clock or the routed clock.

The C-cell implements a range of combinatorial functions up to five inputs (Figure 1-2 on page 1-2). Inclusion of the DB input and its associated inverter function enables the implementation of more than 4,000 combinatorial functions in the eX architecture in a single module.

Two C-cells can be combined together to create a flip-flop to imitate an R-cell via the use of the CC macro. This is particularly useful when implementing non-timing-critical paths and when the design engineer is running out of R-cells. More information about the CC macro can be found in the *Maximizing Logic Utilization in eX, SX and SX-A FPGA Devices Using CC Macros* application note.

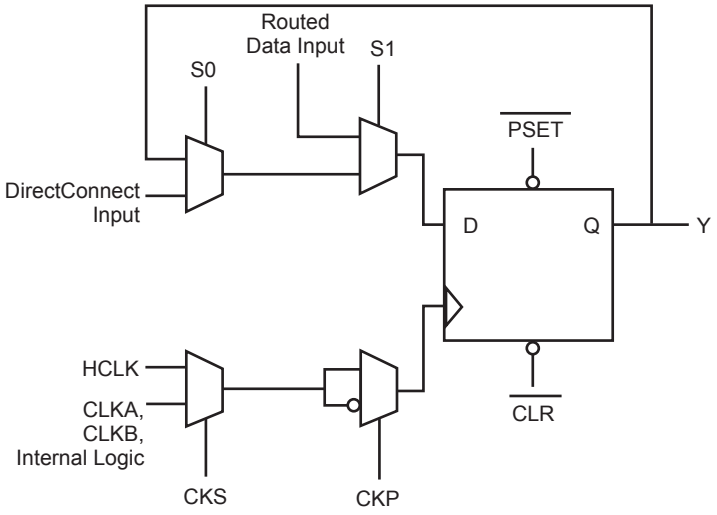


Figure 1-1 • **R-Cell**

Module Organization

C-cell and R-cell logic modules are arranged into horizontal banks called Clusters, each of which contains two C-cells and one R-cell in a C-R-C configuration.

Clusters are further organized into modules called SuperClusters for improved design efficiency and device performance, as shown in Figure 1-3. Each SuperCluster is a two-wide grouping of Clusters.

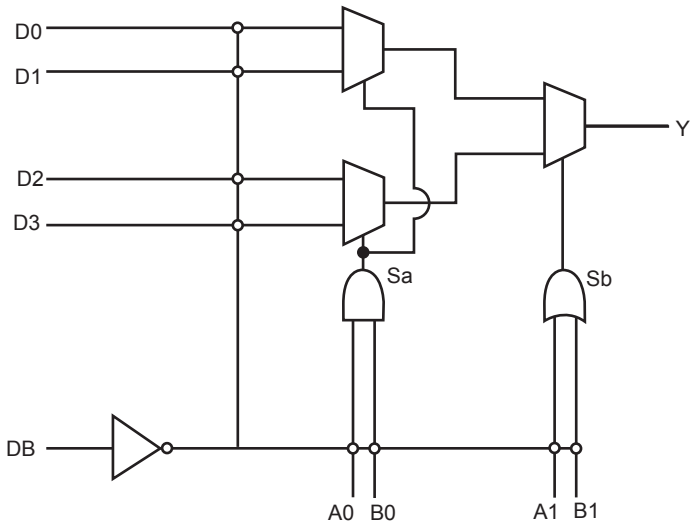


Figure 1-2 • **C-Cell**

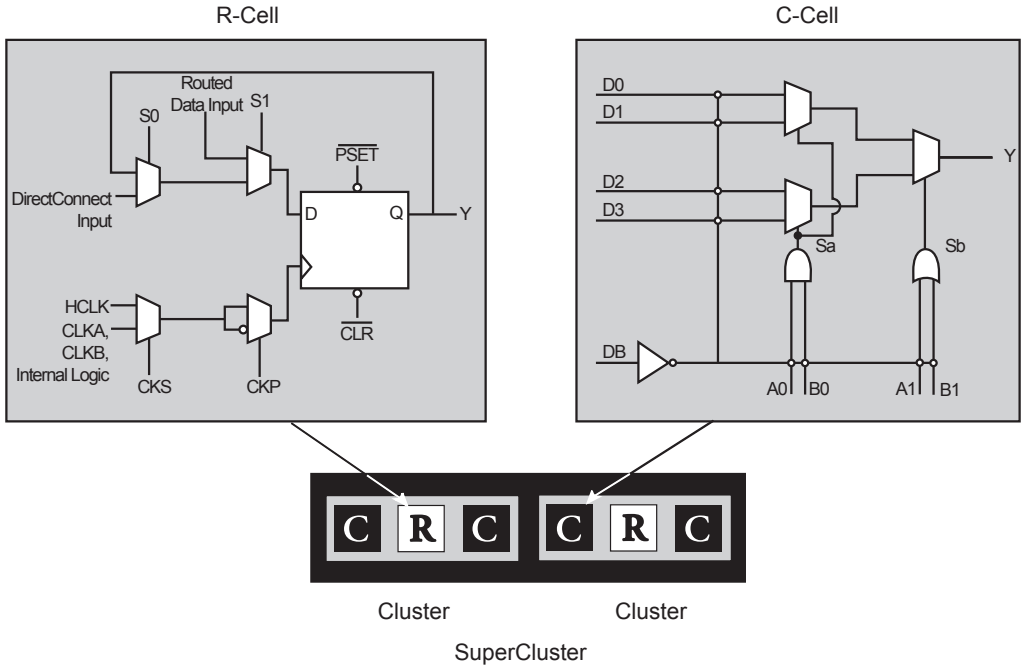
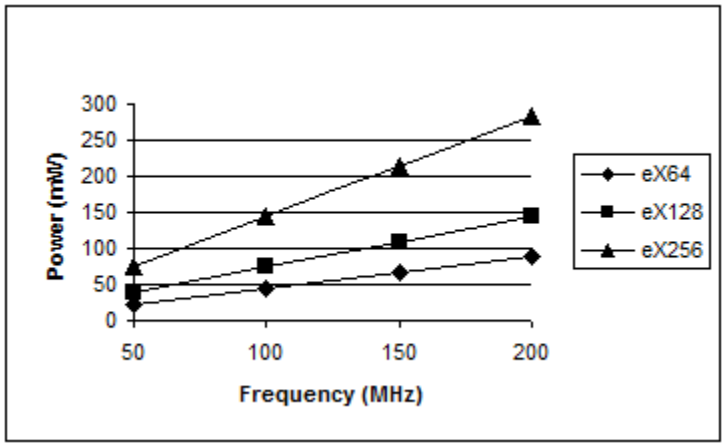


Figure 1-3 • **Cluster Organization**

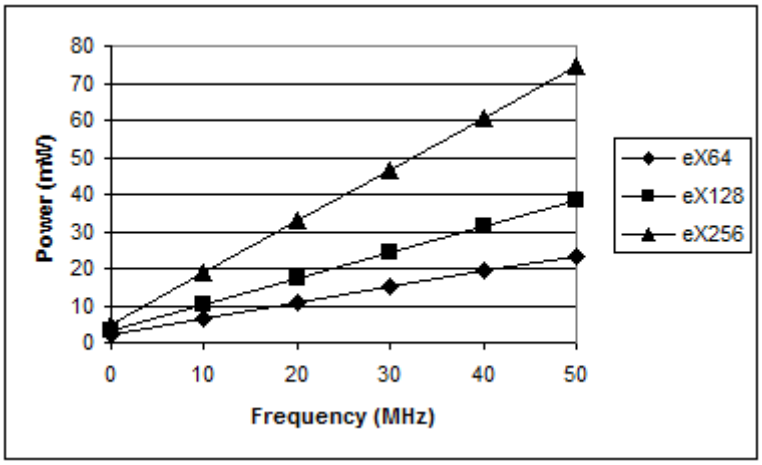
Figure 1-8 to Figure 1-11 on page 1-9 show some sample power characteristics of eX devices.



Notes:

1. *Device filled with 16-bit counters.*
2. *VCCA, VCCI = 2.7 V, device tested at room temperature.*

Figure 1-8 • **eX Dynamic Power Consumption – High Frequency**



Notes:

1. *Device filled with 16-bit counters.*
2. *VCCA, VCCI = 2.7 V, device tested at room temperature.*

Figure 1-9 • **eX Dynamic Power Consumption – Low Frequency**

Boundary Scan Testing (BST)

All eX devices are IEEE 1149.1 compliant. eX devices offer superior diagnostic and testing capabilities by providing Boundary Scan Testing (BST) and probing capabilities. These functions are controlled through the special test pins (TMS, TDI, TCK, TDO and TRST). The functionality of each pin is defined by two available modes: Dedicated and Flexible, and is described in Table 1-4. In the dedicated test mode, TCK, TDI, and TDO are dedicated pins and cannot be used as regular I/Os. In flexible mode (default mode), TMS should be set HIGH through a pull-up resistor of 10 kΩ. TMS can be pulled LOW to initiate the test sequence.

Table 1-4 • **Boundary Scan Pin Functionality**

Dedicated Test Mode	Flexible Mode
TCK, TDI, TDO are dedicated BST pins	TCK, TDI, TDO are flexible and may be used as I/Os
No need for pull-up resistor for TMS and TDI	Use a pull-up resistor of 10 kΩ on TMS

Dedicated Test Mode

In Dedicated mode, all JTAG pins are reserved for BST; designers cannot use them as regular I/Os. An internal pull-up resistor is automatically enabled on both TMS and TDI pins, and the TMS pin will function as defined in the IEEE 1149.1 (JTAG) specification.

To select Dedicated mode, users need to reserve the JTAG pins in Microsemi's Designer software by checking the **Reserve JTAG** box in the Device Selection Wizard (Figure 1-12). JTAG pins comply with LVTTL/TTL I/O specification regardless of whether they are used as a user I/O or a JTAG I/O. Refer to the "3.3 V LVTTL Electrical Specifications" section and "5.0 V TTL Electrical Specifications" section on page 1-18 for detailed specifications.

Figure 1-12 • **Device Selection Wizard**

Flexible Mode

In Flexible Mode, TDI, TCK and TDO may be used as either user I/Os or as JTAG input pins. The internal resistors on the TMS and TDI pins are disabled in flexible JTAG mode, and an external 10 kΩ pull-resistor to V_{CCI} is required on the TMS pin.

To select the Flexible mode, users need to clear the check box for **Reserve JTAG** in the Device Selection Wizard in Microsemi's Designer software. The functionality of TDI, TCK, and TDO pins is controlled by the BST TAP controller. The TAP controller receives two control inputs, TMS and TCK. Upon power-up, the TAP controller enters the Test-Logic-Reset state. In this state, TDI, TCK, and TDO function as user I/Os. The TDI, TCK, and TDO pins are transformed from user I/Os into BST pins when the TMS pin is LOW at the first rising edge of TCK. The TDI, TCK, and TDO pins return to user I/Os when TMS is held HIGH for at least five TCK cycles.

Programming

Device programming is supported through Silicon Sculptor series of programmers. In particular, Silicon Sculptor II is a compact, robust, single-site and multi-site device programmer for the PC.

With standalone software, Silicon Sculptor II allows concurrent programming of multiple units from the same PC, ensuring the fastest programming times possible. Each fuse is subsequently verified by Silicon Sculptor II to insure correct programming. In addition, integrity tests ensure that no extra fuses are programmed. Silicon Sculptor II also provides extensive hardware self-testing capability.

The procedure for programming an eX device using Silicon Sculptor II is as follows:

1. Load the *.AFM file
2. Select the device to be programmed
3. Begin programming

When the design is ready to go to production, Microsemi offers device volume-programming services either through distribution partners or via in-house programming from the factory.

For more details on programming eX devices, please refer to the *Programming Antifuse Devices* application note and the *Silicon Sculptor II User's Guide*.

Probing Capabilities

eX devices provide internal probing capability that is accessed with the JTAG pins. The Silicon Explorer II Diagnostic hardware is used to control the TDI, TCK, TMS and TDO pins to select the desired nets for debugging. The user simply assigns the selected internal nets in the Silicon Explorer II software to the PRA/PRB output pins for observation. Probing functionality is activated when the BST pins are in JTAG mode and the TRST pin is driven HIGH or left floating. If the TRST pin is held LOW, the TAP controller will remain in the Test-Logic-Reset state so no probing can be performed. The Silicon Explorer II automatically places the device into JTAG mode, but the user must drive the TRST pin HIGH or allow the internal pull-up resistor to pull TRST HIGH.

When you select the **Reserve Probe Pin** box, as shown in Figure 1-12 on page 1-10, the layout tool reserves the PRA and PRB pins as dedicated outputs for probing. This reserve option is merely a guideline. If the Layout tool requires that the PRA and PRB pins be user I/Os to achieve successful layout, the tool will use these pins for user I/Os. If you assign user I/Os to the PRA and PRB pins and select the **Reserve Probe Pin** option, Designer Layout will override the "Reserve Probe Pin" option and place your user I/Os on those pins.

To allow for probing capabilities, the security fuse must not be programmed. Programming the security fuse will disable the probe circuitry. Table 1-8 on page 1-13 summarizes the possible device configurations for probing once the device leaves the Test-Logic-Reset JTAG state.

Silicon Explorer II Probe

Silicon Explorer II is an integrated hardware and software solution that, in conjunction with Microsemi Designer software tools, allow users to examine any of the internal nets of the device while it is operating in a prototype or a production system. The user can probe into an eX device via the PRA and PRB pins without changing the placement and routing of the design and without using any additional resources. Silicon Explorer II's noninvasive method does not alter timing or loading effects, thus shortening the debug cycle.

Silicon Explorer II does not require re-layout or additional MUXes to bring signals out to an external pin, which is necessary when using programmable logic devices from other suppliers.

Silicon Explorer II samples data at 100 MHz (asynchronous) or 66 MHz (synchronous). Silicon Explorer II attaches to a PC's standard COM port, turning the PC into a fully functional 18-channel logic analyzer. Silicon Explorer II allows designers to complete the design verification process at their desks and reduces verification time from several hours per cycle to a few seconds.

The Silicon Explorer II tool uses the boundary scan ports (TDI, TCK, TMS and TDO) to select the desired nets for verification. The selected internal nets are assigned to the PRA/PRB pins for observation. Figure 1-13 on page 1-13 illustrates the interconnection between Silicon Explorer II and the eX device to perform in-circuit verification.

Related Documents

Datasheet

eX Automotive Family FPGAs
www.microsemi.com/soc/documents/eX_Auto_DS.pdf

Application Notes

Maximizing Logic Utilization in eX, SX and SX-A FPGA Devices Using CC Macros
www.microsemi.com/soc/documents/CC_Macro_AN.pdf
Implementation of Security in Microsemi Antifuse FPGAs
www.microsemi.com/soc/documents/Antifuse_Security_AN.pdf
Microsemi eX, SX-A, and RT54SX-S I/Os
www.microsemi.com/soc/documents/antifuseIO_AN.pdf
Microsemi SX-A and RT54SX-S Devices in Hot-Swap and Cold-Sparing Applications
www.microsemi.com/soc/documents/HotSwapColdSparing_AN.pdf
Design For Low Power in Microsemi Antifuse FPGAs
www.microsemi.com/soc/documents/Low_Power_AN.pdf
Programming Antifuse Devices
www.microsemi.com/soc/documents/AntifuseProgram_AN.pdf

User Guides

Silicon Sculptor II User's Guide
www.microsemi.com/soc/documents/SiliSculptII_Sculpt3_ug.pdf

Miscellaneous

Libero IDE flow
www.microsemi.com/soc/products/tools/libero/flow.html

3.3 V LVTTL Electrical Specifications

Symbol	Parameter		Commercial		Industrial		Units
			Min.	Max.	Min.	Max.	
VOH	VCCI = MIN, VI = VIH or VIL	(IOH = –8 mA)	2.4		2.4		V
VOL	VCCI = MIN, VI = VIH or VIL	(IOL = 12 mA)		0.4		0.4	V
VIL	Input Low Voltage			0.8		0.8	V
VIH	Input High Voltage		2.0	VCCI +0.5	2.0	VCCI +0.5	V
IIL/ IIH	Input Leakage Current, VIN = VCCI or GND		–10	10	–10	10	µA
IOZ	3-State Output Leakage Current, VOUT = VCCI or GND		–10	10	–10	10	µA
t_R, $t_{F1,2}$	Input Transition Time			10		10	ns
C_{IO}	I/O Capacitance			10		10	pF
ICC[3,4]	Standby Current			1.5		10	mA
IV Curve	Can be derived from the IBIS model at www.microsemi.com/soc/custsup/models/ibis.html.						

Notes:

1. *t_R is the transition time from 0.8 V to 2.0 V.*
2. *t_F is the transition time from 2.0 V to 0.8 V.*
3. *ICC max Commercial –F = 5.0 mA*
4. *ICC = ICCI + ICCA*
5. *JTAG pins comply with LVTTL/TTL I/O specification regardless of whether they are used as a user I/O or a JTAG I/O.*

5.0 V TTL Electrical Specifications

Symbol	Parameter		Commercial		Industrial		Units
			Min.	Max.	Min.	Max.	
VOH	VCCI = MIN, VI = VIH or VIL	(IOH = –8 mA)	2.4		2.4		V
VOL	VCCI = MIN, VI = VIH or VIL	(IOL= 12 mA)		0.4		0.4	V
VIL	Input Low Voltage			0.8		0.8	V
VIH	Input High Voltage		2.0	VCCI +0.5	2.0	VCCI +0.5	V
IIL/ IIH	Input Leakage Current, VIN = VCCI or GND		–10	10	–10	10	µA
IOZ	3-State Output Leakage Current, VOUT = VCCI or GND		–10	10	–10	10	µA
t_R, $t_{F1,2}$	Input Transition Time			10		10	ns
C_{IO}	I/O Capacitance			10		10	pF
ICC[3,4]	Standby Current			15		20	mA
IV Curve	Can be derived from the IBIS model at www.microsemi.com/soc/custsup/models/ibis.html.						

Note:

1. *t_R is the transition time from 0.8 V to 2.0 V.*
2. *t_F is the transition time from 2.0 V to 0.8 V.*
3. *ICC max Commercial –F=20mA*
4. *ICC = ICCI + ICCA*
5. *JTAG pins comply with LVTTL/TTL I/O specification regardless of whether they are used as a user I/O or a JTAG I/O.*

The estimation of the dynamic power dissipation is a piece-wise linear summation of the power dissipation of each component.

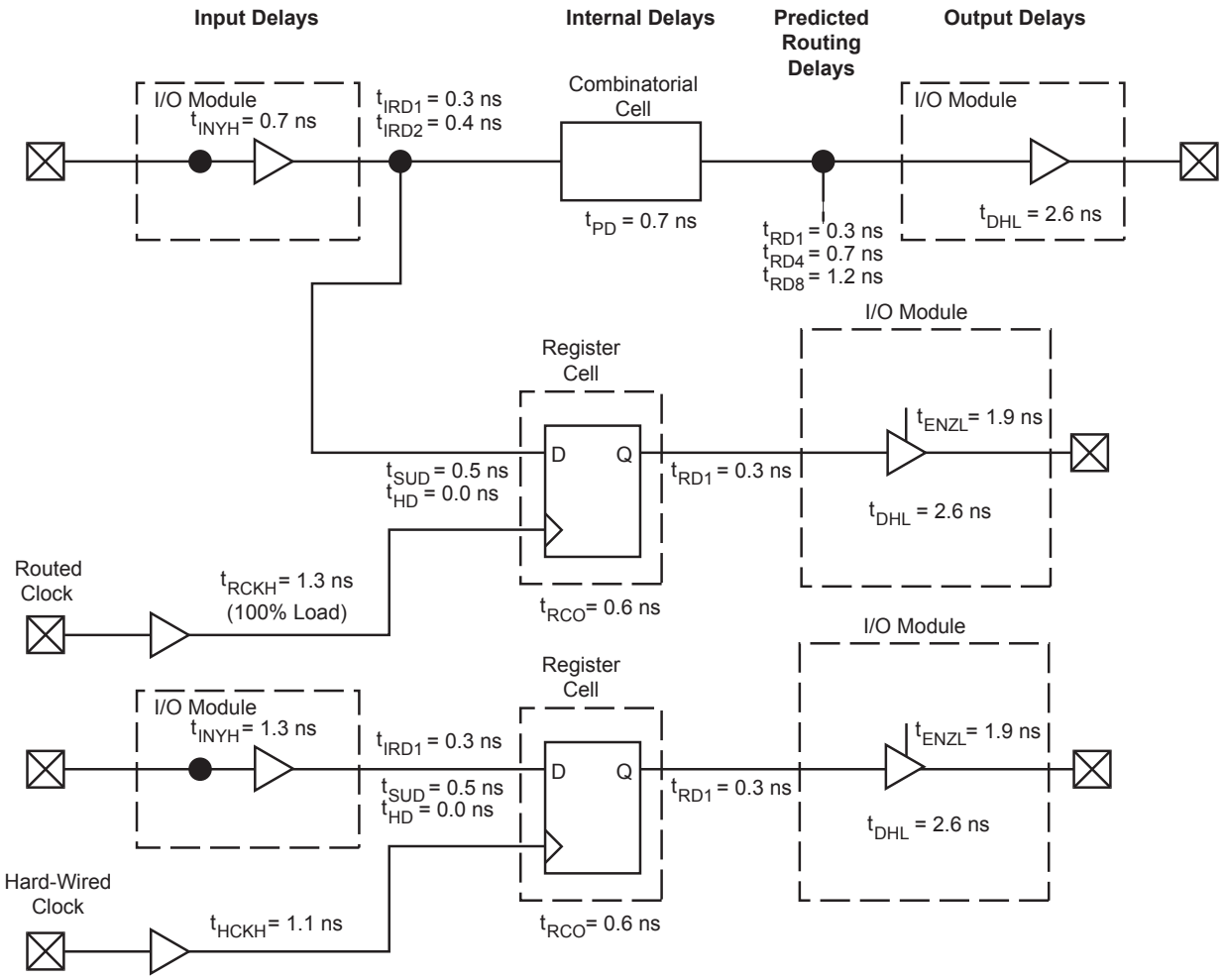
$$\text{Dynamic power dissipation} = VCCA^2 * [(m_c * C_{eqcm} * fm_C)_{\text{Comb Modules}} + (m_s * C_{eqsm} * fm_S)_{\text{Seq Modules}} + (n * C_{eqi} * fn)_{\text{Input Buffers}} + (0.5 * (q1 * C_{eqcr} * fq1) + (r1 * fq1))_{RCLKA} + (0.5 * (q2 * C_{eqcr} * fq2) + (r2 * fq2))_{RCLKB} + (0.5 * (s1 * C_{eqhv} * fs1)+(C_{eqhf} * fs1))_{HCLK}] + V_{CCI}^2 * [(p * (C_{eqo} + C_L) * fp)_{\text{Output Buffers}}]$$

where:

m_c = Number of combinatorial cells switching at frequency fm, typically 20% of C-cells
m_s = Number of sequential cells switching at frequency fm, typically 20% of R-cells
n = Number of input buffers switching at frequency fn, typically number of inputs / 4
p = Number of output buffers switching at frequency fp, typically number of outputs / 4
q1 = Number of R-cells driven by routed array clock A
q2 = Number of R-cells driven by routed array clock B
r1 = Fixed capacitance due to routed array clock A
r2 = Fixed capacitance due to routed array clock B
s1 = Number of R-cells driven by dedicated array clock
C_{eqcm} = Equivalent capacitance of combinatorial modules
C_{eqsm} = Equivalent capacitance of sequential modules
C_{eqi} = Equivalent capacitance of input buffers
C_{eqcr} = Equivalent capacitance of routed array clocks
C_{eqhv} = Variable capacitance of dedicated array clock
C_{eqhf} = Fixed capacitance of dedicated array clock
C_{eqo} = Equivalent capacitance of output buffers
C_L = Average output loading capacitance, typically 10 pF
fm_c = Average C-cell switching frequency, typically F/10
fm_s = Average R-cell switching frequency, typically F/10
fn = Average input buffer switching frequency, typically F/5
fp = Average output buffer switching frequency, typically F/5
fq1 = Frequency of routed clock A
fq2 = Frequency of routed clock B
fs1 = Frequency of dedicated array clock

The eX, SX-A and RTSX-S Power Calculator can be used to estimate the total power dissipation (static and dynamic) of eX devices: www.microsemi.com/soc/techdocs/calculators.aspx.

eX Timing Model



Note: Values shown for eX128–P, worst-case commercial conditions (5.0 V, 35 pF Pad Load).

Figure 1-14 • **eX Timing Model**

Hardwired Clock

External Setup = $t_{INYH} + t_{IRD1} + t_{SUD} – t_{HCKH}$

= 0.7 + 0.3 + 0.5 – 1.1 = 0.4 ns

Clock-to-Out (Pad-to-Pad), typical

= $t_{HCKH} + t_{RCO} + t_{RD1} + t_{DHL}$

= 1.1 + 0.6 + 0.3 + 2.6 = 4.6 ns

Routed Clock

External Setup = $t_{INYH} + t_{IRD2} + t_{SUD} – t_{RCKH}$

= 0.7 + 0.4 + 0.5 – 1.3= 0.3 ns

Clock-to-Out (Pad-to-Pad), typical

= $t_{RCKH} + t_{RCO} + t_{RD1} + t_{DHL}$

= 1.3+ 0.6 + 0.3 + 2.6 = 4.8 ns

Cell Timing Characteristics

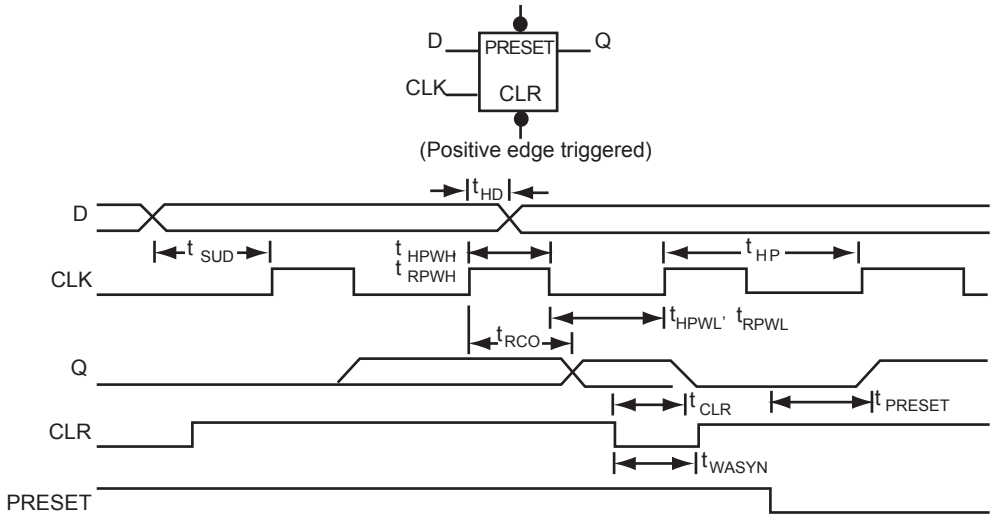


Figure 1-16 • **Flip-Flops**

eX Family Timing Characteristics

***Table 1-17* • eX Family Timing Characteristics**
(Worst-Case Commercial Conditions, VCCA = 2.3 V, T_J = 70°C)

		–P Speed		Std Speed		–F Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
C-Cell Propagation Delays[1]								
t_{PD}	Internal Array Module		0.7		1.0		1.4	ns
Predicted Routing Delays[2]								
t_{DC}	FO=1 Routing Delay, DirectConnect		0.1		0.1		0.2	ns
t_{FC}	FO=1 Routing Delay, FastConnect		0.3		0.5		0.7	ns
t_{RD1}	FO=1 Routing Delay		0.3		0.5		0.7	ns
t_{RD2}	FO=2 Routing Delay		0.4		0.6		0.8	ns
t_{RD3}	FO=3 Routing Delay		0.5		0.8		1.1	ns
t_{RD4}	FO=4 Routing Delay		0.7		1.0		1.3	ns
t_{RD8}	FO=8 Routing Delay		1.2		1.7		2.4	ns
t_{RD12}	FO=12 Routing Delay		1.7		2.5		3.5	ns
R-Cell Timing								
t_{RCO}	Sequential Clock-to-Q		0.6		0.9		1.3	ns
t_{CLR}	Asynchronous Clear-to-Q		0.6		0.8		1.2	ns
t_{PRESET}	Asynchronous Preset-to-Q		0.7		0.9		1.3	ns
t_{SUD}	Flip-Flop Data Input Set-Up	0.5		0.7		1.0		ns
t_{HD}	Flip-Flop Data Input Hold	0.0		0.0		0.0		ns
t_{WASYN}	Asynchronous Pulse Width	1.3		1.9		2.6		ns
$t_{RECASYN}$	Asynchronous Recovery Time	0.3		0.5		0.7		ns
t_{HASYN}	Asynchronous Hold Time	0.3		0.5		0.7		ns
2.5 V Input Module Propagation Delays								
t_{INYH}	Input Data Pad-to-Y HIGH		0.6		0.9		1.3	ns
t_{INYL}	Input Data Pad-to-Y LOW		0.8		1.1		1.5	ns
3.3 V Input Module Propagation Delays								
t_{INYH}	Input Data Pad-to-Y HIGH		0.7		1.0		1.4	ns
t_{INYL}	Input Data Pad-to-Y LOW		0.9		1.3		1.8	ns
5.0 V Input Module Propagation Delays								
t_{INYH}	Input Data Pad-to-Y HIGH		0.7		1.0		1.4	ns
t_{INYL}	Input Data Pad-to-Y LOW		0.9		1.3		1.8	ns
Input Module Predicted Routing Delays[2]								
t_{IRD1}	FO=1 Routing Delay		0.3		0.4		0.5	ns
t_{IRD2}	FO=2 Routing Delay		0.4		0.6		0.8	ns
t_{IRD3}	FO=3 Routing Delay		0.5		0.8		1.1	ns
t_{IRD4}	FO=4 Routing Delay		0.7		1.0		1.3	ns
t_{IRD8}	FO=8 Routing Delay		1.2		1.7		2.4	ns
t_{IRD12}	FO=12 Routing Delay		1.7		2.5		3.5	ns

Notes:

1. *For dual-module macros, use t_{PD} + t_{RD1} + t_{PDn}, t_{RCO} + t_{RD1} + t_{PDn} or t_{PD1} + t_{RD1} + t_{SUD}, whichever is appropriate.*
2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance.*

Table 1-18 • **eX Family Timing Characteristics**
(Worst-Case Commercial Conditions VCCA = 2.3 V, VCCI = 4.75 V, T_J = 70°C)

		–P Speed		Std Speed		–F Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Dedicated (Hard-Wired) Array Clock Networks								
t_{HCKH}	Input LOW to HIGH (Pad to R-Cell Input)		1.1		1.6		2.3	ns
t_{HCKL}	Input HIGH to LOW (Pad to R-Cell Input)		1.1		1.6		2.3	ns
t_{HPWH}	Minimum Pulse Width HIGH	1.4		2.0		2.8		ns
t_{HPWL}	Minimum Pulse Width LOW	1.4		2.0		2.8		ns
t_{HCKSW}	Maximum Skew		<0.1		<0.1		<0.1	ns
t_{HP}	Minimum Period	2.8		4.0		5.6		ns
f_{HMAX}	Maximum Frequency		357		250		178	MHz
Routed Array Clock Networks								
t_{RCKH}	Input LOW to HIGH (Light Load) (Pad to R-Cell Input) MAX.		1.1		1.6		2.2	ns
t_{RCKL}	Input HIGH to LOW (Light Load) (Pad to R-Cell Input) MAX.		1.0		1.4		2.0	ns
t_{RCKH}	Input LOW to HIGH (50% Load) (Pad to R-Cell Input) MAX.		1.2		1.7		2.4	ns
t_{RCKL}	Input HIGH to LOW (50% Load) (Pad to R-Cell Input) MAX.		1.2		1.7		2.4	ns
t_{RCKH}	Input LOW to HIGH (100% Load) (Pad to R-Cell Input) MAX.		1.3		1.9		2.6	ns
t_{RCKL}	Input HIGH to LOW (100% Load) (Pad to R-Cell Input) MAX.		1.3		1.9		2.6	ns
t_{RPWH}	Min. Pulse Width HIGH	1.5		2.1		3.0		ns
t_{RPWL}	Min. Pulse Width LOW	1.5		2.1		3.0		ns
t_{RCKSW}*	Maximum Skew (Light Load)		0.2		0.3		0.4	ns
t_{RCKSW}*	Maximum Skew (50% Load)		0.1		0.2		0.3	ns
t_{RCKSW}*	Maximum Skew (100% Load)		0.1		0.1		0.2	ns

*Note: *Clock skew improves as the clock network becomes more heavily loaded.*

Pin Description

CLKA/B **Routed Clock A and B**

These pins are clock inputs for clock distribution networks. Input levels are compatible with standard TTL or LVTTL specifications. The clock input is buffered prior to clocking the R-cells. If not used, this pin must be set LOW or HIGH on the board. It must not be left floating.

GND **Ground**

LOW supply voltage.

HCLK **Dedicated (Hardwired) Array Clock**

This pin is the clock input for sequential modules. Input levels are compatible with standard TTL or LVTTL specifications. This input is directly wired to each R-cell and offers clock speeds independent of the number of R-cells being driven. If not used, this pin must be set LOW or HIGH on the board. It must not be left floating.

I/O **Input/Output**

The I/O pin functions as an input, output, tristate, or bidirectional buffer. Based on certain configurations, input and output levels are compatible with standard TTL or LVTTL specifications. Unused I/O pins are automatically tristated by the Designer software.

LP **Low Power Pin**

Controls the low power mode of the eX devices. The device is placed in the low power mode by connecting the LP pin to logic HIGH. In low power mode, all I/Os are tristated, all input buffers are turned OFF, and the core of the device is turned OFF. To exit the low power mode, the LP pin must be set LOW. The device enters the low power mode 800 ns after the LP pin is driven to a logic HIGH. It will resume normal operation 200 µs after the LP pin is driven to a logic LOW. LP pin should not be left floating. Under normal operating condition it should be tied to GND via 10 kΩ resistor.

NC **No Connection**

This pin is not connected to circuitry within the device. These pins can be driven to any voltage or can be left floating with no effect on the operation of the device.

PRA/PRB, I/O **Probe A/B**

The Probe pin is used to output data from any user-defined design node within the device. This diagnostic pin can be used independently or in conjunction with the other probe pin to allow real-time diagnostic output of any signal path within the device. The Probe pin can be used as a user-defined I/O when verification has been completed. The pin's probe capabilities can be permanently disabled to protect programmed design confidentiality.

TCK, I/O **Test Clock**

Test clock input for diagnostic probe and device programming. In flexible mode, TCK becomes active when the TMS pin is set LOW (refer to Table 1-4 on page 1-10). This pin functions as an I/O when the boundary scan state machine reaches the "logic reset" state.

TDI, I/O **Test Data Input**

Serial input for boundary scan testing and diagnostic probe. In flexible mode, TDI is active when the TMS pin is set LOW (refer to Table 1-4 on page 1-10). This pin functions as an I/O when the boundary scan state machine reaches the "logic reset" state.

TDO, I/O **Test Data Output**

Serial output for boundary scan testing. In flexible mode, TDO is active when the TMS pin is set LOW (refer to Table 1-4 on page 1-10). This pin functions as an I/O when the boundary scan state machine reaches the "logic reset" state. When Silicon Explorer is being used, TDO will act as an output when the "checksum" command is run. It will return to user I/O when "checksum" is complete.

TQ64		
Pin Number	eX64 Function	eX128 Function
1	GND	GND
2	TDI, I/O	TDI, I/O
3	I/O	I/O
4	TMS	TMS
5	GND	GND
6	VCCI	VCCI
7	I/O	I/O
8	I/O	I/O
9	NC	I/O
10	NC	I/O
11	TRST, I/O	TRST, I/O
12	I/O	I/O
13	NC	I/O
14	GND	GND
15	I/O	I/O
16	I/O	I/O
17	I/O	I/O
18	I/O	I/O
19	VCCI	VCCI
20	I/O	I/O
21	PRB, I/O	PRB, I/O
22	VCCA	VCCA
23	GND	GND
24	I/O	I/O
25	HCLK	HCLK
26	I/O	I/O
27	I/O	I/O
28	I/O	I/O
29	I/O	I/O
30	I/O	I/O
31	I/O	I/O
32	TDO, I/O	TDO, I/O

TQ64		
Pin Number	eX64 Function	eX128 Function
33	GND	GND
34	I/O	I/O
35	I/O	I/O
36	VCCA	VCCA
37	VCCI	VCCI
38	I/O	I/O
39	I/O	I/O
40	NC	I/O
41	NC	I/O
42	I/O	I/O
43	I/O	I/O
44	VCCA	VCCA
45*	GND/LP	GND/ LP
46	GND	GND
47	I/O	I/O
48	I/O	I/O
49	I/O	I/O
50	I/O	I/O
51	I/O	I/O
52	VCCI	VCCI
53	I/O	I/O
54	I/O	I/O
55	CLKA	CLKA
56	CLKB	CLKB
57	VCCA	VCCA
58	GND	GND
59	PRA, I/O	PRA, I/O
60	I/O	I/O
61	VCCI	VCCI
62	I/O	I/O
63	I/O	I/O
64	TCK, I/O	TCK, I/O

*Note: *Please read the LP pin descriptions for restrictions on their use.*

3 – Datasheet Information

List of Changes

The following table lists critical changes that were made in the current version of the document.

Revision	Changes	Page
Revision 10 (October 2012)	The "User Security" section was revised to clarify that although no existing security measures can give an absolute guarantee, Microsemi FPGAs implement industry standard security (SAR 34677).	1-5
	Package names used in the "Product Profile" section and "Package Pin Assignments" section were revised to match standards given in *Package Mechanical Drawings* (SAR 34779).	I 2-1
Revision 9 (June 2011)	The versioning system for datasheets has been changed. Datasheets are assigned a revision number that increments each time the datasheet is revised. The "eX Device Status" table indicates the status for each device in the device family.	II
	The Chip Scale packages (CS49, CS128, CS181) are no longer offered for eX devices. They have been removed from the product family information. Pin tables for CSP packages have been removed from the datasheet (SAR 32002).	N/A
Revision 8 (v4.3, June 2006)	The "Ordering Information" was updated with RoHS information. The TQFP measurement was also updated.	II
	The "Dedicated Test Mode" was updated.	1-10
	Note 5 was added to the "3.3 V LVTTL Electrical Specifications" and "5.0 V TTL Electrical Specifications" tables	1-18
	The "LP Low Power Pin" description was updated.	1-31
Revision 7 (v4.2, June 2004)	The "eX Timing Model" was updated.	1-22
v4.1	The "Development Tool Support" section was updated.	1-13
	The "Package Thermal Characteristics" section was updated.	1-21
v4.0	The "Product Profile" section was updated.	1-I
	The "Ordering Information" section was updated.	1-II
	The "Temperature Grade Offerings" section is new.	1-III
	The "Speed Grade and Temperature Grade Matrix" section is new.	1-III
	The "eX FPGA Architecture and Characteristics" section was updated.	1-1
	The "Clock Resources" section was updated.	1-3
	Table 1-1 •Connections of Routed Clock Networks, CLKA and CLKB is new.	1-4
	The "User Security" section was updated.	1-5
	The "I/O Modules" section was updated.	1-5
	The "Hot-Swapping" section was updated.	1-6
	The "Power Requirements" section was updated.	1-6
	The "Low Power Mode" section was updated.	1-6
	The "Boundary Scan Testing (BST)" section was updated.	1-10
	The "Dedicated Test Mode" section was updated.	1-10

Revision	Changes	Page
v4.0 (continued)	The "Flexible Mode" section was updated.	1-10
	Table 1-5 •Boundary-Scan Pin Configurations and Functions is new.	1-11
	The "TRST Pin" section was updated.	1-11
	The "Probing Capabilities" section is new.	1-12
	The "Programming" section was updated.	1-12
	The "Probing Capabilities" section was updated.	1-12
	The "Silicon Explorer II Probe" section was updated.	1-12
	The "Design Considerations" section was updated.	1-13
	The "Development Tool Support" section was updated.	1-13
	The "Absolute Maximum Ratings*" section was updated.	1-16
	The "Temperature and Voltage Derating Factors" section was updated.	1-26
	The "TDI, I/O Test Data Input" section was updated.	1-31
	The "TDO, I/O Test Data Output" section was updated.	1-31
	The "TMS Test Mode Select" section was updated.	1-32
	The "TRST, I/O Boundary Scan Reset Pin" section was updated.	1-32
	All VSV pins were changed to VCCA. The change affected the following pins: 64-Pin TQFP – Pin 36 100-Pin TQFP – Pin 57 49-Pin CSP – Pin D5 128-Pin CSP– Pin H11 and Pin J1 for eX256 180-Pin CSP – Pins J12 and K2	
v3.0	The "Recommended Operating Conditions" section has been changed.	1-16
	The "3.3 V LVTTL Electrical Specifications" section has been updated.	1-18
	The "5.0 V TTL Electrical Specifications" section has been updated.	1-18
	The "Total Dynamic Power (mW)" section is new.	1-9
	The "System Power at 5%, 10%, and 15% Duty Cycle" section is new.	1-9
	The "eX Timing Model" section has been updated.	1-22
v2.0.1	The I/O Features table, Table 1-2 on page 1-6, was updated.	1-6
	The table, "Standby Power of eX Devices in LP Mode Typical Conditions, VCCA, VCCI = 2.5 V, TJ = 25° C" section, was updated.	1-7
	"Typical eX Standby Current at 25°C" section is a new table.	1-16
	The table in the section, "Package Thermal Characteristics" section has been updated for the 49-Pin CSP.	1-21
	The "eX Timing Model" section has been updated.	1-22
	The timing numbers found in, "eX Family Timing Characteristics" section have been updated.	1-27
	The V_{SV} pin has been added to the "Pin Description" section.	1-31
	Please see the following pin tables for the V_{SV} pin and an important footnote including the pin: "TQ64", "TQ100", "128-Pin CSP", and "180-Pin CSP".	2-1, 2-3, 2-6, 2-11
	The figure, "TQ64" section has been updated.	2-1

Revision	Changes	Page
Advance v0.4	In the Product Profile, the Maximum User I/Os for eX64 was changed to 84.	1-I
	In the Product Profile table, the Maximum User I/Os for eX128 was changed to 100.	1-I
Advance v0.3	The Mechanical Drawings section has been removed from the data sheet. The mechanical drawings are now contained in a separate document, “Package Characteristics and Mechanical Drawings,” available on the Actel web site.	
	A new section describing "Clock Resources"has been added.	1-3
	A new table describing "I/O Features"has been added.	1-6
	The "Pin Description"section has been updated and clarified.	1-31
	The original Electrical Specifications table was separated into two tables (2.5V and 3.3/5.0V). In both tables, several different currents are specified for V_{OH} and V_{OL}.	Page 8 and 9
	A new table listing 2.5V low power specifications and associated power graphs were added.	page 9
	Pin functions for eX256 TQ100 have been added to the "TQ100"table.	2-3
	A CS49 pin drawing and pin assignment table including eX64 and eX128 pin functions have been added.	page 26
	A CS128 pin drawing and pin assignment table including eX64, eX128, and eX256 pin functions have been added.	pages 26-27
	A CS180 pin drawing and pin assignment table for eX256 pin functions have been added.	pages 27, 31
Advance v0.2	The following table note was added to the eX Timing Characteristics table for clarification: Clock skew improves as the clock network becomes more heavily loaded.	pages 14-15

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