



Welcome to [E-XFL.COM](https://www.e-xfl.com)

Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

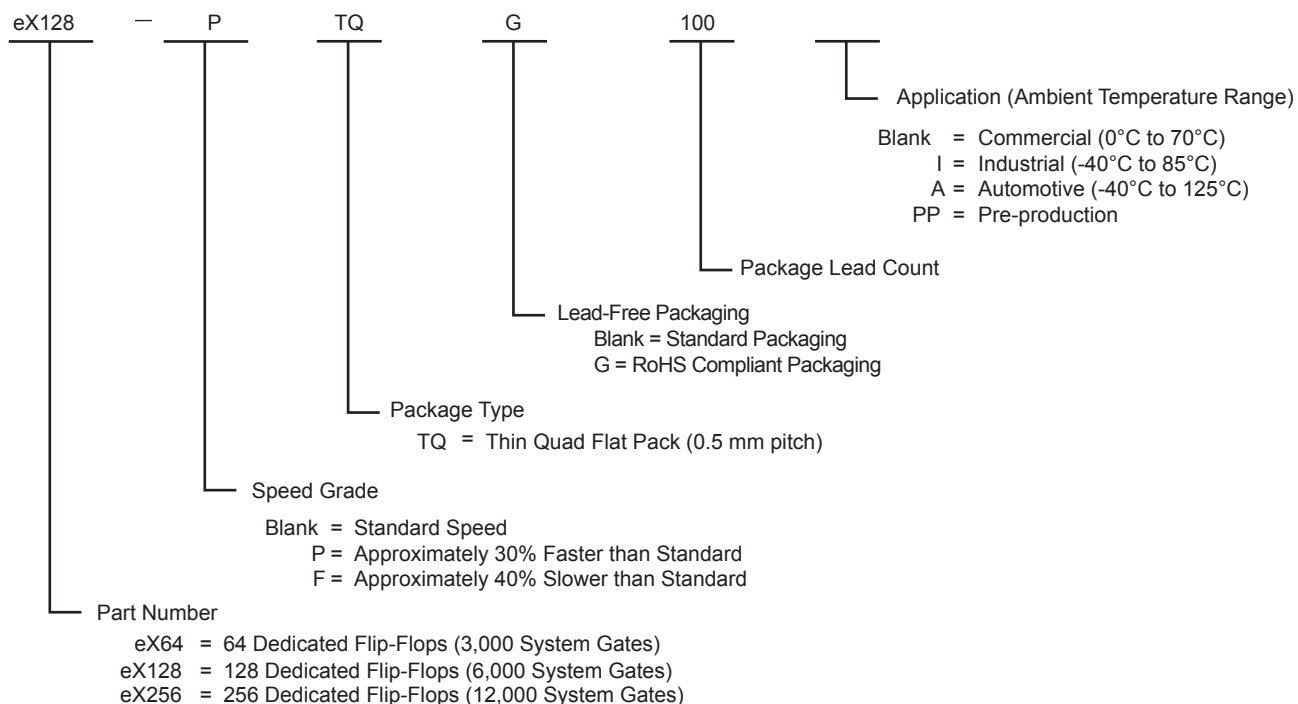
Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	128
Total RAM Bits	-
Number of I/O	41
Number of Gates	3000
Voltage - Supply	2.3V ~ 2.7V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	64-LQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/ex64-ptqg64

Ordering Information



eX Device Status

eX Devices	Status
eX64	Production
eX128	Production
eX256	Production

Plastic Device Resources

Device	User I/Os (Including Clock Buffers)	
	TQ64	TQ100
eX64	41	56
eX128	46	70
eX256	—	81

Note: TQ = Thin Quad Flat Pack

Module Organization

C-cell and R-cell logic modules are arranged into horizontal banks called Clusters, each of which contains two C-cells and one R-cell in a C-R-C configuration.

Clusters are further organized into modules called SuperClusters for improved design efficiency and device performance, as shown in [Figure 1-3](#). Each SuperCluster is a two-wide grouping of Clusters.

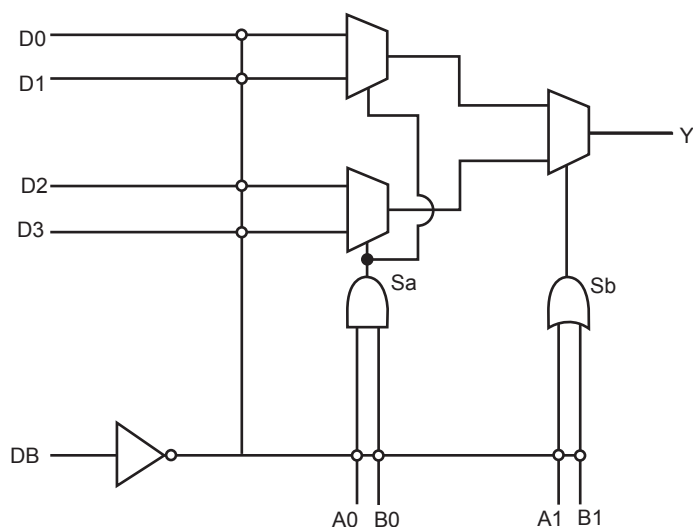


Figure 1-2 • C-Cell

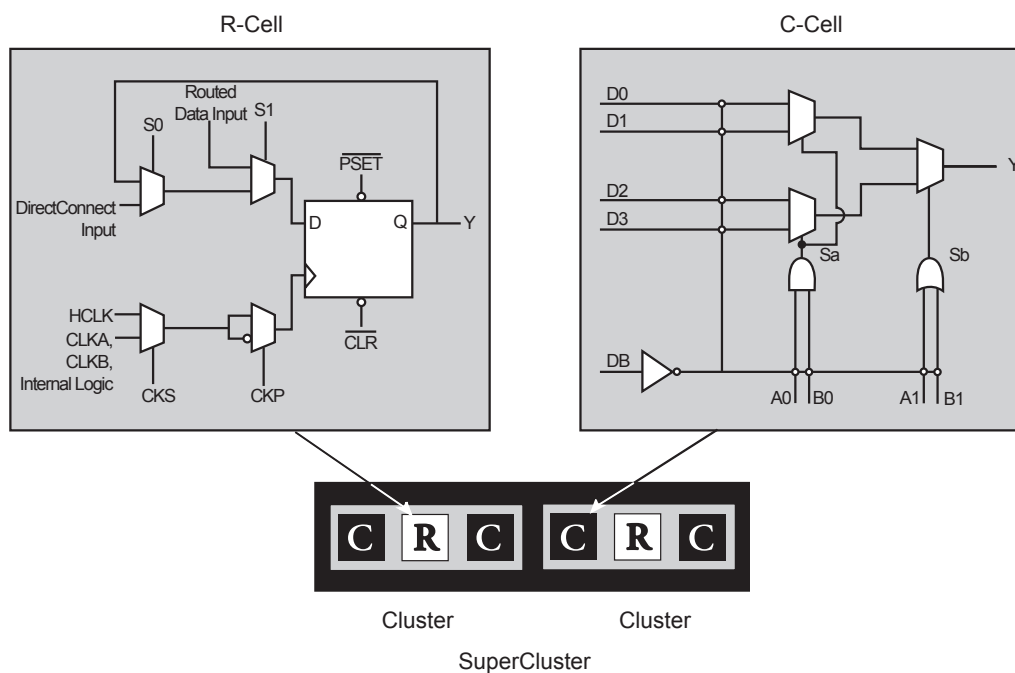


Figure 1-3 • Cluster Organization

Table 1-1 describes the possible connections of the routed clock networks, CLKA and CLKB. Unused clock pins must not be left floating and must be tied to HIGH or LOW.

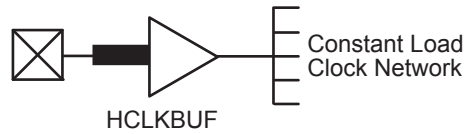


Figure 1-5 • eX HCLK Clock Pad

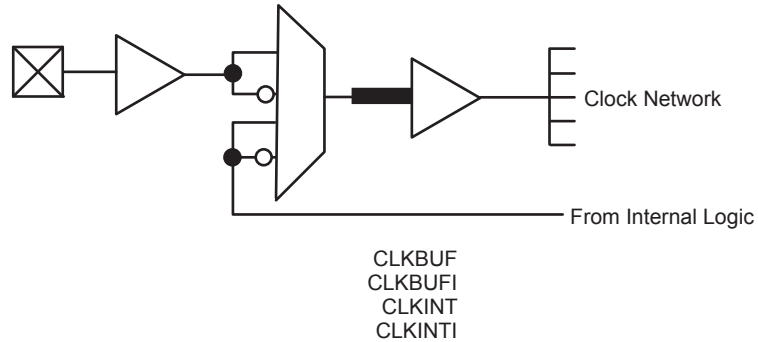
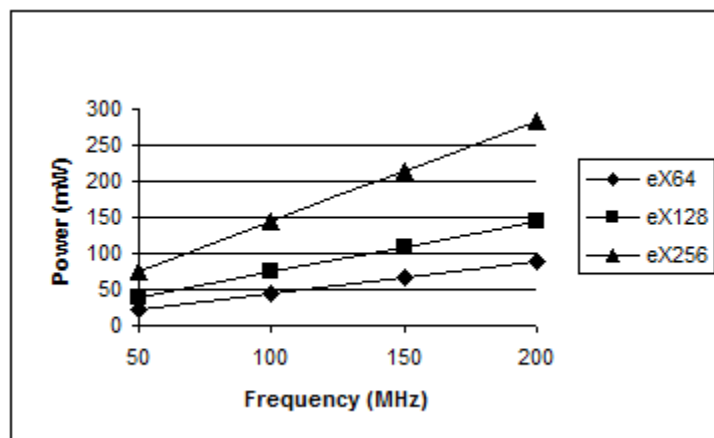


Figure 1-6 • eX Routed Clock Buffer

Table 1-1 • Connections of Routed Clock Networks, CLKA and CLKB

Module	Pins
C-Cell	A0, A1, B0 and B1
R-Cell	CLKA, CLKB, S0, S1, PSET, and CLR
I/O-Cell	EN

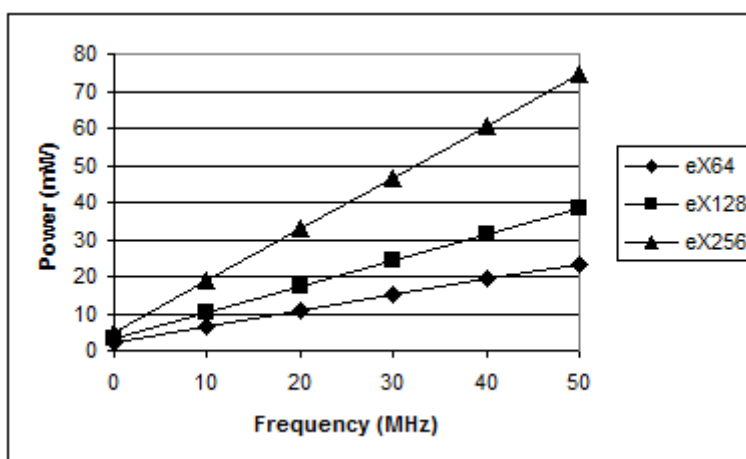
Figure 1-8 to Figure 1-11 on page 1-9 show some sample power characteristics of eX devices.



Notes:

1. Device filled with 16-bit counters.
2. VCCA, VCCI = 2.7 V, device tested at room temperature.

Figure 1-8 • eX Dynamic Power Consumption – High Frequency



Notes:

1. Device filled with 16-bit counters.
2. VCCA, VCCI = 2.7 V, device tested at room temperature.

Figure 1-9 • eX Dynamic Power Consumption – Low Frequency

Boundary Scan Testing (BST)

All eX devices are IEEE 1149.1 compliant. eX devices offer superior diagnostic and testing capabilities by providing Boundary Scan Testing (BST) and probing capabilities. These functions are controlled through the special test pins (TMS, TDI, TCK, TDO and TRST). The functionality of each pin is defined by two available modes: Dedicated and Flexible, and is described in [Table 1-4](#). In the dedicated test mode, TCK, TDI, and TDO are dedicated pins and cannot be used as regular I/Os. In flexible mode (default mode), TMS should be set HIGH through a pull-up resistor of 10 k Ω . TMS can be pulled LOW to initiate the test sequence.

Table 1-4 • Boundary Scan Pin Functionality

Dedicated Test Mode	Flexible Mode
TCK, TDI, TDO are dedicated BST pins	TCK, TDI, TDO are flexible and may be used as I/Os
No need for pull-up resistor for TMS and TDI	Use a pull-up resistor of 10 k Ω on TMS

Dedicated Test Mode

In Dedicated mode, all JTAG pins are reserved for BST; designers cannot use them as regular I/Os. An internal pull-up resistor is automatically enabled on both TMS and TDI pins, and the TMS pin will function as defined in the IEEE 1149.1 (JTAG) specification.

To select Dedicated mode, users need to reserve the JTAG pins in Microsemi's Designer software by checking the **Reserve JTAG** box in the Device Selection Wizard ([Figure 1-12](#)). JTAG pins comply with LVTTTL/TTL I/O specification regardless of whether they are used as a user I/O or a JTAG I/O. Refer to the ["3.3 V LVTTTL Electrical Specifications"](#) section and ["5.0 V TTL Electrical Specifications"](#) section on [page 1-18](#) for detailed specifications.



Figure 1-12 • Device Selection Wizard

Flexible Mode

In Flexible Mode, TDI, TCK and TDO may be used as either user I/Os or as JTAG input pins. The internal resistors on the TMS and TDI pins are disabled in flexible JTAG mode, and an external 10 k Ω pull-resistor to V_{CC1} is required on the TMS pin.

To select the Flexible mode, users need to clear the check box for **Reserve JTAG** in the Device Selection Wizard in Microsemi's Designer software. The functionality of TDI, TCK, and TDO pins is controlled by the BST TAP controller. The TAP controller receives two control inputs, TMS and TCK. Upon power-up, the TAP controller enters the Test-Logic-Reset state. In this state, TDI, TCK, and TDO function as user I/Os. The TDI, TCK, and TDO pins are transformed from user I/Os into BST pins when the TMS pin is LOW at the first rising edge of TCK. The TDI, TCK, and TDO pins return to user I/Os when TMS is held HIGH for at least five TCK cycles.

Programming

Device programming is supported through Silicon Sculptor series of programmers. In particular, Silicon Sculptor II is a compact, robust, single-site and multi-site device programmer for the PC.

With standalone software, Silicon Sculptor II allows concurrent programming of multiple units from the same PC, ensuring the fastest programming times possible. Each fuse is subsequently verified by Silicon Sculptor II to insure correct programming. In addition, integrity tests ensure that no extra fuses are programmed. Silicon Sculptor II also provides extensive hardware self-testing capability.

The procedure for programming an eX device using Silicon Sculptor II is as follows:

1. Load the *.AFM file
2. Select the device to be programmed
3. Begin programming

When the design is ready to go to production, Microsemi offers device volume-programming services either through distribution partners or via in-house programming from the factory.

For more details on programming eX devices, please refer to the [Programming Antifuse Devices](#) application note and the [Silicon Sculptor II User's Guide](#).

Probing Capabilities

eX devices provide internal probing capability that is accessed with the JTAG pins. The Silicon Explorer II Diagnostic hardware is used to control the TDI, TCK, TMS and TDO pins to select the desired nets for debugging. The user simply assigns the selected internal nets in the Silicon Explorer II software to the PRA/PRB output pins for observation. Probing functionality is activated when the BST pins are in JTAG mode and the TRST pin is driven HIGH or left floating. If the TRST pin is held LOW, the TAP controller will remain in the Test-Logic-Reset state so no probing can be performed. The Silicon Explorer II automatically places the device into JTAG mode, but the user must drive the TRST pin HIGH or allow the internal pull-up resistor to pull TRST HIGH.

When you select the **Reserve Probe Pin** box, as shown in [Figure 1-12 on page 1-10](#), the layout tool reserves the PRA and PRB pins as dedicated outputs for probing. This reserve option is merely a guideline. If the Layout tool requires that the PRA and PRB pins be user I/Os to achieve successful layout, the tool will use these pins for user I/Os. If you assign user I/Os to the PRA and PRB pins and select the **Reserve Probe Pin** option, Designer Layout will override the "Reserve Probe Pin" option and place your user I/Os on those pins.

To allow for probing capabilities, the security fuse must not be programmed. Programming the security fuse will disable the probe circuitry. [Table 1-8 on page 1-13](#) summarizes the possible device configurations for probing once the device leaves the Test-Logic-Reset JTAG state.

Silicon Explorer II Probe

Silicon Explorer II is an integrated hardware and software solution that, in conjunction with Microsemi Designer software tools, allow users to examine any of the internal nets of the device while it is operating in a prototype or a production system. The user can probe into an eX device via the PRA and PRB pins without changing the placement and routing of the design and without using any additional resources. Silicon Explorer II's noninvasive method does not alter timing or loading effects, thus shortening the debug cycle.

Silicon Explorer II does not require re-layout or additional MUXes to bring signals out to an external pin, which is necessary when using programmable logic devices from other suppliers.

Silicon Explorer II samples data at 100 MHz (asynchronous) or 66 MHz (synchronous). Silicon Explorer II attaches to a PC's standard COM port, turning the PC into a fully functional 18-channel logic analyzer. Silicon Explorer II allows designers to complete the design verification process at their desks and reduces verification time from several hours per cycle to a few seconds.

The Silicon Explorer II tool uses the boundary scan ports (TDI, TCK, TMS and TDO) to select the desired nets for verification. The selected internal nets are assigned to the PRA/PRB pins for observation. [Figure 1-13 on page 1-13](#) illustrates the interconnection between Silicon Explorer II and the eX device to perform in-circuit verification.

Designer software is a place-and-route tool and provides a comprehensive suite of backend support tools for FPGA development. The Designer software includes timing-driven place-and-route, and a world-class integrated static timing analyzer and constraints editor. With the Designer software, a user can lock his/her design pins before layout while minimally impacting the results of place-and-route. Additionally, the back-annotation flow is compatible with all the major simulators and the simulation results can be cross-probed with Silicon Explorer II, Microsemi integrated verification and logic analysis tool. Another tool included in the Designer software is the SmartGen core generator, which easily creates popular and commonly used logic functions for implementation into your schematic or HDL design. Microsemi's Designer software is compatible with the most popular FPGA design entry and verification tools from companies such as Mentor Graphics, Synplicity, Synopsys, and Cadence Design Systems. The Designer software is available for both the Windows and UNIX operating systems.

The estimation of the dynamic power dissipation is a piece-wise linear summation of the power dissipation of each component.

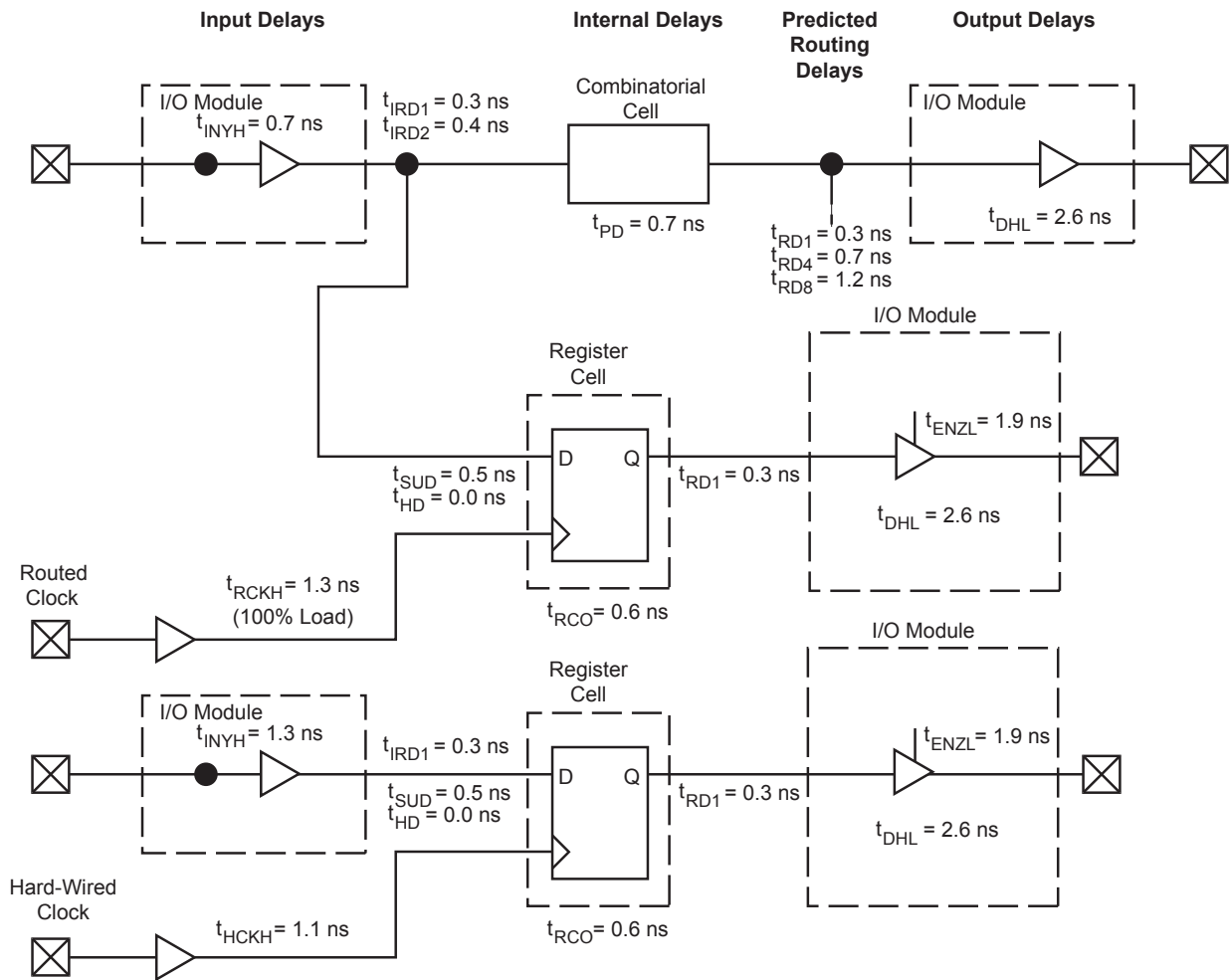
$$\begin{aligned} \text{Dynamic power dissipation} = & V_{CCA}^2 * [(m_c * C_{eqcm} * f_{mC})_{\text{Comb Modules}} + (m_s * C_{eqsm} * f_{mS})_{\text{Seq Modules}} \\ & + (n * C_{eqi} * f_n)_{\text{Input Buffers}} + (0.5 * (q1 * C_{eqcr} * f_{q1}) + (r1 * f_{q1}))_{\text{RCLKA}} + (0.5 * (q2 * C_{eqcr} * f_{q2}) \\ & + (r2 * f_{q2}))_{\text{RCLKB}} + (0.5 * (s1 * C_{eqhv} * f_{s1}) + (C_{eqhf} * f_{s1}))_{\text{HCLK}}] + V_{CCI}^2 * [(p * (C_{eqo} + C_L) \\ & * f_p)_{\text{Output Buffers}}] \end{aligned}$$

where:

- m_c = Number of combinatorial cells switching at frequency f_m , typically 20% of C-cells
- m_s = Number of sequential cells switching at frequency f_m , typically 20% of R-cells
- n = Number of input buffers switching at frequency f_n , typically number of inputs / 4
- p = Number of output buffers switching at frequency f_p , typically number of outputs / 4
- $q1$ = Number of R-cells driven by routed array clock A
- $q2$ = Number of R-cells driven by routed array clock B
- $r1$ = Fixed capacitance due to routed array clock A
- $r2$ = Fixed capacitance due to routed array clock B
- $s1$ = Number of R-cells driven by dedicated array clock
- C_{eqcm} = Equivalent capacitance of combinatorial modules
- C_{eqsm} = Equivalent capacitance of sequential modules
- C_{eqi} = Equivalent capacitance of input buffers
- C_{eqcr} = Equivalent capacitance of routed array clocks
- C_{eqhv} = Variable capacitance of dedicated array clock
- C_{eqhf} = Fixed capacitance of dedicated array clock
- C_{eqo} = Equivalent capacitance of output buffers
- C_L = Average output loading capacitance, typically 10 pF
- f_{mC} = Average C-cell switching frequency, typically $F/10$
- f_{mS} = Average R-cell switching frequency, typically $F/10$
- f_n = Average input buffer switching frequency, typically $F/5$
- f_p = Average output buffer switching frequency, typically $F/5$
- f_{q1} = Frequency of routed clock A
- f_{q2} = Frequency of routed clock B
- f_{s1} = Frequency of dedicated array clock

The eX, SX-A and RTSX-S Power Calculator can be used to estimate the total power dissipation (static and dynamic) of eX devices: www.microsemi.com/soc/techdocs/calculators.aspx.

eX Timing Model



Note: Values shown for eX128-P, worst-case commercial conditions (5.0 V, 35 pF Pad Load).

Figure 1-14 • eX Timing Model

Hardwired Clock

$$\text{External Setup} = t_{INYH} + t_{IRD1} + t_{SUD} - t_{HCKH}$$

$$= 0.7 + 0.3 + 0.5 - 1.1 = 0.4 \text{ ns}$$

Clock-to-Out (Pad-to-Pad), typical

$$= t_{HCKH} + t_{RCO} + t_{RD1} + t_{DHL}$$

$$= 1.1 + 0.6 + 0.3 + 2.6 = 4.6 \text{ ns}$$

Routed Clock

$$\text{External Setup} = t_{INYH} + t_{IRD2} + t_{SUD} - t_{RCKH}$$

$$= 0.7 + 0.4 + 0.5 - 1.3 = 0.3 \text{ ns}$$

Clock-to-Out (Pad-to-Pad), typical

$$= t_{RCKH} + t_{RCO} + t_{RD1} + t_{DHL}$$

$$= 1.3 + 0.6 + 0.3 + 2.6 = 4.8 \text{ ns}$$

Input Buffer Delays

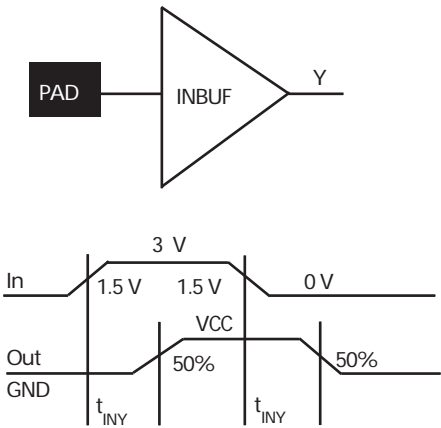


Table 1-14 • Input Buffer Delays

C-Cell Delays

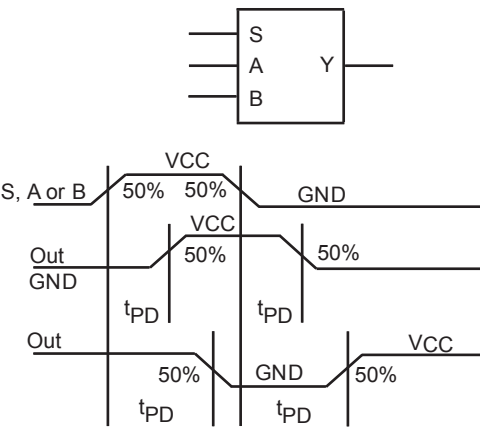


Table 1-15 • C-Cell Delays

Cell Timing Characteristics

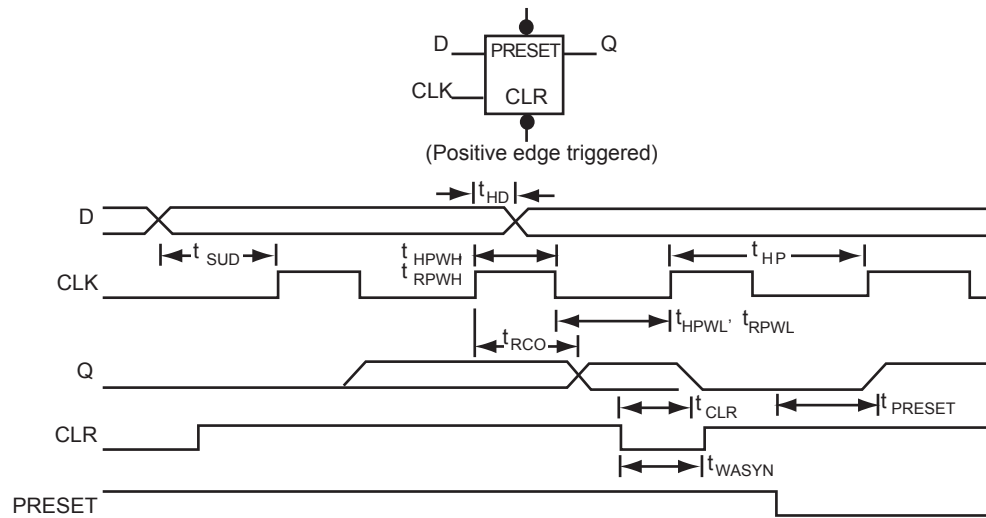


Figure 1-16 • Flip-Flops

Timing Characteristics

Timing characteristics for eX devices fall into three categories: family-dependent, device-dependent, and design-dependent. The input and output buffer characteristics are common to all eX family members. Internal routing delays are device-dependent. Design dependency means actual delays are not determined until after placement and routing of the user's design are complete. Delay values may then be determined by using the Timer utility or performing simulation with post-layout delays.

Critical Nets and Typical Nets

Propagation delays are expressed only for typical nets, which are used for initial design performance evaluation. Critical net delays can then be applied to the most timing critical paths. Critical nets are determined by net property assignment prior to placement and routing. Up to six percent of the nets in a design may be designated as critical.

Long Tracks

Some nets in the design use long tracks. Long tracks are special routing resources that span multiple rows, columns, or modules. Long tracks employ three to five antifuse connections. This increases capacitance and resistance, resulting in longer net delays for macros connected to long tracks. Typically, no more than six percent of nets in a fully utilized device require long tracks. Long tracks contribute approximately 4 ns to 8.4 ns delay. This additional delay is represented statistically in higher fanout routing delays.

Timing Derating

eX devices are manufactured with a CMOS process. Therefore, device performance varies according to temperature, voltage, and process changes. Minimum timing parameters reflect maximum operating voltage, minimum operating temperature, and best-case processing. Maximum timing parameters reflect minimum operating voltage, maximum operating temperature, and worst-case processing.

Temperature and Voltage Derating Factors

Table 1-16 • Temperature and Voltage Derating Factors
(Normalized to Worst-Case Commercial, $T_J = 70^\circ\text{C}$, $V_{CCA} = 2.3\text{V}$)

VCCA	Junction Temperature (T_J)						
	-55	-40	0	25	70	85	125
2.3	0.79	0.80	0.87	0.88	1.00	1.04	1.13
2.5	0.74	0.74	0.81	0.83	0.93	0.97	1.06
2.7	0.69	0.70	0.76	0.78	0.88	0.91	1.00

Table 1-20 • eX Family Timing Characteristics
(Worst-Case Commercial Conditions VCCA = 2.3 V, T_J = 70°C)

		–P Speed		Std Speed		–F Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Units
2.5 V LVCMOS Output Module Timing¹ (VCCI = 2.3 V)								
t _{DLH}	Data-to-Pad LOW to HIGH		3.3		4.7		6.6	ns
t _{DHL}	Data-to-Pad HIGH to LOW		3.5		5.0		7.0	ns
t _{DHLS}	Data-to-Pad HIGH to LOW—Low Slew		11.6		16.6		23.2	ns
t _{ENZL}	Enable-to-Pad, Z to L		2.5		3.6		5.1	ns
t _{ENZLS}	Enable-to-Pad Z to L—Low Slew		11.8		16.9		23.7	ns
t _{ENZH}	Enable-to-Pad, Z to H		3.4		4.9		6.9	ns
t _{ENLZ}	Enable-to-Pad, L to Z		2.1		3.0		4.2	ns
t _{ENHZ}	Enable-to-Pad, H to Z		2.4		5.67		7.94	ns
d _{TLH}	Delta Delay vs. Load LOW to HIGH		0.034		0.046		0.066	ns/pF
d _{THL}	Delta Delay vs. Load HIGH to LOW		0.016		0.022		0.05	ns/pF
d _{THLS}	Delta Delay vs. Load HIGH to LOW—Low Slew		0.05		0.072		0.1	ns/pF
3.3 V LVTTTL Output Module Timing¹ (VCCI = 3.0 V)								
t _{DLH}	Data-to-Pad LOW to HIGH		2.8		4.0		5.6	ns
t _{DHL}	Data-to-Pad HIGH to LOW		2.7		3.9		5.4	ns
t _{DHLS}	Data-to-Pad HIGH to LOW—Low Slew		9.7		13.9		19.5	ns
t _{ENZL}	Enable-to-Pad, Z to L		2.2		3.2		4.4	ns
t _{ENZLS}	Enable-to-Pad Z to L—Low Slew		9.7		13.9		19.6	ns
t _{ENZH}	Enable-to-Pad, Z to H		2.8		4.0		5.6	ns
t _{ENLZ}	Enable-to-Pad, L to Z		2.8		4.0		5.6	ns
t _{ENHZ}	Enable-to-Pad, H to Z		2.6		3.8		5.3	ns
d _{TLH}	Delta Delay vs. Load LOW to HIGH		0.02		0.03		0.046	ns/pF
d _{THL}	Delta Delay vs. Load HIGH to LOW		0.016		0.022		0.05	ns/pF
d _{THLS}	Delta Delay vs. Load HIGH to LOW—Low Slew		0.05		0.072		0.1	ns/pF
5.0 V TTL Output Module Timing* (VCCI = 4.75 V)								
t _{DLH}	Data-to-Pad LOW to HIGH		2.0		2.9		4.0	ns
t _{DHL}	Data-to-Pad HIGH to LOW		2.6		3.7		5.2	ns
t _{DHLS}	Data-to-Pad HIGH to LOW—Low Slew		6.8		9.7		13.6	ns
t _{ENZL}	Enable-to-Pad, Z to L		1.9		2.7		3.8	ns
t _{ENZLS}	Enable-to-Pad Z to L—Low Slew		6.8		9.8		13.7	ns
t _{ENZH}	Enable-to-Pad, Z to H		2.1		3.0		4.1	ns
t _{ENLZ}	Enable-to-Pad, L to Z		3.3		4.8		6.6	ns

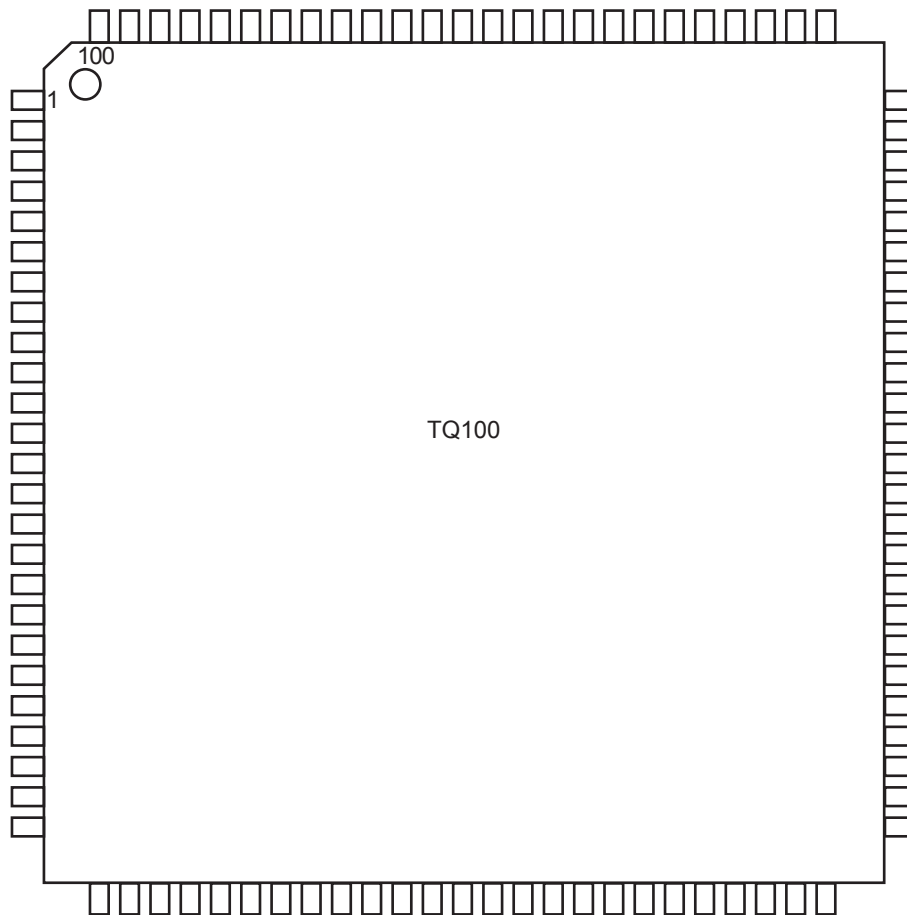
Note: *Delays based on 35 pF loading.

TQ64		
Pin Number	eX64 Function	eX128 Function
1	GND	GND
2	TDI, I/O	TDI, I/O
3	I/O	I/O
4	TMS	TMS
5	GND	GND
6	VCCI	VCCI
7	I/O	I/O
8	I/O	I/O
9	NC	I/O
10	NC	I/O
11	TRST, I/O	TRST, I/O
12	I/O	I/O
13	NC	I/O
14	GND	GND
15	I/O	I/O
16	I/O	I/O
17	I/O	I/O
18	I/O	I/O
19	VCCI	VCCI
20	I/O	I/O
21	PRB, I/O	PRB, I/O
22	VCCA	VCCA
23	GND	GND
24	I/O	I/O
25	HCLK	HCLK
26	I/O	I/O
27	I/O	I/O
28	I/O	I/O
29	I/O	I/O
30	I/O	I/O
31	I/O	I/O
32	TDO, I/O	TDO, I/O

TQ64		
Pin Number	eX64 Function	eX128 Function
33	GND	GND
34	I/O	I/O
35	I/O	I/O
36	VCCA	VCCA
37	VCCI	VCCI
38	I/O	I/O
39	I/O	I/O
40	NC	I/O
41	NC	I/O
42	I/O	I/O
43	I/O	I/O
44	VCCA	VCCA
45*	GND/LP	GND/ LP
46	GND	GND
47	I/O	I/O
48	I/O	I/O
49	I/O	I/O
50	I/O	I/O
51	I/O	I/O
52	VCCI	VCCI
53	I/O	I/O
54	I/O	I/O
55	CLKA	CLKA
56	CLKB	CLKB
57	VCCA	VCCA
58	GND	GND
59	PRA, I/O	PRA, I/O
60	I/O	I/O
61	VCCI	VCCI
62	I/O	I/O
63	I/O	I/O
64	TCK, I/O	TCK, I/O

Note: *Please read the LP pin descriptions for restrictions on their use.

TQ100



Note: For Package Manufacturing and Environmental information, visit Resource center at www.microsemi.com/soc/products/rescenter/package/index.html.

TQ100			
Pin Number	eX64 Function	eX128 Function	eX256 Function
1	GND	GND	GND
2	TDI, I/O	TDI, I/O	TDI, I/O
3	NC	NC	I/O
4	NC	NC	I/O
5	NC	NC	I/O
6	I/O	I/O	I/O
7	TMS	TMS	TMS
8	VCCI	VCCI	VCCI
9	GND	GND	GND
10	NC	I/O	I/O
11	NC	I/O	I/O
12	I/O	I/O	I/O
13	NC	I/O	I/O
14	I/O	I/O	I/O
15	NC	I/O	I/O
16	TRST, I/O	TRST, I/O	TRST, I/O
17	NC	I/O	I/O
18	I/O	I/O	I/O
19	NC	I/O	I/O
20	VCCI	VCCI	VCCI
21	I/O	I/O	I/O
22	NC	I/O	I/O
23	NC	NC	I/O
24	NC	NC	I/O
25	I/O	I/O	I/O
26	I/O	I/O	I/O
27	I/O	I/O	I/O
28	I/O	I/O	I/O
29	I/O	I/O	I/O
30	I/O	I/O	I/O
31	I/O	I/O	I/O
32	I/O	I/O	I/O
33	I/O	I/O	I/O
34	PRB, I/O	PRB, I/O	PRB, I/O
35	VCCA	VCCA	VCCA

TQ100			
Pin Number	eX64 Function	eX128 Function	eX256 Function
36	GND	GND	GND
37	NC	NC	NC
38	I/O	I/O	I/O
39	HCLK	HCLK	HCLK
40	I/O	I/O	I/O
41	I/O	I/O	I/O
42	I/O	I/O	I/O
43	I/O	I/O	I/O
44	VCCI	VCCI	VCCI
45	I/O	I/O	I/O
46	I/O	I/O	I/O
47	I/O	I/O	I/O
48	I/O	I/O	I/O
49	TDO, I/O	TDO, I/O	TDO, I/O
50	NC	I/O	I/O
51	GND	GND	GND
52	NC	NC	I/O
53	NC	NC	I/O
54	NC	NC	I/O
55	I/O	I/O	I/O
56	I/O	I/O	I/O
57	VCCA	VCCA	VCCA
58	VCCI	VCCI	VCCI
59	NC	I/O	I/O
60	I/O	I/O	I/O
61	NC	I/O	I/O
62	I/O	I/O	I/O
63	NC	I/O	I/O
64	I/O	I/O	I/O
65	NC	I/O	I/O
66	I/O	I/O	I/O
67	VCCA	VCCA	VCCA
68	GND/LP	GND/LP	GND/LP
69	GND	GND	GND
70	I/O	I/O	I/O

Note: *Please read the LP pin descriptions for restrictions on their use.

TQ100			
Pin Number	eX64 Function	eX128 Function	eX256 Function
71	I/O	I/O	I/O
72	NC	I/O	I/O
73	NC	NC	I/O
74	NC	NC	I/O
75	NC	NC	I/O
76	NC	I/O	I/O
77	I/O	I/O	I/O
78	I/O	I/O	I/O
79	I/O	I/O	I/O
80	I/O	I/O	I/O
81	I/O	I/O	I/O
82	VCCI	VCCI	VCCI
83	I/O	I/O	I/O
84	I/O	I/O	I/O
85	I/O	I/O	I/O
86	I/O	I/O	I/O
87	CLKA	CLKA	CLKA
88	CLKB	CLKB	CLKB
89	NC	NC	NC
90	VCCA	VCCA	VCCA
91	GND	GND	GND
92	PRA, I/O	PRA, I/O	PRA, I/O
93	I/O	I/O	I/O
94	I/O	I/O	I/O
95	I/O	I/O	I/O
96	I/O	I/O	I/O
97	I/O	I/O	I/O
98	I/O	I/O	I/O
99	I/O	I/O	I/O
100	TCK, I/O	TCK, I/O	TCK, I/O

Note: *Please read the LP pin descriptions for restrictions on their use.

3 – Datasheet Information

List of Changes

The following table lists critical changes that were made in the current version of the document.

Revision	Changes	Page
Revision 10 (October 2012)	The "User Security" section was revised to clarify that although no existing security measures can give an absolute guarantee, Microsemi FPGAs implement industry standard security (SAR 34677).	1-5
	Package names used in the "Product Profile" section and "Package Pin Assignments" section were revised to match standards given in <i>Package Mechanical Drawings</i> (SAR 34779).	I 2-1
Revision 9 (June 2011)	The versioning system for datasheets has been changed. Datasheets are assigned a revision number that increments each time the datasheet is revised. The "eX Device Status" table indicates the status for each device in the device family.	II
	The Chip Scale packages (CS49, CS128, CS181) are no longer offered for eX devices. They have been removed from the product family information. Pin tables for CSP packages have been removed from the datasheet (SAR 32002).	N/A
Revision 8 (v4.3, June 2006)	The "Ordering Information" was updated with RoHS information. The TQFP measurement was also updated.	II
	The "Dedicated Test Mode" was updated.	1-10
	Note 5 was added to the "3.3 V LVTTTL Electrical Specifications" and "5.0 V TTL Electrical Specifications" tables	1-18
	The "LP Low Power Pin" description was updated.	1-31
Revision 7 (v4.2, June 2004)	The "eX Timing Model" was updated.	1-22
v4.1	The "Development Tool Support" section was updated.	1-13
	The "Package Thermal Characteristics" section was updated.	1-21
v4.0	The "Product Profile" section was updated.	1-I
	The "Ordering Information" section was updated.	1-II
	The "Temperature Grade Offerings" section is new.	1-III
	The "Speed Grade and Temperature Grade Matrix" section is new.	1-III
	The "eX FPGA Architecture and Characteristics" section was updated.	1-1
	The "Clock Resources" section was updated.	1-3
	Table 1-1 •Connections of Routed Clock Networks, CLKA and CLKB is new.	1-4
	The "User Security" section was updated.	1-5
	The "I/O Modules" section was updated.	1-5
	The "Hot-Swapping" section was updated.	1-6
	The "Power Requirements" section was updated.	1-6
	The "Low Power Mode" section was updated.	1-6
	The "Boundary Scan Testing (BST)" section was updated.	1-10
	The "Dedicated Test Mode" section was updated.	1-10

Revision	Changes	Page
Advance v0.4	In the Product Profile , the Maximum User I/Os for eX64 was changed to 84.	1-I
	In the Product Profile table, the Maximum User I/Os for eX128 was changed to 100.	1-I
Advance v0.3	The Mechanical Drawings section has been removed from the data sheet. The mechanical drawings are now contained in a separate document, "Package Characteristics and Mechanical Drawings," available on the Actel web site.	
	A new section describing " Clock Resources " has been added.	1-3
	A new table describing " I/O Features " has been added.	1-6
	The " Pin Description " section has been updated and clarified.	1-31
	The original Electrical Specifications table was separated into two tables (2.5V and 3.3/5.0V). In both tables, several different currents are specified for V_{OH} and V_{OL} .	Page 8 and 9
	A new table listing 2.5V low power specifications and associated power graphs were added.	page 9
	Pin functions for eX256 TQ100 have been added to the " TQ100 " table.	2-3
	A CS49 pin drawing and pin assignment table including eX64 and eX128 pin functions have been added.	page 26
	A CS128 pin drawing and pin assignment table including eX64, eX128, and eX256 pin functions have been added.	pages 26-27
	A CS180 pin drawing and pin assignment table for eX256 pin functions have been added.	pages 27, 31
Advance v0.2	The following table note was added to the eX Timing Characteristics table for clarification: Clock skew improves as the clock network becomes more heavily loaded.	pages 14-15