Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	128
Total RAM Bits	-
Number of I/O	41
Number of Gates	3000
Voltage - Supply	2.3V ~ 2.7V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 85°C (TA)
Package / Case	64-LQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/ex64-ptqg64i

Temperature Grade Offerings

Device\ Package	TQ64	TQ100
eX64	C, I, A	C, I, A
eX128	C, I, A	C, I, A
eX256	C, I, A	C, I, A

Note: C = Commercial
I = Industrial
A = Automotive

Speed Grade and Temperature Grade Matrix

	–F	Std	–P
C	✓	✓	✓
I		✓	✓
A		✓	

Note: P = Approximately 30% faster than Standard
–F = Approximately 40% slower than Standard
Refer to the eX Automotive Family FPGAs datasheet for details on automotive temperature offerings.

Contact your local Microsemi representative for device availability.

Other Architectural Features

Performance

The combination of architectural features described above enables eX devices to operate with internal clock frequencies exceeding 350 MHz for very fast execution of complex logic functions. The eX family is an optimal platform upon which the functionality previously contained in CPLDs can be integrated. eX devices meet the performance goals of gate arrays, and at the same time, present significant improvements in cost and time to market. Using timing-driven place-and-route tools, designers can achieve highly deterministic device performance.

User Security

Microsemi FuseLock advantage provides the highest level of protection in the FPGA industry against unauthorized modifications. In addition to the inherent strengths of the architecture, special security fuses that are intended to prevent internal probing and overwriting are hidden throughout the fabric of the device. They are located such that they cannot be accessed or bypassed without destroying the rest of the device, making Microsemi antifuse FPGAs highly resistant to both invasive and more subtle noninvasive attacks.

Look for this symbol to ensure your valuable IP is secure. The FuseLock Symbol on the FPGA ensures that the device is safeguarded to cryptographic attacks.

Figure 1-7 • **Fuselock**

For more information, refer to *Implementation of Security in Microsemi Antifuse FPGAs* application note.

I/O Modules

Each I/O on an eX device can be configured as an input, an output, a tristate output, or a bidirectional pin. Even without the inclusion of dedicated I/O registers, these I/Os, in combination with array registers, can achieve clock-to-out (pad-to-pad) timing as fast as 3.9 ns. I/O cells in eX devices do not contain embedded latches or flip-flops and can be inferred directly from HDL code. The device can easily interface with any other device in the system, which in turn enables parallel design of system components and reduces overall design time.

All unused I/Os are configured as tristate outputs by Microsemi's Designer software, for maximum flexibility when designing new boards or migrating existing designs. Each I/O module has an available pull-up or pull-down resistor of approximately 50 kΩ that can configure the I/O in a known state during power-up. Just shortly before V_{CCA} reaches 2.5 V, the resistors are disabled and the I/Os will be controlled by user logic.

Table 1-2 describes the I/O features of eX devices. For more information on I/Os, refer to *Microsemi eX, SX-A, and RT54SX-S I/Os* application note.

Table 1-2 • **I/O Features**

Function	Description
Input Buffer Threshold Selection	• 5.0V TTL • 3.3V LVTTL • 2.5V LVCMOS2
Nominal Output Drive	• 5.0V TTL/CMOS • 3.3V LVTTL • 2.5V LVCMOS 2
Output Buffer	"Hot-Swap" Capability • I/O on an unpowered device does not sink current • Can be used for "cold sparing" Selectable on an individual I/O basis Individually selectable low-slew option
Power-Up	Individually selectable pull ups and pull downs during power-up (default is to power up in tristate) Enables deterministic power-up of device V_{CCA} and V_{CCI} can be powered in any order

The eX family supports mixed-voltage operation and is designed to tolerate 5.0 V inputs in each case.

A detailed description of the I/O pins in eX devices can be found in "Pin Description" on page 1-31.

Hot-Swapping

eX I/Os are configured to be hot-swappable. During power-up/down (or partial up/down), all I/Os are tristated, provided V_{CCA} ramps up within a diode drop of V_{CCI}. V_{CCA} and V_{CCI} do not have to be stable. during power-up/down, and they do not require a specific power-up or power-down sequence in order to avoid damage to the eX devices. In addition, all outputs can be programmed to have a weak resistor pull-up or pull-down for output tristate at power-up. After the eX device is plugged into an electrically active system, the device will not degrade the reliability of or cause damage to the host system. The device's output pins are driven to a high impedance state until normal chip operating conditions are reached. Please see the application note, *Microsemi SX-A and RT54SX-S Devices in Hot-Swap and Cold-Sparing Applications*, which also applies to the eX devices, for more information on hot swapping.

Power Requirements

Power consumption is extremely low for the eX family due to the low capacitance of the antifuse interconnects. The antifuse architecture does not require active circuitry to hold a charge (as do SRAM or EPROM), making it the lowest-power FPGA architecture available today.

Low Power Mode

The eX family has been designed with a Low Power Mode. This feature, activated with setting the special LP pin to HIGH for a period longer than 800 ns, is particularly useful for battery-operated systems where battery life is a primary concern. In this mode, the core of the device is turned off and the device consumes minimal power with low standby current. In addition, all input buffers are turned off, and all outputs and bidirectional buffers are tristated when the device enters this mode. Since the core of the device is turned off, the states of the registers are lost. The device must be re-initialized when returning to normal operating mode. I/Os can be driven during LP mode. For details, refer to the *Design for Low Power in Microsemi Antifuse FPGAs* application note under the section Using the LP Mode Pin on eX Devices. Clock pins should be driven either HIGH or LOW and should not float; otherwise, they will draw current and burn power. The device must be re-initialized when exiting LP mode.

Programming

Device programming is supported through Silicon Sculptor series of programmers. In particular, Silicon Sculptor II is a compact, robust, single-site and multi-site device programmer for the PC.

With standalone software, Silicon Sculptor II allows concurrent programming of multiple units from the same PC, ensuring the fastest programming times possible. Each fuse is subsequently verified by Silicon Sculptor II to insure correct programming. In addition, integrity tests ensure that no extra fuses are programmed. Silicon Sculptor II also provides extensive hardware self-testing capability.

The procedure for programming an eX device using Silicon Sculptor II is as follows:

1. Load the *.AFM file
2. Select the device to be programmed
3. Begin programming

When the design is ready to go to production, Microsemi offers device volume-programming services either through distribution partners or via in-house programming from the factory.

For more details on programming eX devices, please refer to the *Programming Antifuse Devices* application note and the *Silicon Sculptor II User's Guide*.

Probing Capabilities

eX devices provide internal probing capability that is accessed with the JTAG pins. The Silicon Explorer II Diagnostic hardware is used to control the TDI, TCK, TMS and TDO pins to select the desired nets for debugging. The user simply assigns the selected internal nets in the Silicon Explorer II software to the PRA/PRB output pins for observation. Probing functionality is activated when the BST pins are in JTAG mode and the TRST pin is driven HIGH or left floating. If the TRST pin is held LOW, the TAP controller will remain in the Test-Logic-Reset state so no probing can be performed. The Silicon Explorer II automatically places the device into JTAG mode, but the user must drive the TRST pin HIGH or allow the internal pull-up resistor to pull TRST HIGH.

When you select the **Reserve Probe Pin** box, as shown in Figure 1-12 on page 1-10, the layout tool reserves the PRA and PRB pins as dedicated outputs for probing. This reserve option is merely a guideline. If the Layout tool requires that the PRA and PRB pins be user I/Os to achieve successful layout, the tool will use these pins for user I/Os. If you assign user I/Os to the PRA and PRB pins and select the **Reserve Probe Pin** option, Designer Layout will override the "Reserve Probe Pin" option and place your user I/Os on those pins.

To allow for probing capabilities, the security fuse must not be programmed. Programming the security fuse will disable the probe circuitry. Table 1-8 on page 1-13 summarizes the possible device configurations for probing once the device leaves the Test-Logic-Reset JTAG state.

Silicon Explorer II Probe

Silicon Explorer II is an integrated hardware and software solution that, in conjunction with Microsemi Designer software tools, allow users to examine any of the internal nets of the device while it is operating in a prototype or a production system. The user can probe into an eX device via the PRA and PRB pins without changing the placement and routing of the design and without using any additional resources. Silicon Explorer II's noninvasive method does not alter timing or loading effects, thus shortening the debug cycle.

Silicon Explorer II does not require re-layout or additional MUXes to bring signals out to an external pin, which is necessary when using programmable logic devices from other suppliers.

Silicon Explorer II samples data at 100 MHz (asynchronous) or 66 MHz (synchronous). Silicon Explorer II attaches to a PC's standard COM port, turning the PC into a fully functional 18-channel logic analyzer. Silicon Explorer II allows designers to complete the design verification process at their desks and reduces verification time from several hours per cycle to a few seconds.

The Silicon Explorer II tool uses the boundary scan ports (TDI, TCK, TMS and TDO) to select the desired nets for verification. The selected internal nets are assigned to the PRA/PRB pins for observation. Figure 1-13 on page 1-13 illustrates the interconnection between Silicon Explorer II and the eX device to perform in-circuit verification.

Design Considerations

The TDI, TCK, TDO, PRA, and PRB pins should not be used as input or bidirectional ports. Since these pins are active during probing, critical signals input through these pins are not available while probing. In addition, the Security Fuse should not be programmed because doing so disables the probe circuitry. It is recommended to use a series 70Ω termination resistor on every probe connector (TDI, TCK, TMS, TDO, PRA, PRB). The 70Ω series termination is used to prevent data transmission corruption during probing and reading back the checksum.

Table 1-8 • **Device Configuration Options for Probe Capability (TRST pin reserved)**

JTAG Mode	TRST[1]	Security Fuse Programmed	PRA, PRB[2]	TDI, TCK, TDO[2]
Dedicated	LOW	No	User I/O[3]	Probing Unavailable
Flexible	LOW	No	User I/O[3]	User I/O[3]
Dedicated	HIGH	No	Probe Circuit Outputs	Probe Circuit Inputs
Flexible	HIGH	No	Probe Circuit Outputs	Probe Circuit Inputs
–	–	Yes	Probe Circuit Secured	Probe Circuit Secured

Notes:

1. *If TRST pin is not reserved, the device behaves according to TRST = HIGH in the table.*
2. *Avoid using the TDI, TCK, TDO, PRA, and PRB pins as input or bidirectional ports. Since these pins are active during probing, input signals will not pass through these pins and may cause contention.*
3. *If no user signal is assigned to these pins, they will behave as unused I/Os in this mode. Unused pins are automatically tristated by Microsemi Designer software.*

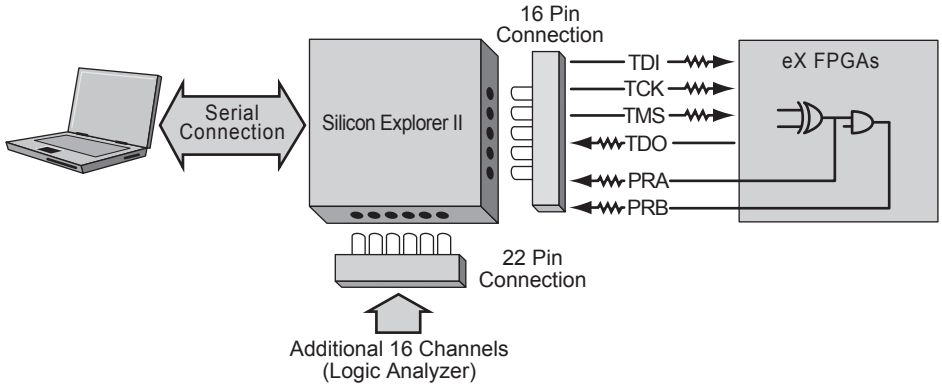


Figure 1-13 • **Silicon Explorer II Probe Setup**

Development Tool Support

The eX family of FPGAs is fully supported by both Libero® Integrated Design Environment and Designer FPGA Development software. Libero IDE is a design management environment that streamlines the design flow. Libero IDE provides an integrated design manager that seamlessly integrates design tools while guiding the user through the design flow, managing all design and log files, and passing necessary design data among tools. Additionally, Libero IDE allows users to integrate both schematic and HDL synthesis into a single flow and verify the entire design in a single environment. Libero IDE includes Synplify® for Microsemi from Synplicity®, ViewDraw for Microsemi from Mentor Graphics, ModelSim® HDL Simulator from Mentor Graphics®, WaveFormer Lite™ from SynaptiCAD™, and Designer software from Microsemi. Refer to the *Libero IDE flow* (located on Microsemi SoC Product Group's website) diagram for more information.

2.5 V / 3.3 V /5.0 V Operating Conditions

Table 1-9 • **Absolute Maximum Ratings***

Symbol	Parameter	Limits	Units
VCCI	DC Supply Voltage for I/Os	–0.3 to +6.0	V
VCCA	DC Supply Voltage for Array	–0.3 to +3.0	V
VI	Input Voltage	–0.5 to +5.75	V
VO	Output Voltage	–0.5 to +V_{CCI}	V
T_{STG}	Storage Temperature	–65 to +150	°C

*Note: *Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Devices should not be operated outside the Recommended Operating Conditions.*

Table 1-10 • **Recommended Operating Conditions**

Parameter	Commercial	Industrial	Units
Temperature Range*	0 to +70	–40 to +85	°C
2.5V Power Supply Range (VCCA, VCCI)	2.3 to 2.7	2.3 to 2.7	V
3.3V Power Supply Range (VCCI)	3.0 to 3.6	3.0 to 3.6	V
5.0V Power Supply Range (VCCI)	4.75 to 5.25	4.75 to 5.25	V

*Note: *Ambient temperature (T_A).*

Table 1-11 • **Typical eX Standby Current at 25°C**

Product	VCCA= 2.5 V VCCI = 2.5 V	VCCA = 2.5 V VCCI = 3.3 V	VCCA = 2.5 V VCCI = 5.0 V
eX64	397 µA	497 µA	700 µA
eX128	696 µA	795 µA	1,000 µA
eX256	698 µA	796 µA	2,000 µA

2.5 V LVCMOS2 Electrical Specifications

Symbol	Parameter		Commercial Min.	Commercial Max.	Industrial Min.	Industrial Max.	Units
VOH	VCCI = MIN, VI = VIH or VIL	(IOH = –100 mA)	2.1		2.1		V
	VCCI = MIN, VI = VIH or VIL	(IOH = –1 mA)	2.0		2.0		V
	VCCI = MIN, VI = VIH or VIL	(IOH = –2 mA)	1.7		1.7		V
VOL	VCCI = MIN, VI = VIH or VIL	(IOL = 100 mA)		0.2		0.2	V
	VCCI = MIN, VI = VIH or VIL	(IOL = 1mA)		0.4		0.4	V
	VCCI = MIN,VI = VIH or VIL	(IOL = 2 mA)		0.7		0.7	V
VIL	Input Low Voltage, VOUT ≤ VOL (max.)		–0.3	0.7	-0.3	0.7	V
VIH	Input High Voltage, VOUT ≥ VOH (min.)		1.7	VCCI + 0.3	1.7	VCCI + 0.3	V
IIL/ IIH	Input Leakage Current, VIN = VCCI or GND		–10	10	–10	10	µA
IOZ	3-State Output Leakage Current, VOUT = VCCI or GND		–10	10	–10	10	µA
t_R, $t_{F1,2}$	Input Transition Time			10		10	ns
C_{IO}	I/O Capacitance			10		10	pF
ICC[3,4]	Standby Current			1.0		3.0	mA
IV Curve	Can be derived from the IBIS model at www.microsemi.com/soc/custsup/models/ibis.html.						

Notes:

1. *t_R is the transition time from 0.7 V to 1.7 V.*
2. *t_F is the transition time from 1.7 V to 0.7 V.*
3. *I_{CC} max Commercial –F = 5.0 mA*
4. *$I_{CC} = I_{CCI} + I_{CCA}$*

The estimation of the dynamic power dissipation is a piece-wise linear summation of the power dissipation of each component.

$$\text{Dynamic power dissipation} = VCCA^2 * [(m_c * C_{eqcm} * fm_C)_{\text{Comb Modules}} + (m_s * C_{eqsm} * fm_S)_{\text{Seq Modules}} + (n * C_{eqi} * fn)_{\text{Input Buffers}} + (0.5 * (q1 * C_{eqcr} * fq1) + (r1 * fq1))_{RCLKA} + (0.5 * (q2 * C_{eqcr} * fq2) + (r2 * fq2))_{RCLKB} + (0.5 * (s1 * C_{eqhv} * fs1)+(C_{eqhf} * fs1))_{HCLK}] + V_{CCI}^2 * [(p * (C_{eqo} + C_L) * fp)_{\text{Output Buffers}}]$$

where:

m_c = Number of combinatorial cells switching at frequency fm, typically 20% of C-cells
m_s = Number of sequential cells switching at frequency fm, typically 20% of R-cells
n = Number of input buffers switching at frequency fn, typically number of inputs / 4
p = Number of output buffers switching at frequency fp, typically number of outputs / 4
q1 = Number of R-cells driven by routed array clock A
q2 = Number of R-cells driven by routed array clock B
r1 = Fixed capacitance due to routed array clock A
r2 = Fixed capacitance due to routed array clock B
s1 = Number of R-cells driven by dedicated array clock
C_{eqcm} = Equivalent capacitance of combinatorial modules
C_{eqsm} = Equivalent capacitance of sequential modules
C_{eqi} = Equivalent capacitance of input buffers
C_{eqcr} = Equivalent capacitance of routed array clocks
C_{eqhv} = Variable capacitance of dedicated array clock
C_{eqhf} = Fixed capacitance of dedicated array clock
C_{eqo} = Equivalent capacitance of output buffers
C_L = Average output loading capacitance, typically 10 pF
fm_c = Average C-cell switching frequency, typically F/10
fm_s = Average R-cell switching frequency, typically F/10
fn = Average input buffer switching frequency, typically F/5
fp = Average output buffer switching frequency, typically F/5
fq1 = Frequency of routed clock A
fq2 = Frequency of routed clock B
fs1 = Frequency of dedicated array clock

The eX, SX-A and RTSX-S Power Calculator can be used to estimate the total power dissipation (static and dynamic) of eX devices: www.microsemi.com/soc/techdocs/calculators.aspx.

Input Buffer Delays

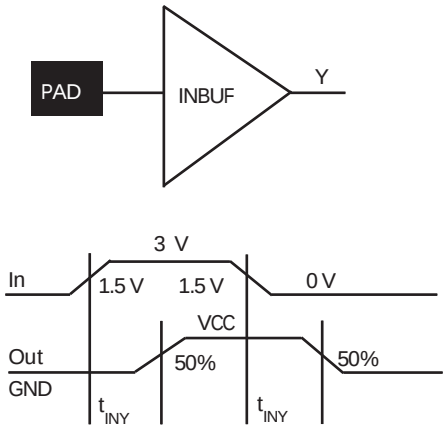


***Table 1-14* • Input Buffer Delays**

C-Cell Delays

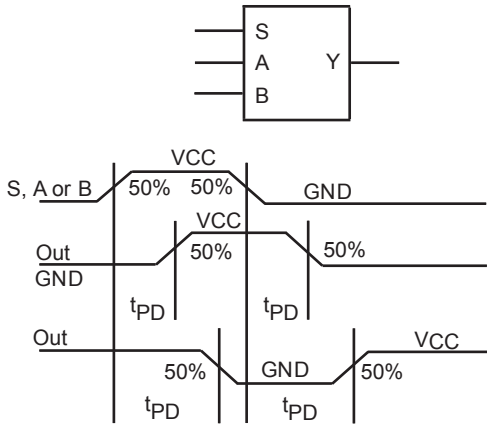


***Table 1-15* • C-Cell Delays**

eX Family Timing Characteristics

***Table 1-17* • eX Family Timing Characteristics**
(Worst-Case Commercial Conditions, VCCA = 2.3 V, T_J = 70°C)

		–P Speed		Std Speed		–F Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
C-Cell Propagation Delays[1]								
t_{PD}	Internal Array Module		0.7		1.0		1.4	ns
Predicted Routing Delays[2]								
t_{DC}	FO=1 Routing Delay, DirectConnect		0.1		0.1		0.2	ns
t_{FC}	FO=1 Routing Delay, FastConnect		0.3		0.5		0.7	ns
t_{RD1}	FO=1 Routing Delay		0.3		0.5		0.7	ns
t_{RD2}	FO=2 Routing Delay		0.4		0.6		0.8	ns
t_{RD3}	FO=3 Routing Delay		0.5		0.8		1.1	ns
t_{RD4}	FO=4 Routing Delay		0.7		1.0		1.3	ns
t_{RD8}	FO=8 Routing Delay		1.2		1.7		2.4	ns
t_{RD12}	FO=12 Routing Delay		1.7		2.5		3.5	ns
R-Cell Timing								
t_{RCO}	Sequential Clock-to-Q		0.6		0.9		1.3	ns
t_{CLR}	Asynchronous Clear-to-Q		0.6		0.8		1.2	ns
t_{PRESET}	Asynchronous Preset-to-Q		0.7		0.9		1.3	ns
t_{SUD}	Flip-Flop Data Input Set-Up	0.5		0.7		1.0		ns
t_{HD}	Flip-Flop Data Input Hold	0.0		0.0		0.0		ns
t_{WASYN}	Asynchronous Pulse Width	1.3		1.9		2.6		ns
$t_{RECASYN}$	Asynchronous Recovery Time	0.3		0.5		0.7		ns
t_{HASYN}	Asynchronous Hold Time	0.3		0.5		0.7		ns
2.5 V Input Module Propagation Delays								
t_{INYH}	Input Data Pad-to-Y HIGH		0.6		0.9		1.3	ns
t_{INYL}	Input Data Pad-to-Y LOW		0.8		1.1		1.5	ns
3.3 V Input Module Propagation Delays								
t_{INYH}	Input Data Pad-to-Y HIGH		0.7		1.0		1.4	ns
t_{INYL}	Input Data Pad-to-Y LOW		0.9		1.3		1.8	ns
5.0 V Input Module Propagation Delays								
t_{INYH}	Input Data Pad-to-Y HIGH		0.7		1.0		1.4	ns
t_{INYL}	Input Data Pad-to-Y LOW		0.9		1.3		1.8	ns
Input Module Predicted Routing Delays[2]								
t_{IRD1}	FO=1 Routing Delay		0.3		0.4		0.5	ns
t_{IRD2}	FO=2 Routing Delay		0.4		0.6		0.8	ns
t_{IRD3}	FO=3 Routing Delay		0.5		0.8		1.1	ns
t_{IRD4}	FO=4 Routing Delay		0.7		1.0		1.3	ns
t_{IRD8}	FO=8 Routing Delay		1.2		1.7		2.4	ns
t_{IRD12}	FO=12 Routing Delay		1.7		2.5		3.5	ns

Notes:

1. *For dual-module macros, use t_{PD} + t_{RD1} + t_{PDn}, t_{RCO} + t_{RD1} + t_{PDn} or t_{PD1} + t_{RD1} + t_{SUD}, whichever is appropriate.*
2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance.*

Table 1-18 • **eX Family Timing Characteristics**
(Worst-Case Commercial Conditions VCCA = 2.3 V, VCCI = 4.75 V, T_J = 70°C)

		–P Speed		Std Speed		–F Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Dedicated (Hard-Wired) Array Clock Networks								
t_{HCKH}	Input LOW to HIGH (Pad to R-Cell Input)		1.1		1.6		2.3	ns
t_{HCKL}	Input HIGH to LOW (Pad to R-Cell Input)		1.1		1.6		2.3	ns
t_{HPWH}	Minimum Pulse Width HIGH	1.4		2.0		2.8		ns
t_{HPWL}	Minimum Pulse Width LOW	1.4		2.0		2.8		ns
t_{HCKSW}	Maximum Skew		<0.1		<0.1		<0.1	ns
t_{HP}	Minimum Period	2.8		4.0		5.6		ns
f_{HMAX}	Maximum Frequency		357		250		178	MHz
Routed Array Clock Networks								
t_{RCKH}	Input LOW to HIGH (Light Load) (Pad to R-Cell Input) MAX.		1.1		1.6		2.2	ns
t_{RCKL}	Input HIGH to LOW (Light Load) (Pad to R-Cell Input) MAX.		1.0		1.4		2.0	ns
t_{RCKH}	Input LOW to HIGH (50% Load) (Pad to R-Cell Input) MAX.		1.2		1.7		2.4	ns
t_{RCKL}	Input HIGH to LOW (50% Load) (Pad to R-Cell Input) MAX.		1.2		1.7		2.4	ns
t_{RCKH}	Input LOW to HIGH (100% Load) (Pad to R-Cell Input) MAX.		1.3		1.9		2.6	ns
t_{RCKL}	Input HIGH to LOW (100% Load) (Pad to R-Cell Input) MAX.		1.3		1.9		2.6	ns
t_{RPWH}	Min. Pulse Width HIGH	1.5		2.1		3.0		ns
t_{RPWL}	Min. Pulse Width LOW	1.5		2.1		3.0		ns
t_{RCKSW}*	Maximum Skew (Light Load)		0.2		0.3		0.4	ns
t_{RCKSW}*	Maximum Skew (50% Load)		0.1		0.2		0.3	ns
t_{RCKSW}*	Maximum Skew (100% Load)		0.1		0.1		0.2	ns

*Note: *Clock skew improves as the clock network becomes more heavily loaded.*

Table 1-19 • eX Family Timing Characteristics
(Worst-Case Commercial Conditions VCCA = 2.3V, VCCI = 2.3 V or 3.0V, T_J = 70°C)

		'–P' Speed		'Std' Speed		'–F' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Dedicated (Hard-Wired) Array Clock Networks								
t_{HCKH}	Input LOW to HIGH (Pad to R-Cell Input)		1.1		1.6		2.3	ns
t_{HCKL}	Input HIGH to LOW (Pad to R-Cell Input)		1.1		1.6		2.3	ns
t_{HPWH}	Minimum Pulse Width HIGH	1.4		2.0		2.8		ns
t_{HPWL}	Minimum Pulse Width LOW	1.4		2.0		2.8		ns
t_{HCKSW}	Maximum Skew		<0.1		<0.1		<0.1	ns
t_{HP}	Minimum Period	2.8		4.0		5.6		ns
f_{HMAX}	Maximum Frequency		357		250		178	MHz
Routed Array Clock Networks								
t_{RCKH}	Input LOW to HIGH (Light Load) (Pad to R-Cell Input) MAX.		1.0		1.4		2.0	ns
t_{RCKL}	Input HIGH to LOW (Light Load) (Pad to R-Cell Input) MAX.		1.0		1.4		2.0	ns
t_{RCKH}	Input LOW to HIGH (50% Load) (Pad to R-Cell Input) MAX.		1.2		1.7		2.4	ns
t_{RCKL}	Input HIGH to LOW (50% Load) (Pad to R-Cell Input) MAX.		1.2		1.7		2.4	ns
t_{RCKH}	Input LOW to HIGH (100% Load) (Pad to R-Cell Input) MAX.		1.4		2.0		2.8	ns
t_{RCKL}	Input HIGH to LOW (100% Load) (Pad to R-Cell Input) MAX.		1.4		2.0		2.8	ns
t_{RPWH}	Min. Pulse Width HIGH	1.4		2.0		2.8		ns
t_{RPWL}	Min. Pulse Width LOW	1.4		2.0		2.8		ns
t_{RCKSW}*	Maximum Skew (Light Load)		0.2		0.3		0.4	ns
t_{RCKSW}*	Maximum Skew (50% Load)		0.2		0.2		0.3	ns
t_{RCKSW}*	Maximum Skew (100% Load)		0.1		0.1		0.2	ns

*Note: *Clock skew improves as the clock network becomes more heavily loaded.*

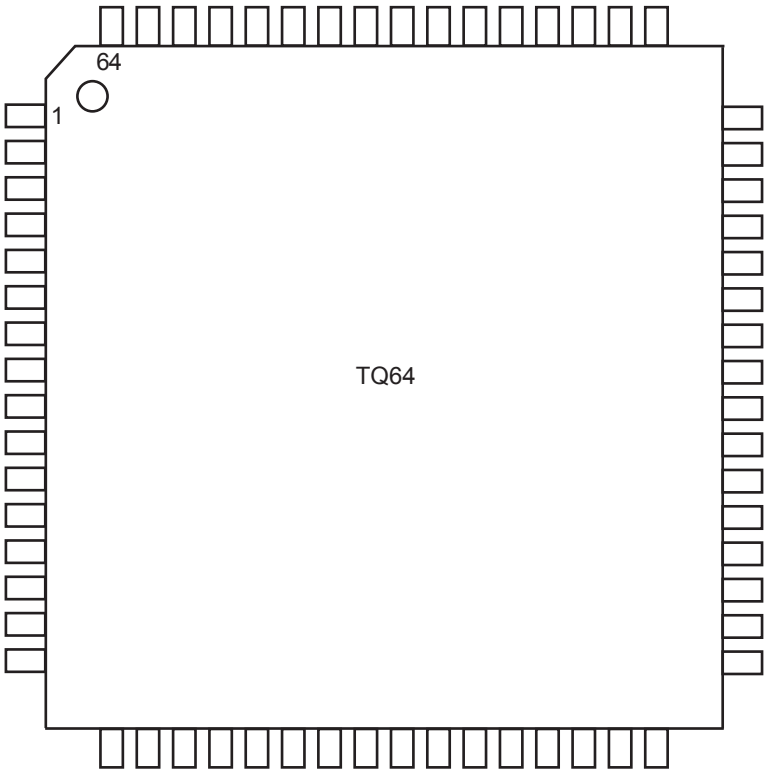
Table 1-20 • **eX Family Timing Characteristics**
(Worst-Case Commercial Conditions VCCA = 2.3 V, T_J = 70°C)

		–P Speed		Std Speed		–F Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
2.5 V LVCMOS Output Module Timing[1] (VCCI = 2.3 V)								
t_{DLH}	Data-to-Pad LOW to HIGH		3.3		4.7		6.6	ns
t_{DHL}	Data-to-Pad HIGH to LOW		3.5		5.0		7.0	ns
t_{DHLS}	Data-to-Pad HIGH to LOW—Low Slew		11.6		16.6		23.2	ns
t_{ENZL}	Enable-to-Pad, Z to L		2.5		3.6		5.1	ns
t_{ENZLS}	Enable-to-Pad Z to L—Low Slew		11.8		16.9		23.7	ns
t_{ENZH}	Enable-to-Pad, Z to H		3.4		4.9		6.9	ns
t_{ENLZ}	Enable-to-Pad, L to Z		2.1		3.0		4.2	ns
t_{ENHZ}	Enable-to-Pad, H to Z		2.4		5.67		7.94	ns
d_{TLH}	Delta Delay vs. Load LOW to HIGH		0.034		0.046		0.066	ns/pF
d_{THL}	Delta Delay vs. Load HIGH to LOW		0.016		0.022		0.05	ns/pF
d_{THLS}	Delta Delay vs. Load HIGH to LOW—Low Slew		0.05		0.072		0.1	ns/pF
3.3 V LVTTL Output Module Timing[1] (VCCI = 3.0 V)								
t_{DLH}	Data-to-Pad LOW to HIGH		2.8		4.0		5.6	ns
t_{DHL}	Data-to-Pad HIGH to LOW		2.7		3.9		5.4	ns
t_{DHLS}	Data-to-Pad HIGH to LOW—Low Slew		9.7		13.9		19.5	ns
t_{ENZL}	Enable-to-Pad, Z to L		2.2		3.2		4.4	ns
t_{ENZLS}	Enable-to-Pad Z to L—Low Slew		9.7		13.9		19.6	ns
t_{ENZH}	Enable-to-Pad, Z to H		2.8		4.0		5.6	ns
t_{ENLZ}	Enable-to-Pad, L to Z		2.8		4.0		5.6	ns
t_{ENHZ}	Enable-to-Pad, H to Z		2.6		3.8		5.3	ns
d_{TLH}	Delta Delay vs. Load LOW to HIGH		0.02		0.03		0.046	ns/pF
d_{THL}	Delta Delay vs. Load HIGH to LOW		0.016		0.022		0.05	ns/pF
d_{THLS}	Delta Delay vs. Load HIGH to LOW—Low Slew		0.05		0.072		0.1	ns/pF
5.0 V TTL Output Module Timing* (VCCI = 4.75 V)								
t_{DLH}	Data-to-Pad LOW to HIGH		2.0		2.9		4.0	ns
t_{DHL}	Data-to-Pad HIGH to LOW		2.6		3.7		5.2	ns
t_{DHLS}	Data-to-Pad HIGH to LOW—Low Slew		6.8		9.7		13.6	ns
t_{ENZL}	Enable-to-Pad, Z to L		1.9		2.7		3.8	ns
t_{ENZLS}	Enable-to-Pad Z to L—Low Slew		6.8		9.8		13.7	ns
t_{ENZH}	Enable-to-Pad, Z to H		2.1		3.0		4.1	ns
t_{ENLZ}	Enable-to-Pad, L to Z		3.3		4.8		6.6	ns

*Note: *Delays based on 35 pF loading.*

2 – Package Pin Assignments

TQ64



Note: For Package Manufacturing and Environmental information, visit Resource center at www.microsemi.com/soc/products/rescenter/package/index.html.

TQ64		
Pin Number	eX64 Function	eX128 Function
1	GND	GND
2	TDI, I/O	TDI, I/O
3	I/O	I/O
4	TMS	TMS
5	GND	GND
6	VCCI	VCCI
7	I/O	I/O
8	I/O	I/O
9	NC	I/O
10	NC	I/O
11	TRST, I/O	TRST, I/O
12	I/O	I/O
13	NC	I/O
14	GND	GND
15	I/O	I/O
16	I/O	I/O
17	I/O	I/O
18	I/O	I/O
19	VCCI	VCCI
20	I/O	I/O
21	PRB, I/O	PRB, I/O
22	VCCA	VCCA
23	GND	GND
24	I/O	I/O
25	HCLK	HCLK
26	I/O	I/O
27	I/O	I/O
28	I/O	I/O
29	I/O	I/O
30	I/O	I/O
31	I/O	I/O
32	TDO, I/O	TDO, I/O

TQ64		
Pin Number	eX64 Function	eX128 Function
33	GND	GND
34	I/O	I/O
35	I/O	I/O
36	VCCA	VCCA
37	VCCI	VCCI
38	I/O	I/O
39	I/O	I/O
40	NC	I/O
41	NC	I/O
42	I/O	I/O
43	I/O	I/O
44	VCCA	VCCA
45*	GND/LP	GND/ LP
46	GND	GND
47	I/O	I/O
48	I/O	I/O
49	I/O	I/O
50	I/O	I/O
51	I/O	I/O
52	VCCI	VCCI
53	I/O	I/O
54	I/O	I/O
55	CLKA	CLKA
56	CLKB	CLKB
57	VCCA	VCCA
58	GND	GND
59	PRA, I/O	PRA, I/O
60	I/O	I/O
61	VCCI	VCCI
62	I/O	I/O
63	I/O	I/O
64	TCK, I/O	TCK, I/O

*Note: *Please read the LP pin descriptions for restrictions on their use.*

TQ100			
Pin Number	eX64 Function	eX128 Function	eX256 Function
1	GND	GND	GND
2	TDI, I/O	TDI, I/O	TDI, I/O
3	NC	NC	I/O
4	NC	NC	I/O
5	NC	NC	I/O
6	I/O	I/O	I/O
7	TMS	TMS	TMS
8	VCCI	VCCI	VCCI
9	GND	GND	GND
10	NC	I/O	I/O
11	NC	I/O	I/O
12	I/O	I/O	I/O
13	NC	I/O	I/O
14	I/O	I/O	I/O
15	NC	I/O	I/O
16	TRST, I/O	TRST, I/O	TRST, I/O
17	NC	I/O	I/O
18	I/O	I/O	I/O
19	NC	I/O	I/O
20	VCCI	VCCI	VCCI
21	I/O	I/O	I/O
22	NC	I/O	I/O
23	NC	NC	I/O
24	NC	NC	I/O
25	I/O	I/O	I/O
26	I/O	I/O	I/O
27	I/O	I/O	I/O
28	I/O	I/O	I/O
29	I/O	I/O	I/O
30	I/O	I/O	I/O
31	I/O	I/O	I/O
32	I/O	I/O	I/O
33	I/O	I/O	I/O
34	PRB, I/O	PRB, I/O	PRB, I/O
35	VCCA	VCCA	VCCA

TQ100			
Pin Number	eX64 Function	eX128 Function	eX256 Function
36	GND	GND	GND
37	NC	NC	NC
38	I/O	I/O	I/O
39	HCLK	HCLK	HCLK
40	I/O	I/O	I/O
41	I/O	I/O	I/O
42	I/O	I/O	I/O
43	I/O	I/O	I/O
44	VCCI	VCCI	VCCI
45	I/O	I/O	I/O
46	I/O	I/O	I/O
47	I/O	I/O	I/O
48	I/O	I/O	I/O
49	TDO, I/O	TDO, I/O	TDO, I/O
50	NC	I/O	I/O
51	GND	GND	GND
52	NC	NC	I/O
53	NC	NC	I/O
54	NC	NC	I/O
55	I/O	I/O	I/O
56	I/O	I/O	I/O
57	VCCA	VCCA	VCCA
58	VCCI	VCCI	VCCI
59	NC	I/O	I/O
60	I/O	I/O	I/O
61	NC	I/O	I/O
62	I/O	I/O	I/O
63	NC	I/O	I/O
64	I/O	I/O	I/O
65	NC	I/O	I/O
66	I/O	I/O	I/O
67	VCCA	VCCA	VCCA
68	GND/LP	GND/LP	GND/LP
69	GND	GND	GND
70	I/O	I/O	I/O

*Note: *Please read the LP pin descriptions for restrictions on their use.*

TQ100			
Pin Number	**eX64 Function**	**eX128 Function**	**eX256 Function**
71	I/O	I/O	I/O
72	NC	I/O	I/O
73	NC	NC	I/O
74	NC	NC	I/O
75	NC	NC	I/O
76	NC	I/O	I/O
77	I/O	I/O	I/O
78	I/O	I/O	I/O
79	I/O	I/O	I/O
80	I/O	I/O	I/O
81	I/O	I/O	I/O
82	VCCI	VCCI	VCCI
83	I/O	I/O	I/O
84	I/O	I/O	I/O
85	I/O	I/O	I/O
86	I/O	I/O	I/O
87	CLKA	CLKA	CLKA
88	CLKB	CLKB	CLKB
89	NC	NC	NC
90	VCCA	VCCA	VCCA
91	GND	GND	GND
92	PRA, I/O	PRA, I/O	PRA, I/O
93	I/O	I/O	I/O
94	I/O	I/O	I/O
95	I/O	I/O	I/O
96	I/O	I/O	I/O
97	I/O	I/O	I/O
98	I/O	I/O	I/O
99	I/O	I/O	I/O
100	TCK, I/O	TCK, I/O	TCK, I/O

*Note: *Please read the LP pin descriptions for restrictions on their use.*

Revision	Changes	Page
Advance v0.4	In the Product Profile, the Maximum User I/Os for eX64 was changed to 84.	1-I
	In the Product Profile table, the Maximum User I/Os for eX128 was changed to 100.	1-I
Advance v0.3	The Mechanical Drawings section has been removed from the data sheet. The mechanical drawings are now contained in a separate document, “Package Characteristics and Mechanical Drawings,” available on the Actel web site.	
	A new section describing "Clock Resources"has been added.	1-3
	A new table describing "I/O Features"has been added.	1-6
	The "Pin Description"section has been updated and clarified.	1-31
	The original Electrical Specifications table was separated into two tables (2.5V and 3.3/5.0V). In both tables, several different currents are specified for V_{OH} and V_{OL}.	Page 8 and 9
	A new table listing 2.5V low power specifications and associated power graphs were added.	page 9
	Pin functions for eX256 TQ100 have been added to the "TQ100"table.	2-3
	A CS49 pin drawing and pin assignment table including eX64 and eX128 pin functions have been added.	page 26
	A CS128 pin drawing and pin assignment table including eX64, eX128, and eX256 pin functions have been added.	pages 26-27
	A CS180 pin drawing and pin assignment table for eX256 pin functions have been added.	pages 27, 31
Advance v0.2	The following table note was added to the eX Timing Characteristics table for clarification: Clock skew improves as the clock network becomes more heavily loaded.	pages 14-15