**Welcome to E-XFL.COM**

**Understanding Embedded - FPGAs (Field Programmable Gate Array)**

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.
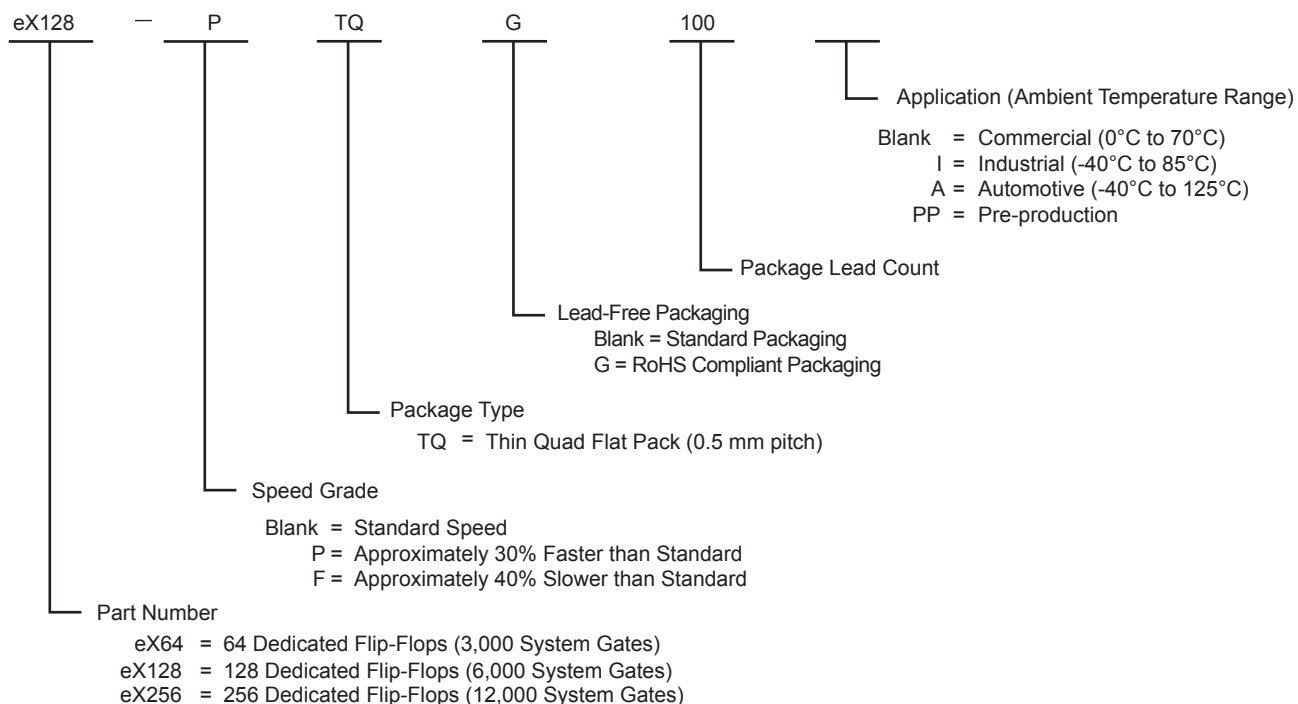
**Applications of Embedded - FPGAs**

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

## Details

| | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | - |
| Number of Logic Elements/Cells | 128 |
| Total RAM Bits | - |
| Number of I/O | 56 |
| Number of Gates | 3000 |
| Voltage - Supply | 2.3V ~ 2.7V |
| Mounting Type | Surface Mount |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Package / Case | 100-LQFP |
| Supplier Device Package | 100-TQFP (14x14) |
| Purchase URL | https://www.e-xfl.com/product-detail/microsemi/ex64-tq100i |

# Ordering Information



```
eX128   —   P      TQ      G      100
```

Application (Ambient Temperature Range)

Blank = Commercial (0°C to 70°C)
I = Industrial (-40°C to 85°C)
A = Automotive (-40°C to 125°C)
PP = Pre-production

Package Lead Count

Lead-Free Packaging
Blank = Standard Packaging
G = RoHS Compliant Packaging

Package Type
TQ = Thin Quad Flat Pack (0.5 mm pitch)

Speed Grade
Blank = Standard Speed
P = Approximately 30% Faster than Standard
F = Approximately 40% Slower than Standard

Part Number
eX64 = 64 Dedicated Flip-Flops (3,000 System Gates)
eX128 = 128 Dedicated Flip-Flops (6,000 System Gates)
eX256 = 256 Dedicated Flip-Flops (12,000 System Gates)

# eX Device Status

| eX Devices | Status |
|---|---|
| eX64 | Production |
| eX128 | Production |
| eX256 | Production |

# Plastic Device Resources

| Device | User I/Os (Including Clock Buffers) | |
|---|---|---|
| | TQ64 | TQ100 |
| eX64 | 41 | 56 |
| eX128 | 46 | 70 |
| eX256 | — | 81 |

Note: TQ = Thin Quad Flat Pack

# Temperature Grade Offerings

| Device\ Package | TQ64 | TQ100 |
|---|---|---|
| eX64 | C, I, A | C, I, A |
| eX128 | C, I, A | C, I, A |
| eX256 | C, I, A | C, I, A |

*Note:* *C = Commercial*

*I = Industrial*

*A = Automotive*

# Speed Grade and Temperature Grade Matrix

| | –F | Std | –P |
|---|---|---|---|
| C | ✓ | ✓ | ✓ |
| I | | ✓ | ✓ |
| A | | ✓ | |

*Note:* *P = Approximately 30% faster than Standard*

*–F = Approximately 40% slower than Standard*

*Refer to the* eX Automotive Family FPGAs *datasheet for details on automotive temperature offerings.*

Contact your local Microsemi representative for device availability.

# Table of Contents

Figure 1-8 to Figure 1-11 on page 1-9 show some sample power characteristics of eX devices.
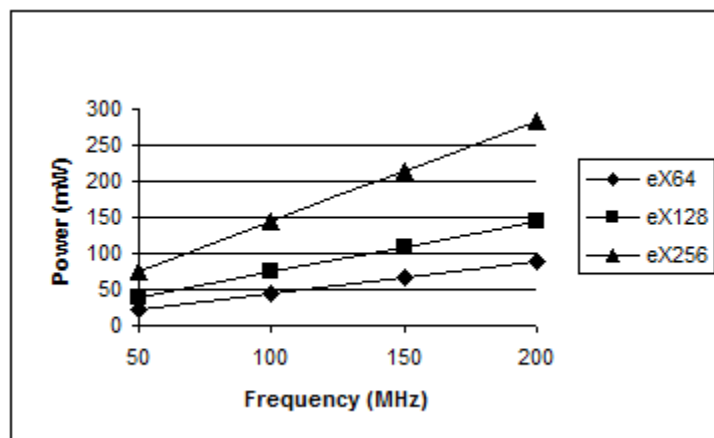


Notes:
1. Device filled with 16-bit counters.
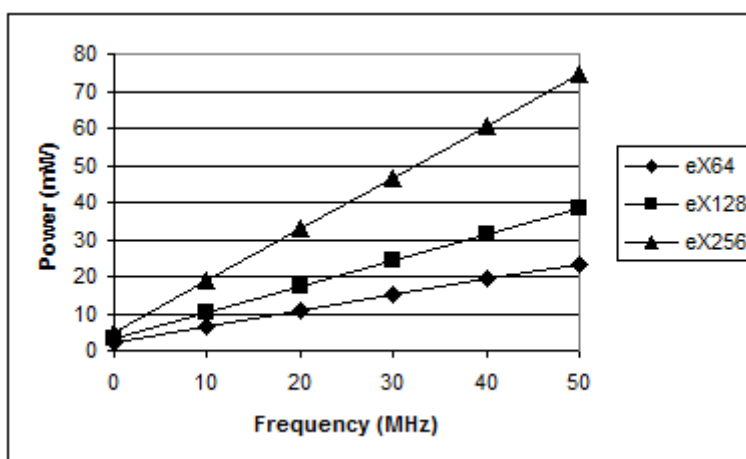2. VCCA, VCCI = 2.7 V, device tested at room temperature.

*Figure 1-8 •   eX Dynamic Power Consumption – High Frequency*



Notes:
1. Device filled with 16-bit counters.
2. VCCA, VCCI = 2.7 V, device tested at room temperature.

*Figure 1-9 •   eX Dynamic Power Consumption – Low Frequency*

## Programming

Device programming is supported through Silicon Sculptor series of programmers. In particular, Silicon Sculptor II is a compact, robust, single-site and multi-site device programmer for the PC.

With standalone software, Silicon Sculptor II allows concurrent programming of multiple units from the same PC, ensuring the fastest programming times possible. Each fuse is subsequently verified by Silicon Sculptor II to insure correct programming. In addition, integrity tests ensure that no extra fuses are programmed. Silicon Sculptor II also provides extensive hardware self-testing capability.

The procedure for programming an eX device using Silicon Sculptor II is as follows:

1. Load the *.AFM file
2. Select the device to be programmed
3. Begin programming

When the design is ready to go to production, Microsemi offers device volume-programming services either through distribution partners or via in-house programming from the factory.

For more details on programming eX devices, please refer to the *Programming Antifuse Devices* application note and the *Silicon Sculptor II User's Guide*.

## Probing Capabilities

eX devices provide internal probing capability that is accessed with the JTAG pins. The Silicon Explorer II Diagnostic hardware is used to control the TDI, TCK, TMS and TDO pins to select the desired nets for debugging. The user simply assigns the selected internal nets in the Silicon Explorer II software to the PRA/PRB output pins for observation. Probing functionality is activated when the BST pins are in JTAG mode and the TRST pin is driven HIGH or left floating. If the TRST pin is held LOW, the TAP controller will remain in the Test-Logic-Reset state so no probing can be performed. The Silicon Explorer II automatically places the device into JTAG mode, but the user must drive the TRST pin HIGH or allow the internal pull-up resistor to pull TRST HIGH.

When you select the **Reserve Probe Pin** box, as shown in Figure 1-12 on page 1-10, the layout tool reserves the PRA and PRB pins as dedicated outputs for probing. This reserve option is merely a guideline. If the Layout tool requires that the PRA and PRB pins be user I/Os to achieve successful layout, the tool will use these pins for user I/Os. If you assign user I/Os to the PRA and PRB pins and select the **Reserve Probe Pin** option, Designer Layout will override the "Reserve Probe Pin" option and place your user I/Os on those pins.

To allow for probing capabilities, the security fuse must not be programmed. Programming the security fuse will disable the probe circuitry. Table 1-8 on page 1-13 summarizes the possible device configurations for probing once the device leaves the Test-Logic-Reset JTAG state.

## Silicon Explorer II Probe

Silicon Explorer II is an integrated hardware and software solution that, in conjunction with Microsemi Designer software tools, allow users to examine any of the internal nets of the device while it is operating in a prototype or a production system. The user can probe into an eX device via the PRA and PRB pins without changing the placement and routing of the design and without using any additional resources. Silicon Explorer II's noninvasive method does not alter timing or loading effects, thus shortening the debug cycle.

Silicon Explorer II does not require re-layout or additional MUXes to bring signals out to an external pin, which is necessary when using programmable logic devices from other suppliers.

Silicon Explorer II samples data at 100 MHz (asynchronous) or 66 MHz (synchronous). Silicon Explorer II attaches to a PC's standard COM port, turning the PC into a fully functional 18-channel logic analyzer. Silicon Explorer II allows designers to complete the design verification process at their desks and reduces verification time from several hours per cycle to a few seconds.

The Silicon Explorer II tool uses the boundary scan ports (TDI, TCK, TMS and TDO) to select the desired nets for verification. The selected internal nets are assigned to the PRA/PRB pins for observation. Figure 1-13 on page 1-13 illustrates the interconnection between Silicon Explorer II and the eX device to perform in-circuit verification.

# Design Considerations

The TDI, TCK, TDO, PRA, and PRB pins should not be used as input or bidirectional ports. Since these pins are active during probing, critical signals input through these pins are not available while probing. In addition, the Security Fuse should not be programmed because doing so disables the probe circuitry. It is recommended to use a series 70Ω termination resistor on every probe connector (TDI, TCK, TMS, TDO, PRA, PRB). The 70Ω series termination is used to prevent data transmission corruption during probing and reading back the checksum.

*Table 1-8 •* **Device Configuration Options for Probe Capability (TRST pin reserved)**

| JTAG Mode | TRST[1] | Security Fuse Programmed | PRA, PRB[2] | TDI, TCK, TDO[2] |
|---|---|---|---|---|
| Dedicated | LOW | No | User I/O[3] | Probing Unavailable |
| Flexible | LOW | No | User I/O[3] | User I/O[3] |
| Dedicated | HIGH | No | Probe Circuit Outputs | Probe Circuit Inputs |
| Flexible | HIGH | No | Probe Circuit Outputs | Probe Circuit Inputs |
| – | – | Yes | Probe Circuit Secured | Probe Circuit Secured |

*Notes:*

1. *If TRST pin is not reserved, the device behaves according to TRST = HIGH in the table.*
2. *Avoid using the TDI, TCK, TDO, PRA, and PRB pins as input or bidirectional ports. Since these pins are active during probing, input signals will not pass through these pins and may cause contention.*
3. *If no user signal is assigned to these pins, they will behave as unused I/Os in this mode. Unused pins are automatically tristated by Microsemi Designer software.*
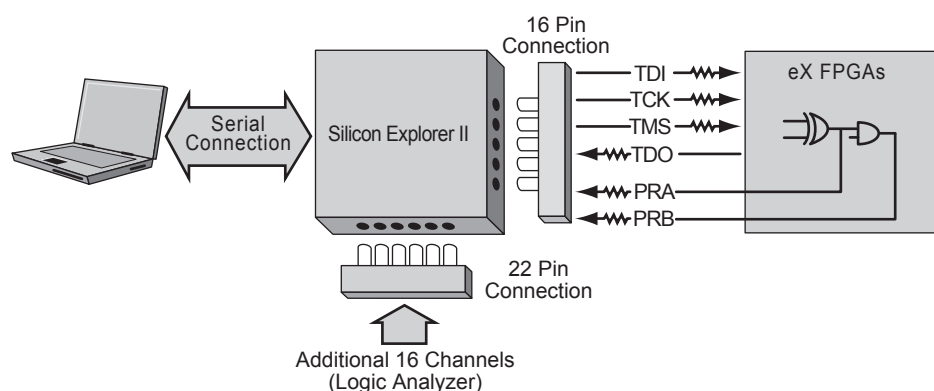


*Figure 1-13 •* **Silicon Explorer II Probe Setup**

## Development Tool Support

The eX family of FPGAs is fully supported by both Libero® Integrated Design Environment and Designer FPGA Development software. Libero IDE is a design management environment that streamlines the design flow. Libero IDE provides an integrated design manager that seamlessly integrates design tools while guiding the user through the design flow, managing all design and log files, and passing necessary design data among tools. Additionally, Libero IDE allows users to integrate both schematic and HDL synthesis into a single flow and verify the entire design in a single environment. Libero IDE includes Synplify® for Microsemi from Synplicity®, ViewDraw for Microsemi from Mentor Graphics, ModelSim® HDL Simulator from Mentor Graphics®, WaveFormer Lite™ from SynaptiCAD™, and Designer software from Microsemi. Refer to the *Libero IDE flow* (located on Microsemi SoC Product Group's website) diagram for more information.

# Related Documents

## Datasheet

*eX Automotive Family FPGAs*

www.microsemi.com/soc/documents/eX_Auto_DS.pdf

## Application Notes

*Maximizing Logic Utilization in eX, SX and SX-A FPGA Devices Using CC Macros*

www.microsemi.com/soc/documents/CC_Macro_AN.pdf

*Implementation of Security in Microsemi Antifuse FPGAs*

www.microsemi.com/soc/documents/Antifuse_Security_AN.pdf

*Microsemi eX, SX-A, and RT54SX-S I/Os*

www.microsemi.com/soc/documents/antifuseIO_AN.pdf

*Microsemi SX-A and RT54SX-S Devices in Hot-Swap and Cold-Sparing Applications*

www.microsemi.com/soc/documents/HotSwapColdSparing_AN.pdf

*Design For Low Power in Microsemi Antifuse FPGAs*

www.microsemi.com/soc/documents/Low_Power_AN.pdf

*Programming Antifuse Devices*

www.microsemi.com/soc/documents/AntifuseProgram_AN.pdf

## User Guides

*Silicon Sculptor II User's Guide*

www.microsemi.com/soc/documents/SiliSculptII_Sculpt3_ug.pdf

## Miscellaneous

*Libero IDE flow*

www.microsemi.com/soc/products/tools/libero/flow.html

# 2.5 V / 3.3 V /5.0 V Operating Conditions

*Table 1-9 •* **Absolute Maximum Ratings\***

| Symbol | Parameter | Limits | Units |
|---|---|---|---|
| VCCI | DC Supply Voltage for I/Os | –0.3 to +6.0 | V |
| VCCA | DC Supply Voltage for Array | –0.3 to +3.0 | V |
| VI | Input Voltage | –0.5 to +5.75 | V |
| VO | Output Voltage | –0.5 to +$V_{CCI}$ | V |
| $T_{STG}$ | Storage Temperature | –65 to +150 | °C |

Note: *\*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Devices should not be operated outside the Recommended Operating Conditions.*

*Table 1-10 •* **Recommended Operating Conditions**

| Parameter | Commercial | Industrial | Units |
|---|---|---|---|
| Temperature Range\* | 0 to +70 | –40 to +85 | °C |
| 2.5V Power Supply Range (VCCA, VCCI) | 2.3 to 2.7 | 2.3 to 2.7 | V |
| 3.3V Power Supply Range (VCCI) | 3.0 to 3.6 | 3.0 to 3.6 | V |
| 5.0V Power Supply Range (VCCI) | 4.75 to 5.25 | 4.75 to 5.25 | V |

Note: *\*Ambient temperature ($T_A$).*

*Table 1-11 •* **Typical eX Standby Current at 25°C**

| Product | VCCA= 2.5 V VCCI = 2.5 V | VCCA = 2.5 V VCCI = 3.3 V | VCCA = 2.5 V VCCI = 5.0 V |
|---|---|---|---|
| eX64 | 397 µA | 497 µA | 700 µA |
| eX128 | 696 µA | 795 µA | 1,000 µA |
| eX256 | 698 µA | 796 µA | 2,000 µA |

# 2.5 V LVCMOS2 Electrical Specifications

| Symbol | Parameter | | Commercial Min. | Max. | Industrial Min. | Max. | Units |
|---|---|---|---|---|---|---|---|
| VOH | VCCI = MIN, VI = VIH or VIL | (IOH = –100 mA) | 2.1 | | 2.1 | | V |
| | VCCI = MIN, VI = VIH or VIL | (IOH = –1 mA) | 2.0 | | 2.0 | | V |
| | VCCI = MIN, VI = VIH or VIL | (IOH = –2 mA) | 1.7 | | 1.7 | | V |
| VOL | VCCI = MIN, VI = VIH or VIL | (IOL = 100 mA) | | 0.2 | | 0.2 | V |
| | VCCI = MIN, VI = VIH or VIL | (IOL = 1mA) | | 0.4 | | 0.4 | V |
| | VCCI = MIN,VI = VIH or VIL | (IOL = 2 mA) | | 0.7 | | 0.7 | V |
| VIL | Input Low Voltage, VOUT ≤ VOL (max.) | | –0.3 | 0.7 | -0.3 | 0.7 | V |
| VIH | Input High Voltage, VOUT ≥ VOH (min.) | | 1.7 | VCCI + 0.3 | 1.7 | VCCI + 0.3 | V |
| IIL/ IIH | Input Leakage Current, VIN = VCCI or GND | | –10 | 10 | –10 | 10 | µA |
| IOZ | 3-State Output Leakage Current, VOUT = VCCI or GND | | –10 | 10 | –10 | 10 | µA |
| $t_R$, $t_{F1,2}$ | Input Transition Time | | | 10 | | 10 | ns |
| $C_{IO}$ | I/O Capacitance | | | 10 | | 10 | pF |
| ICC[3,4] | Standby Current | | | 1.0 | | 3.0 | mA |
| IV Curve | Can be derived from the IBIS model at www.microsemi.com/soc/custsup/models/ibis.html. | | | | | | |

Notes:

1. $t_R$ is the transition time from 0.7 V to 1.7 V.
2. $t_F$ is the transition time from 1.7 V to 0.7 V.
3. $I_{CC}$ max Commercial –F = 5.0 mA
4. $I_{CC} = I_{CCI} + I_{CCA}$

The estimation of the dynamic power dissipation is a piece-wise linear summation of the power dissipation of each component.

$$\text{Dynamic power dissipation} = V_{CCA}^2 * [(m_c * C_{eqcm} * fm_C)_{\text{Comb Modules}} + (m_s * C_{eqsm} * fm_S)_{\text{Seq Modules}}$$

$$+ (n * C_{eqi} * fn)_{\text{Input Buffers}} + (0.5 * (q1 * C_{eqcr} * fq1) + (r1 * fq1))_{\text{RCLKA}} + (0.5 * (q2 * C_{eqcr} * fq2)$$

$$+ (r2 * fq2))_{\text{RCLKB}} + (0.5 * (s1 * C_{eqhv} * fs1) + (C_{eqhf} * fs1))_{\text{HCLK}}] + V_{CCI}^2 * [(p * (C_{eqo} + C_L)$$

$$* fp)_{\text{Output Buffers}}]$$

where:

$m_c$     =  Number of combinatorial cells switching at frequency fm, typically 20% of C-cells

$m_s$     =  Number of sequential cells switching at frequency fm, typically 20% of R-cells

n     =  Number of input buffers switching at frequency fn, typically number of inputs / 4

p     =  Number of output buffers switching at frequency fp, typically number of outputs / 4

q1     =  Number of R-cells driven by routed array clock A

q2     =   Number of R-cells driven by routed array clock B

r1     =   Fixed capacitance due to routed array clock A

r2     =   Fixed capacitance due to routed array clock B

s1     =   Number of R-cells driven by dedicated array clock

$C_{eqcm}$  =  Equivalent capacitance of combinatorial modules

$C_{eqsm}$  =  Equivalent capacitance of sequential modules

$C_{eqi}$   =  Equivalent capacitance of input buffers

$C_{eqcr}$  =  Equivalent capacitance of routed array clocks

$C_{eqhv}$  =  Variable capacitance of dedicated array clock

$C_{eqhf}$  =  Fixed capacitance of dedicated array clock

$C_{eqo}$   =  Equivalent capacitance of output buffers

$C_L$     =  Average output loading capacitance, typically 10 pF

$fm_c$    =  Average C-cell switching frequency, typically F/10

$fm_s$    =  Average R-cell switching frequency, typically F/10

fn     =   Average input buffer switching frequency, typically F/5

fp     =  Average output buffer switching frequency, typically F/5

fq1     =   Frequency of routed clock A

fq2     =  Frequency of routed clock B

fs1     =   Frequency of dedicated array clock

The eX, SX-A and RTSX-S Power Calculator can be used to estimate the total power dissipation (static and dynamic) of eX devices: www.microsemi.com/soc/techdocs/calculators.aspx.

# Thermal Characteristics

The temperature variable in the Designer software refers to the junction temperature, not the ambient temperature. This is an important distinction because the heat generated from dynamic power consumption is usually hotter than the ambient temperature. EQ 1, shown below, can be used to calculate junction temperature.

*EQ 1*

Junction Temperature = $\Delta T + T_a(1)$

Where:

$T_a$ = Ambient Temperature

$\Delta T$ = Temperature gradient between junction (silicon) and ambient = $\theta_{ja} * P$

P = Power

$\theta_{ja}$ = Junction to ambient of package. $\theta_{ja}$ numbers are located in the "Package Thermal Characteristics" section below.

# Package Thermal Characteristics

The device junction-to-case thermal characteristic is $\theta_{jc}$, and the junction-to-ambient air characteristic is $\theta_{ja}$. The thermal characteristics for $\theta_{ja}$ are shown with two different air flow rates. $\theta_{jc}$ is provided for reference. The maximum junction temperature is 150°C.

The maximum power dissipation allowed for eX devices is a function of $\theta_{ja}$. A sample calculation of the absolute maximum power dissipation allowed for a TQFP 100-pin package at commercial temperature and still air is as follows:

$$\text{Maximum Power Allowed} = \frac{\text{Max. junction temp. (°C)} - \text{Max. ambient temp. (°C)}}{\theta_{ja}(°C/W)} = \frac{150°C - 70°C}{33.5°C/W} = 2.39W$$

| Package Type | Pin Count | $\theta_{jc}$ | $\theta_{ja}$ Still Air | 1.0 m/s 200 ft/min | 2.5 m/s 500 ft/min | Units |
|---|---|---|---|---|---|---|
| Thin Quad Flat Pack (TQFP) | 64 | 12.0 | 42.4 | 36.3 | 34.0 | °C/W |
| Thin Quad Flat Pack (TQFP) | 100 | 14.0 | 33.5 | 27.4 | 25.0 | °C/W |

# Timing Characteristics

Timing characteristics for eX devices fall into three categories: family-dependent, device-dependent, and design-dependent. The input and output buffer characteristics are common to all eX family members. Internal routing delays are device-dependent. Design dependency means actual delays are not determined until after placement and routing of the user's design are complete. Delay values may then be determined by using the Timer utility or performing simulation with post-layout delays.

## Critical Nets and Typical Nets

Propagation delays are expressed only for typical nets, which are used for initial design performance evaluation. Critical net delays can then be applied to the most timing critical paths. Critical nets are determined by net property assignment prior to placement and routing. Up to six percent of the nets in a design may be designated as critical.

## Long Tracks

Some nets in the design use long tracks. Long tracks are special routing resources that span multiple rows, columns, or modules. Long tracks employ three to five antifuse connections. This increases capacitance and resistance, resulting in longer net delays for macros connected to long tracks. Typically, no more than six percent of nets in a fully utilized device require long tracks. Long tracks contribute approximately 4 ns to 8.4 ns delay. This additional delay is represented statistically in higher fanout routing delays.

## Timing Derating

eX devices are manufactured with a CMOS process. Therefore, device performance varies according to temperature, voltage, and process changes. Minimum timing parameters reflect maximum operating voltage, minimum operating temperature, and best-case processing. Maximum timing parameters reflect minimum operating voltage, maximum operating temperature, and worst-case processing.

### Temperature and Voltage Derating Factors

*Table 1-16 •* **Temperature and Voltage Derating Factors**
**(Normalized to Worst-Case Commercial, $T_J$ = 70°C, VCCA = 2.3V)**

| VCCA | Junction Temperature ($T_J$) | | | | | | |
|------|------|------|------|------|------|------|------|
|      | −55  | −40  | 0    | 25   | 70   | 85   | 125  |
| 2.3  | 0.79 | 0.80 | 0.87 | 0.88 | 1.00 | 1.04 | 1.13 |
| 2.5  | 0.74 | 0.74 | 0.81 | 0.83 | 0.93 | 0.97 | 1.06 |
| 2.7  | 0.69 | 0.70 | 0.76 | 0.78 | 0.88 | 0.91 | 1.00 |

*eX FPGA Architecture and Characteristics*

*Table 1-18 •* **eX Family Timing Characteristics**
**(Worst-Case Commercial Conditions VCCA = 2.3 V, VCCI = 4.75 V, T$_J$ = 70°C)**

| Parameter | Description | –P Speed Min. | –P Speed Max. | Std Speed Min. | Std Speed Max. | –F Speed Min. | –F Speed Max. | Units |
|---|---|---|---|---|---|---|---|---|
| **Dedicated (Hard-Wired) Array Clock Networks** | | | | | | | | |
| t$_{HCKH}$ | Input LOW to HIGH (Pad to R-Cell Input) | | 1.1 | | 1.6 | | 2.3 | ns |
| t$_{HCKL}$ | Input HIGH to LOW (Pad to R-Cell Input) | | 1.1 | | 1.6 | | 2.3 | ns |
| t$_{HPWH}$ | Minimum Pulse Width HIGH | 1.4 | | 2.0 | | 2.8 | | ns |
| t$_{HPWL}$ | Minimum Pulse Width LOW | 1.4 | | 2.0 | | 2.8 | | ns |
| t$_{HCKSW}$ | Maximum Skew | | <0.1 | | <0.1 | | <0.1 | ns |
| t$_{HP}$ | Minimum Period | 2.8 | | 4.0 | | 5.6 | | ns |
| f$_{HMAX}$ | Maximum Frequency | | 357 | | 250 | | 178 | MHz |
| **Routed Array Clock Networks** | | | | | | | | |
| t$_{RCKH}$ | Input LOW to HIGH (Light Load) (Pad to R-Cell Input) MAX. | | 1.1 | | 1.6 | | 2.2 | ns |
| t$_{RCKL}$ | Input HIGH to LOW (Light Load) (Pad to R-Cell Input) MAX. | | 1.0 | | 1.4 | | 2.0 | ns |
| t$_{RCKH}$ | Input LOW to HIGH (50% Load) (Pad to R-Cell Input) MAX. | | 1.2 | | 1.7 | | 2.4 | ns |
| t$_{RCKL}$ | Input HIGH to LOW (50% Load) (Pad to R-Cell Input) MAX. | | 1.2 | | 1.7 | | 2.4 | ns |
| t$_{RCKH}$ | Input LOW to HIGH (100% Load) (Pad to R-Cell Input) MAX. | | 1.3 | | 1.9 | | 2.6 | ns |
| t$_{RCKL}$ | Input HIGH to LOW (100% Load) (Pad to R-Cell Input) MAX. | | 1.3 | | 1.9 | | 2.6 | ns |
| t$_{RPWH}$ | Min. Pulse Width HIGH | 1.5 | | 2.1 | | 3.0 | | ns |
| t$_{RPWL}$ | Min. Pulse Width LOW | 1.5 | | 2.1 | | 3.0 | | ns |
| t$_{RCKSW}$* | Maximum Skew (Light Load) | | 0.2 | | 0.3 | | 0.4 | ns |
| t$_{RCKSW}$* | Maximum Skew (50% Load) | | 0.1 | | 0.2 | | 0.3 | ns |
| t$_{RCKSW}$* | Maximum Skew (100% Load) | | 0.1 | | 0.1 | | 0.2 | ns |

*Note: *Clock skew improves as the clock network becomes more heavily loaded.*

*Table 1-19 •* **eX Family Timing Characteristics**
**(Worst-Case Commercial Conditions VCCA = 2.3V, VCCI = 2.3 V or 3.0V, T$_J$ = 70°C)**

| Parameter | Description | '–P' Speed Min. | '–P' Speed Max. | 'Std' Speed Min. | 'Std' Speed Max. | '–F' Speed Min. | '–F' Speed Max. | Units |
|---|---|---|---|---|---|---|---|---|
| **Dedicated (Hard-Wired) Array Clock Networks** | | | | | | | | |
| t$_{HCKH}$ | Input LOW to HIGH (Pad to R-Cell Input) | | 1.1 | | 1.6 | | 2.3 | ns |
| t$_{HCKL}$ | Input HIGH to LOW (Pad to R-Cell Input) | | 1.1 | | 1.6 | | 2.3 | ns |
| t$_{HPWH}$ | Minimum Pulse Width HIGH | 1.4 | | 2.0 | | 2.8 | | ns |
| t$_{HPWL}$ | Minimum Pulse Width LOW | 1.4 | | 2.0 | | 2.8 | | ns |
| t$_{HCKSW}$ | Maximum Skew | | <0.1 | | <0.1 | | <0.1 | ns |
| t$_{HP}$ | Minimum Period | 2.8 | | 4.0 | | 5.6 | | ns |
| f$_{HMAX}$ | Maximum Frequency | | 357 | | 250 | | 178 | MHz |
| **Routed Array Clock Networks** | | | | | | | | |
| t$_{RCKH}$ | Input LOW to HIGH (Light Load) (Pad to R-Cell Input) MAX. | | 1.0 | | 1.4 | | 2.0 | ns |
| t$_{RCKL}$ | Input HIGH to LOW (Light Load) (Pad to R-Cell Input) MAX. | | 1.0 | | 1.4 | | 2.0 | ns |
| t$_{RCKH}$ | Input LOW to HIGH (50% Load) (Pad to R-Cell Input) MAX. | | 1.2 | | 1.7 | | 2.4 | ns |
| t$_{RCKL}$ | Input HIGH to LOW (50% Load) (Pad to R-Cell Input) MAX. | | 1.2 | | 1.7 | | 2.4 | ns |
| t$_{RCKH}$ | Input LOW to HIGH (100% Load) (Pad to R-Cell Input) MAX. | | 1.4 | | 2.0 | | 2.8 | ns |
| t$_{RCKL}$ | Input HIGH to LOW (100% Load) (Pad to R-Cell Input) MAX. | | 1.4 | | 2.0 | | 2.8 | ns |
| t$_{RPWH}$ | Min. Pulse Width HIGH | 1.4 | | 2.0 | | 2.8 | | ns |
| t$_{RPWL}$ | Min. Pulse Width LOW | 1.4 | | 2.0 | | 2.8 | | ns |
| t$_{RCKSW}$* | Maximum Skew (Light Load) | | 0.2 | | 0.3 | | 0.4 | ns |
| t$_{RCKSW}$* | Maximum Skew (50% Load) | | 0.2 | | 0.2 | | 0.3 | ns |
| t$_{RCKSW}$* | Maximum Skew (100% Load) | | 0.1 | | 0.1 | | 0.2 | ns |

*Note: *Clock skew improves as the clock network becomes more heavily loaded.*

*Table 1-20 •* **eX Family Timing Characteristics**
   **(Worst-Case Commercial Conditions VCCA = 2.3 V, T$_J$ = 70°C)**

| Parameter | Description | –P Speed Min. | –P Speed Max. | Std Speed Min. | Std Speed Max. | –F Speed Min. | –F Speed Max. | Units |
|---|---|---|---|---|---|---|---|---|
| **2.5 V LVCMOS Output Module Timing[1] (VCCI = 2.3 V)** | | | | | | | | |
| t$_{DLH}$ | Data-to-Pad LOW to HIGH | | 3.3 | | 4.7 | | 6.6 | ns |
| t$_{DHL}$ | Data-to-Pad HIGH to LOW | | 3.5 | | 5.0 | | 7.0 | ns |
| t$_{DHLS}$ | Data-to-Pad HIGH to LOW—Low Slew | | 11.6 | | 16.6 | | 23.2 | ns |
| t$_{ENZL}$ | Enable-to-Pad, Z to L | | 2.5 | | 3.6 | | 5.1 | ns |
| t$_{ENZLS}$ | Enable-to-Pad Z to L—Low Slew | | 11.8 | | 16.9 | | 23.7 | ns |
| t$_{ENZH}$ | Enable-to-Pad, Z to H | | 3.4 | | 4.9 | | 6.9 | ns |
| t$_{ENLZ}$ | Enable-to-Pad, L to Z | | 2.1 | | 3.0 | | 4.2 | ns |
| t$_{ENHZ}$ | Enable-to-Pad, H to Z | | 2.4 | | 5.67 | | 7.94 | ns |
| d$_{TLH}$ | Delta Delay vs. Load LOW to HIGH | | 0.034 | | 0.046 | | 0.066 | ns/pF |
| d$_{THL}$ | Delta Delay vs. Load HIGH to LOW | | 0.016 | | 0.022 | | 0.05 | ns/pF |
| d$_{THLS}$ | Delta Delay vs. Load HIGH to LOW—Low Slew | | 0.05 | | 0.072 | | 0.1 | ns/pF |
| **3.3 V LVTTL Output Module Timing[1] (VCCI = 3.0 V)** | | | | | | | | |
| t$_{DLH}$ | Data-to-Pad LOW to HIGH | | 2.8 | | 4.0 | | 5.6 | ns |
| t$_{DHL}$ | Data-to-Pad HIGH to LOW | | 2.7 | | 3.9 | | 5.4 | ns |
| t$_{DHLS}$ | Data-to-Pad HIGH to LOW—Low Slew | | 9.7 | | 13.9 | | 19.5 | ns |
| t$_{ENZL}$ | Enable-to-Pad, Z to L | | 2.2 | | 3.2 | | 4.4 | ns |
| t$_{ENZLS}$ | Enable-to-Pad Z to L—Low Slew | | 9.7 | | 13.9 | | 19.6 | ns |
| t$_{ENZH}$ | Enable-to-Pad, Z to H | | 2.8 | | 4.0 | | 5.6 | ns |
| t$_{ENLZ}$ | Enable-to-Pad, L to Z | | 2.8 | | 4.0 | | 5.6 | ns |
| t$_{ENHZ}$ | Enable-to-Pad, H to Z | | 2.6 | | 3.8 | | 5.3 | ns |
| d$_{TLH}$ | Delta Delay vs. Load LOW to HIGH | | 0.02 | | 0.03 | | 0.046 | ns/pF |
| d$_{THL}$ | Delta Delay vs. Load HIGH to LOW | | 0.016 | | 0.022 | | 0.05 | ns/pF |
| d$_{THLS}$ | Delta Delay vs. Load HIGH to LOW—Low Slew | | 0.05 | | 0.072 | | 0.1 | ns/pF |
| **5.0 V TTL Output Module Timing* (VCCI = 4.75 V)** | | | | | | | | |
| t$_{DLH}$ | Data-to-Pad LOW to HIGH | | 2.0 | | 2.9 | | 4.0 | ns |
| t$_{DHL}$ | Data-to-Pad HIGH to LOW | | 2.6 | | 3.7 | | 5.2 | ns |
| t$_{DHLS}$ | Data-to-Pad HIGH to LOW—Low Slew | | 6.8 | | 9.7 | | 13.6 | ns |
| t$_{ENZL}$ | Enable-to-Pad, Z to L | | 1.9 | | 2.7 | | 3.8 | ns |
| t$_{ENZLS}$ | Enable-to-Pad Z to L—Low Slew | | 6.8 | | 9.8 | | 13.7 | ns |
| t$_{ENZH}$ | Enable-to-Pad, Z to H | | 2.1 | | 3.0 | | 4.1 | ns |
| t$_{ENLZ}$ | Enable-to-Pad, L to Z | | 3.3 | | 4.8 | | 6.6 | ns |

*Note:* *Delays based on 35 pF loading.*

| TQ64 | | | TQ64 | | |
|---|---|---|---|---|---|
| Pin Number | eX64 Function | eX128 Function | Pin Number | eX64 Function | eX128 Function |
| 1 | GND | GND | 33 | GND | GND |
| 2 | TDI, I/O | TDI, I/O | 34 | I/O | I/O |
| 3 | I/O | I/O | 35 | I/O | I/O |
| 4 | TMS | TMS | 36 | VCCA | VCCA |
| 5 | GND | GND | 37 | VCCI | VCCI |
| 6 | VCCI | VCCI | 38 | I/O | I/O |
| 7 | I/O | I/O | 39 | I/O | I/O |
| 8 | I/O | I/O | 40 | NC | I/O |
| 9 | NC | I/O | 41 | NC | I/O |
| 10 | NC | I/O | 42 | I/O | I/O |
| 11 | TRST, I/O | TRST, I/O | 43 | I/O | I/O |
| 12 | I/O | I/O | 44 | VCCA | VCCA |
| 13 | NC | I/O | 45* | GND/LP | GND/ LP |
| 14 | GND | GND | 46 | GND | GND |
| 15 | I/O | I/O | 47 | I/O | I/O |
| 16 | I/O | I/O | 48 | I/O | I/O |
| 17 | I/O | I/O | 49 | I/O | I/O |
| 18 | I/O | I/O | 50 | I/O | I/O |
| 19 | VCCI | VCCI | 51 | I/O | I/O |
| 20 | I/O | I/O | 52 | VCCI | VCCI |
| 21 | PRB, I/O | PRB, I/O | 53 | I/O | I/O |
| 22 | VCCA | VCCA | 54 | I/O | I/O |
| 23 | GND | GND | 55 | CLKA | CLKA |
| 24 | I/O | I/O | 56 | CLKB | CLKB |
| 25 | HCLK | HCLK | 57 | VCCA | VCCA |
| 26 | I/O | I/O | 58 | GND | GND |
| 27 | I/O | I/O | 59 | PRA, I/O | PRA, I/O |
| 28 | I/O | I/O | 60 | I/O | I/O |
| 29 | I/O | I/O | 61 | VCCI | VCCI |
| 30 | I/O | I/O | 62 | I/O | I/O |
| 31 | I/O | I/O | 63 | I/O | I/O |
| 32 | TDO, I/O | TDO, I/O | 64 | TCK, I/O | TCK, I/O |

*Note:*   *\*Please read the LP pin descriptions for restrictions on their use.*

# TQ100
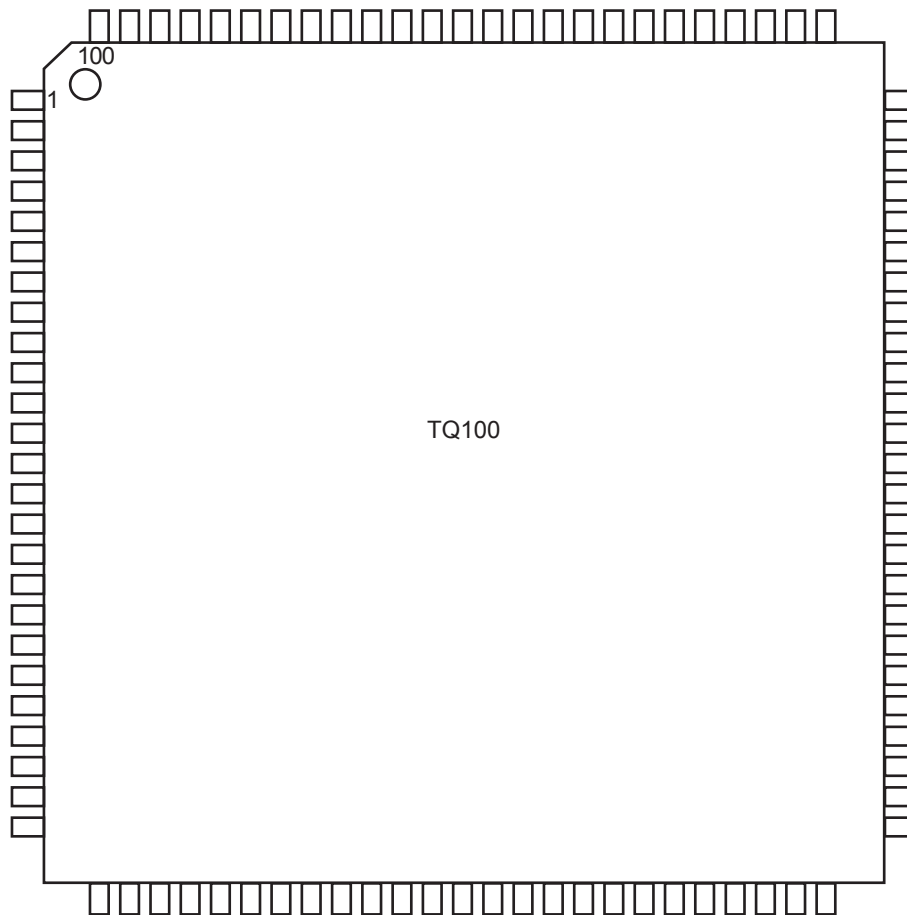


Note: For Package Manufacturing and Environmental information, visit Resource center at
www.microsemi.com/soc/products/rescenter/package/index.html.

# 3 – Datasheet Information

## List of Changes

The following table lists critical changes that were made in the current version of the document.

| Revision | Changes | Page |
|---|---|---|
| Revision 10 (October 2012) | The "User Security" section was revised to clarify that although no existing security measures can give an absolute guarantee, Microsemi FPGAs implement industry standard security (SAR 34677). | 1-5 |
| | Package names used in the "Product Profile" section and "Package Pin Assignments" section were revised to match standards given in *Package Mechanical Drawings* (SAR 34779). | I<br>2-1 |
| Revision 9 (June 2011) | The versioning system for datasheets has been changed. Datasheets are assigned a revision number that increments each time the datasheet is revised. The "eX Device Status" table indicates the status for each device in the device family. | II |
| | The Chip Scale packages (CS49, CS128, CS181) are no longer offered for eX devices. They have been removed from the product family information. Pin tables for CSP packages have been removed from the datasheet (SAR 32002). | N/A |
| Revision 8 (v4.3, June 2006) | The "Ordering Information" was updated with RoHS information. The TQFP measurement was also updated. | II |
| | The "Dedicated Test Mode" was updated. | 1-10 |
| | Note 5 was added to the "3.3 V LVTTL Electrical Specifications" and "5.0 V TTL Electrical Specifications" tables | 1-18 |
| | The "LP Low Power Pin" description was updated. | 1-31 |
| Revision 7 (v4.2, June 2004) | The "eX Timing Model" was updated. | 1-22 |
| v4.1 | The "Development Tool Support" section was updated. | 1-13 |
| | The "Package Thermal Characteristics" section was updated. | 1-21 |
| v4.0 | The "Product Profile" section was updated. | 1-I |
| | The "Ordering Information" section was updated. | 1-II |
| | The "Temperature Grade Offerings" section is new. | 1-III |
| | The "Speed Grade and Temperature Grade Matrix" section is new. | 1-III |
| | The "eX FPGA Architecture and Characteristics" section was updated. | 1-1 |
| | The "Clock Resources" section was updated. | 1-3 |
| | Table 1-1 •Connections of Routed Clock Networks, CLKA and CLKB is new. | 1-4 |
| | The "User Security" section was updated. | 1-5 |
| | The "I/O Modules" section was updated. | 1-5 |
| | The "Hot-Swapping" section was updated. | 1-6 |
| | The "Power Requirements" section was updated. | 1-6 |
| | The "Low Power Mode" section was updated. | 1-6 |
| | The "Boundary Scan Testing (BST)" section was updated. | 1-10 |
| | The "Dedicated Test Mode" section was updated. | 1-10 |

| Revision | Changes | Page |
|---|---|---|
| v4.0 (continued) | The "Flexible Mode" section was updated. | 1-10 |
| | Table 1-5 •Boundary-Scan Pin Configurations and Functions is new. | 1-11 |
| | The "TRST Pin" section was updated. | 1-11 |
| | The "Probing Capabilities" section is new. | 1-12 |
| | The "Programming" section was updated. | 1-12 |
| | The "Probing Capabilities" section was updated. | 1-12 |
| | The "Silicon Explorer II Probe" section was updated. | 1-12 |
| | The "Design Considerations" section was updated. | 1-13 |
| | The "Development Tool Support" section was updated. | 1-13 |
| | The "Absolute Maximum Ratings*" section was updated. | 1-16 |
| | The "Temperature and Voltage Derating Factors" section was updated. | 1-26 |
| | The "TDI, I/O Test Data Input" section was updated. | 1-31 |
| | The "TDO, I/O Test Data Output" section was updated. | 1-31 |
| | The "TMS Test Mode Select" section was updated. | 1-32 |
| | The "TRST, I/O Boundary Scan Reset Pin" section was updated. | 1-32 |
| | All VSV pins were changed to VCCA. The change affected the following pins:<br>64-Pin TQFP –               Pin 36<br>100-Pin TQFP –               Pin 57<br>49-Pin CSP –               Pin D5<br>128-Pin CSP–               Pin H11 and Pin J1 for eX256<br>180-Pin CSP –               Pins J12 and K2 | |
| v3.0 | The "Recommended Operating Conditions" section has been changed. | 1-16 |
| | The "3.3 V LVTTL Electrical Specifications" section has been updated. | 1-18 |
| | The "5.0 V TTL Electrical Specifications" section has been updated. | 1-18 |
| | The "Total Dynamic Power (mW)" section is new. | 1-9 |
| | The "System Power at 5%, 10%, and 15% Duty Cycle" section is new. | 1-9 |
| | The "eX Timing Model" section has been updated. | 1-22 |
| v2.0.1 | The I/O Features table, Table 1-2 on page 1-6, was updated. | 1-6 |
| | The table, "Standby Power of eX Devices in LP Mode Typical Conditions, VCCA, VCCI = 2.5 V,  TJ = 25° C" section, was updated. | 1-7 |
| | "Typical eX Standby Current at 25°C" section is a new table. | 1-16 |
| | The table in the section, "Package Thermal Characteristics" section has been updated for the 49-Pin CSP. | 1-21 |
| | The "eX Timing Model" section has been updated. | 1-22 |
| | The timing numbers found in, "eX Family Timing Characteristics" section have been updated. | 1-27 |
| | The $V_{SV}$ pin has been added to the "Pin Description" section. | 1-31 |
| | Please see the following pin tables for the $V_{SV}$ pin and an important footnote including the pin: "TQ64", "TQ100", "128-Pin CSP", and "180-Pin CSP". | 2-1, 2-3, 2-6, 2-11 |
| | The figure, "TQ64" section has been updated. | 2-1 |

| Revision | Changes | Page |
|---|---|---|
| Advance v0.4 | In the Product Profile, the Maximum User I/Os for eX64 was changed to 84. | 1-I |
| | In the Product Profile table, the Maximum User I/Os for eX128 was changed to 100. | 1-I |
| Advance v0.3 | The Mechanical Drawings section has been removed from the data sheet. The mechanical drawings are now contained in a separate document, "Package Characteristics and Mechanical Drawings," available on the Actel web site. | |
| | A new section describing "Clock Resources"has been added. | 1-3 |
| | A new table describing "I/O Features"has been added. | 1-6 |
| | The "Pin Description"section has been updated and clarified. | 1-31 |
| | The original Electrical Specifications table was separated into two tables (2.5V and 3.3/5.0V). In both tables, several different currents are specified for $V_{OH}$ and $V_{OL}$. | Page 8 and 9 |
| | A new table listing 2.5V low power specifications and associated power graphs were added. | page 9 |
| | Pin functions for eX256 TQ100 have been added to the "TQ100"table. | 2-3 |
| | A CS49 pin drawing and pin assignment table including eX64 and eX128 pin functions have been added. | page 26 |
| | A CS128 pin drawing and pin assignment table including eX64, eX128, and eX256 pin functions have been added. | pages 26-27 |
| | A CS180 pin drawing and pin assignment table for eX256 pin functions have been added. | pages 27, 31 |
| Advance v0.2 | The following table note was added to the eX Timing Characteristics table for clarification: Clock skew improves as the clock network becomes more heavily loaded. | pages 14-15 |