Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.
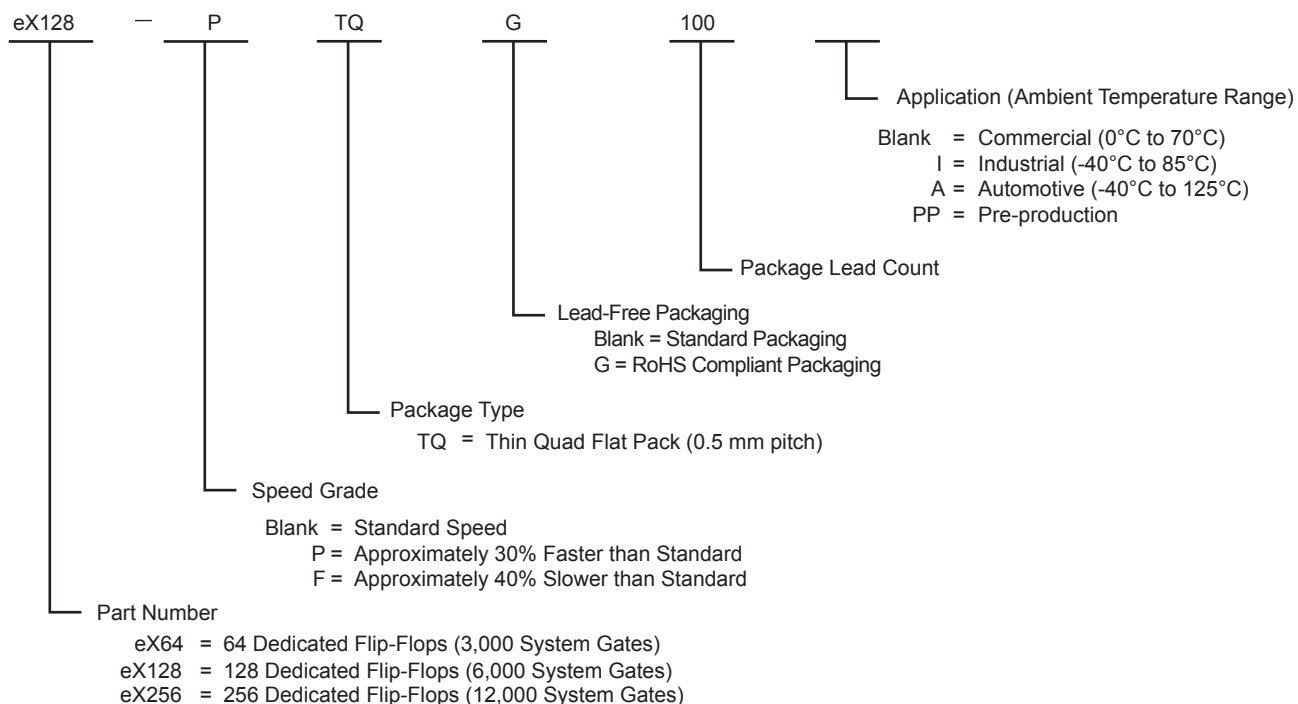
Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	128
Total RAM Bits	-
Number of I/O	41
Number of Gates	3000
Voltage - Supply	2.3V ~ 2.7V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 125°C (TA)
Package / Case	64-LQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/ex64-tq64a

Ordering Information

```
eX128        —        P        TQ        G        100
  │                   │        │         │         │
  │                   │        │         │         └──────── Application (Ambient Temperature Range)
  │                   │        │         │                      Blank  =  Commercial (0°C to 70°C)
  │                   │        │         │                          I  =  Industrial (-40°C to 85°C)
  │                   │        │         │                          A  =  Automotive (-40°C to 125°C)
  │                   │        │         │                         PP  =  Pre-production
  │                   │        │         │
  │                   │        │         └──────── Package Lead Count
  │                   │        │
  │                   │        └──────── Lead-Free Packaging
  │                   │                     Blank = Standard Packaging
  │                   │                     G = RoHS Compliant Packaging
  │                   │
  │                   └──────── Package Type
  │                               TQ  =  Thin Quad Flat Pack (0.5 mm pitch)
  │
  └──────── Speed Grade
               Blank  =  Standard Speed
                   P  =  Approximately 30% Faster than Standard
                   F  =  Approximately 40% Slower than Standard

  └──────── Part Number
               eX64   =  64 Dedicated Flip-Flops (3,000 System Gates)
               eX128  =  128 Dedicated Flip-Flops (6,000 System Gates)
               eX256  =  256 Dedicated Flip-Flops (12,000 System Gates)
```

eX Device Status

eX Devices	Status
eX64	Production
eX128	Production
eX256	Production

Plastic Device Resources

Device	User I/Os (Including Clock Buffers)	
	TQ64	**TQ100**
eX64	41	56
eX128	46	70
eX256	—	81

Note: TQ = Thin Quad Flat Pack

Temperature Grade Offerings

Device\ Package	TQ64	TQ100
eX64	C, I, A	C, I, A
eX128	C, I, A	C, I, A
eX256	C, I, A	C, I, A

Note: *C = Commercial*

     I = Industrial

     A = Automotive

Speed Grade and Temperature Grade Matrix

	–F	Std	–P
C	✓	✓	✓
I		✓	✓
A		✓	

Note: *P = Approximately 30% faster than Standard*

    –F = Approximately 40% slower than Standard

    Refer to the eX Automotive Family FPGAs *datasheet for details on automotive temperature offerings.*

Contact your local Microsemi representative for device availability.

Module Organization

C-cell and R-cell logic modules are arranged into horizontal banks called Clusters, each of which contains two C-cells and one R-cell in a C-R-C configuration.

Clusters are further organized into modules called SuperClusters for improved design efficiency and device performance, as shown in Figure 1-3. Each SuperCluster is a two-wide grouping of Clusters.
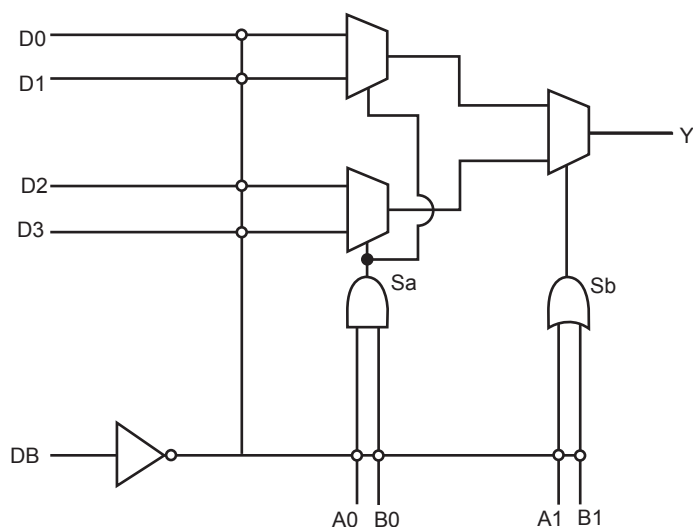
Figure 1-2 • **C-Cell**
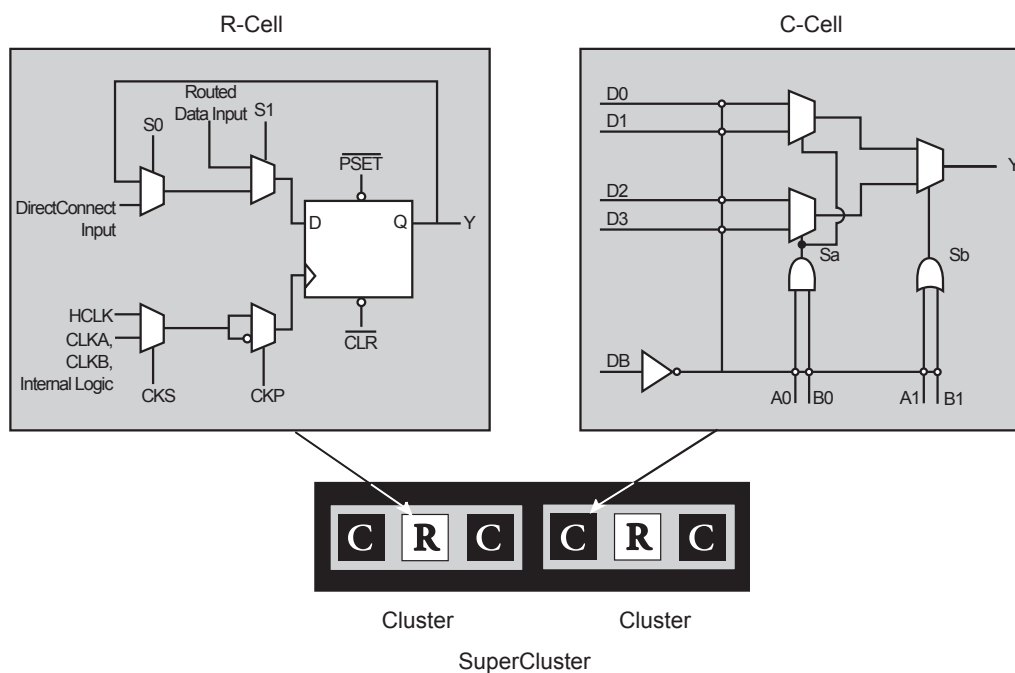
Figure 1-3 • **Cluster Organization**

Table 1-2 describes the I/O features of eX devices. For more information on I/Os, refer to *Microsemi eX, SX-A, and RT54SX-S I/Os* application note.

Table 1-2 • **I/O Features**

Function	Description
Input Buffer Threshold Selection	• 5.0V TTL • 3.3V LVTTL • 2.5V LVCMOS2
Nominal Output Drive	• 5.0V TTL/CMOS • 3.3V LVTTL • 2.5V LVCMOS 2
Output Buffer	"Hot-Swap" Capability • I/O on an unpowered device does not sink current • Can be used for "cold sparing" Selectable on an individual I/O basis Individually selectable low-slew option
Power-Up	Individually selectable pull ups and pull downs during power-up (default is to power up in tristate) Enables deterministic power-up of device V_{CCA} and V_{CCI} can be powered in any order

The eX family supports mixed-voltage operation and is designed to tolerate 5.0 V inputs in each case.

A detailed description of the I/O pins in eX devices can be found in "Pin Description" on page 1-31.

Hot-Swapping

eX I/Os are configured to be hot-swappable. During power-up/down (or partial up/down), all I/Os are tristated, provided V_{CCA} ramps up within a diode drop of V_{CCI}. V_{CCA} and V_{CCI} do not have to be stable. during power-up/down, and they do not require a specific power-up or power-down sequence in order to avoid damage to the eX devices. In addition, all outputs can be programmed to have a weak resistor pull-up or pull-down for output tristate at power-up. After the eX device is plugged into an electrically active system, the device will not degrade the reliability of or cause damage to the host system. The device's output pins are driven to a high impedance state until normal chip operating conditions are reached. Please see the application note, *Microsemi SX-A and RT54SX-S Devices in Hot-Swap and Cold-Sparing Applications*, which also applies to the eX devices, for more information on hot swapping.

Power Requirements

Power consumption is extremely low for the eX family due to the low capacitance of the antifuse interconnects. The antifuse architecture does not require active circuitry to hold a charge (as do SRAM or EPROM), making it the lowest-power FPGA architecture available today.

Low Power Mode

The eX family has been designed with a Low Power Mode. This feature, activated with setting the special LP pin to HIGH for a period longer than 800 ns, is particularly useful for battery-operated systems where battery life is a primary concern. In this mode, the core of the device is turned off and the device consumes minimal power with low standby current. In addition, all input buffers are turned off, and all outputs and bidirectional buffers are tristated when the device enters this mode. Since the core of the device is turned off, the states of the registers are lost. The device must be re-initialized when returning to normal operating mode. I/Os can be driven during LP mode. For details, refer to the *Design for Low Power in Microsemi Antifuse FPGAs* application note under the section Using the LP Mode Pin on eX Devices. Clock pins should be driven either HIGH or LOW and should not float; otherwise, they will draw current and burn power. The device must be re-initialized when exiting LP mode.
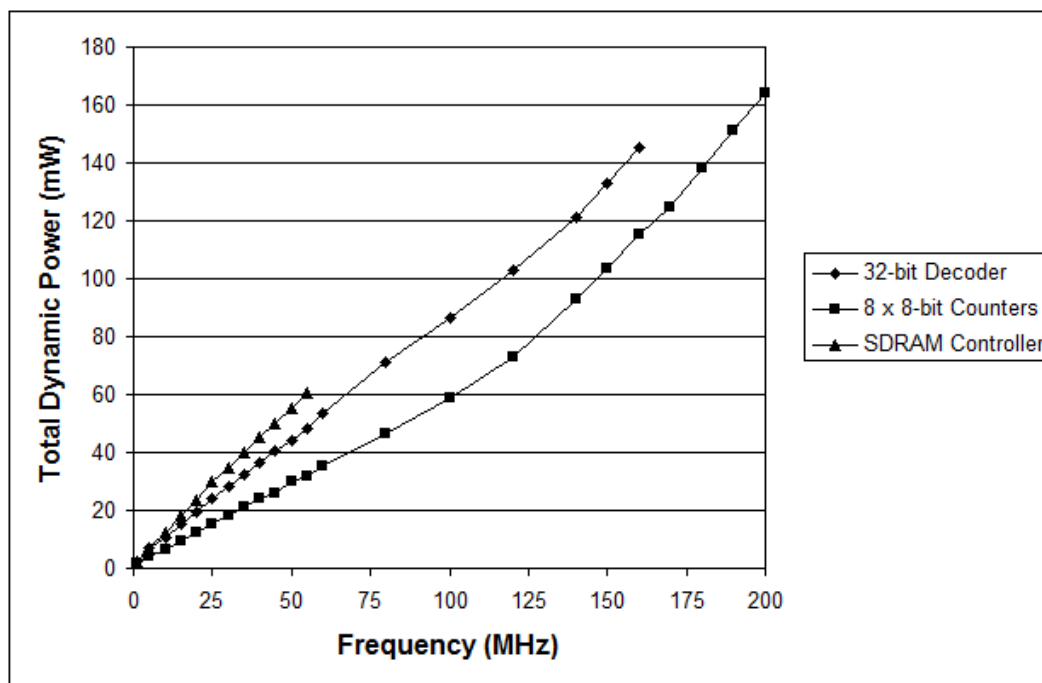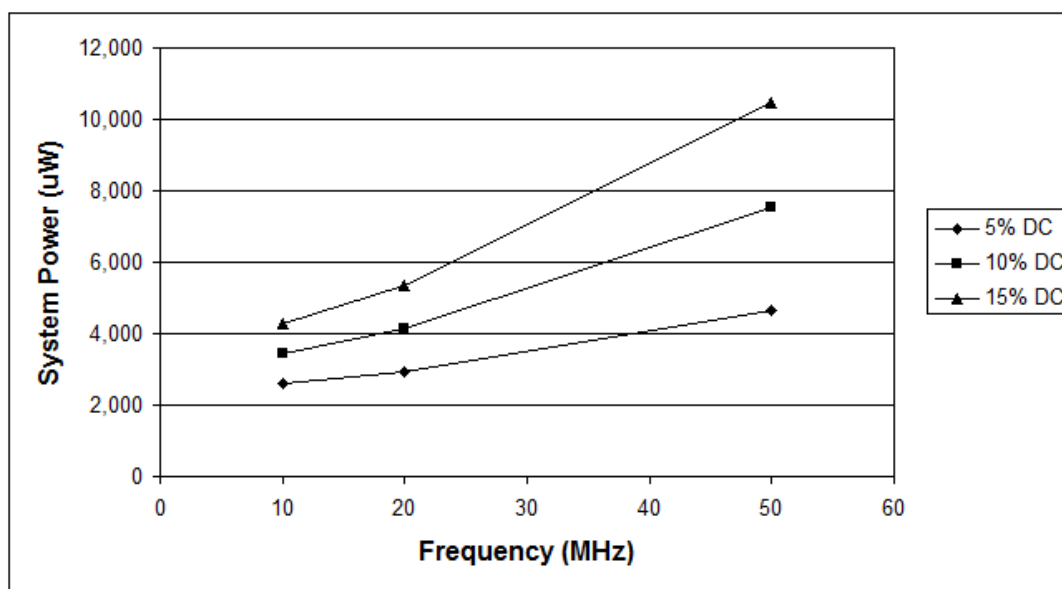
Figure 1-10 • **Total Dynamic Power (mW)**

Figure 1-11 • **System Power at 5%, 10%, and 15% Duty Cycle**

Programming

Device programming is supported through Silicon Sculptor series of programmers. In particular, Silicon Sculptor II is a compact, robust, single-site and multi-site device programmer for the PC.

With standalone software, Silicon Sculptor II allows concurrent programming of multiple units from the same PC, ensuring the fastest programming times possible. Each fuse is subsequently verified by Silicon Sculptor II to insure correct programming. In addition, integrity tests ensure that no extra fuses are programmed. Silicon Sculptor II also provides extensive hardware self-testing capability.

The procedure for programming an eX device using Silicon Sculptor II is as follows:

1. Load the *.AFM file
2. Select the device to be programmed
3. Begin programming

When the design is ready to go to production, Microsemi offers device volume-programming services either through distribution partners or via in-house programming from the factory.

For more details on programming eX devices, please refer to the *Programming Antifuse Devices* application note and the *Silicon Sculptor II User's Guide*.

Probing Capabilities

eX devices provide internal probing capability that is accessed with the JTAG pins. The Silicon Explorer II Diagnostic hardware is used to control the TDI, TCK, TMS and TDO pins to select the desired nets for debugging. The user simply assigns the selected internal nets in the Silicon Explorer II software to the PRA/PRB output pins for observation. Probing functionality is activated when the BST pins are in JTAG mode and the TRST pin is driven HIGH or left floating. If the TRST pin is held LOW, the TAP controller will remain in the Test-Logic-Reset state so no probing can be performed. The Silicon Explorer II automatically places the device into JTAG mode, but the user must drive the TRST pin HIGH or allow the internal pull-up resistor to pull TRST HIGH.

When you select the **Reserve Probe Pin** box, as shown in Figure 1-12 on page 1-10, the layout tool reserves the PRA and PRB pins as dedicated outputs for probing. This reserve option is merely a guideline. If the Layout tool requires that the PRA and PRB pins be user I/Os to achieve successful layout, the tool will use these pins for user I/Os. If you assign user I/Os to the PRA and PRB pins and select the **Reserve Probe Pin** option, Designer Layout will override the "Reserve Probe Pin" option and place your user I/Os on those pins.

To allow for probing capabilities, the security fuse must not be programmed. Programming the security fuse will disable the probe circuitry. Table 1-8 on page 1-13 summarizes the possible device configurations for probing once the device leaves the Test-Logic-Reset JTAG state.

Silicon Explorer II Probe

Silicon Explorer II is an integrated hardware and software solution that, in conjunction with Microsemi Designer software tools, allow users to examine any of the internal nets of the device while it is operating in a prototype or a production system. The user can probe into an eX device via the PRA and PRB pins without changing the placement and routing of the design and without using any additional resources. Silicon Explorer II's noninvasive method does not alter timing or loading effects, thus shortening the debug cycle.

Silicon Explorer II does not require re-layout or additional MUXes to bring signals out to an external pin, which is necessary when using programmable logic devices from other suppliers.

Silicon Explorer II samples data at 100 MHz (asynchronous) or 66 MHz (synchronous). Silicon Explorer II attaches to a PC's standard COM port, turning the PC into a fully functional 18-channel logic analyzer. Silicon Explorer II allows designers to complete the design verification process at their desks and reduces verification time from several hours per cycle to a few seconds.

The Silicon Explorer II tool uses the boundary scan ports (TDI, TCK, TMS and TDO) to select the desired nets for verification. The selected internal nets are assigned to the PRA/PRB pins for observation. Figure 1-13 on page 1-13 illustrates the interconnection between Silicon Explorer II and the eX device to perform in-circuit verification.

Design Considerations

The TDI, TCK, TDO, PRA, and PRB pins should not be used as input or bidirectional ports. Since these pins are active during probing, critical signals input through these pins are not available while probing. In addition, the Security Fuse should not be programmed because doing so disables the probe circuitry. It is recommended to use a series 70Ω termination resistor on every probe connector (TDI, TCK, TMS, TDO, PRA, PRB). The 70Ω series termination is used to prevent data transmission corruption during probing and reading back the checksum.

Table 1-8 • **Device Configuration Options for Probe Capability (TRST pin reserved)**

JTAG Mode	TRST[1]	Security Fuse Programmed	PRA, PRB[2]	TDI, TCK, TDO[2]
Dedicated	LOW	No	User I/O[3]	Probing Unavailable
Flexible	LOW	No	User I/O[3]	User I/O[3]
Dedicated	HIGH	No	Probe Circuit Outputs	Probe Circuit Inputs
Flexible	HIGH	No	Probe Circuit Outputs	Probe Circuit Inputs
–	–	Yes	Probe Circuit Secured	Probe Circuit Secured

Notes:

1. If TRST pin is not reserved, the device behaves according to TRST = HIGH in the table.

2. Avoid using the TDI, TCK, TDO, PRA, and PRB pins as input or bidirectional ports. Since these pins are active during probing, input signals will not pass through these pins and may cause contention.

3. If no user signal is assigned to these pins, they will behave as unused I/Os in this mode. Unused pins are automatically tristated by Microsemi Designer software.
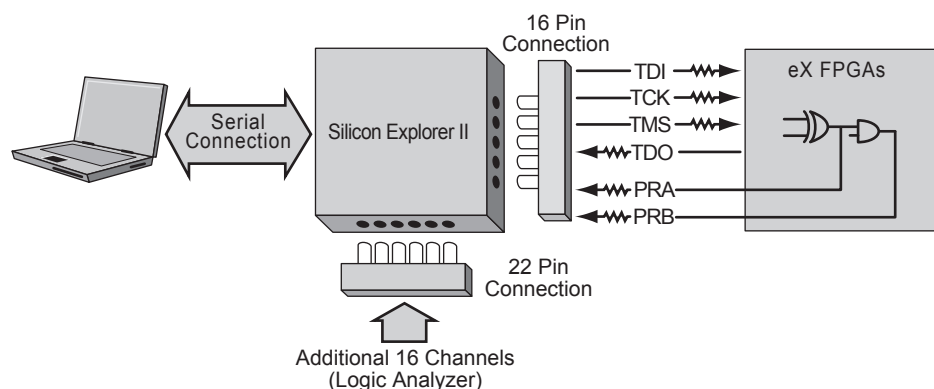

Figure 1-13 • **Silicon Explorer II Probe Setup**

Development Tool Support

The eX family of FPGAs is fully supported by both Libero® Integrated Design Environment and Designer FPGA Development software. Libero IDE is a design management environment that streamlines the design flow. Libero IDE provides an integrated design manager that seamlessly integrates design tools while guiding the user through the design flow, managing all design and log files, and passing necessary design data among tools. Additionally, Libero IDE allows users to integrate both schematic and HDL synthesis into a single flow and verify the entire design in a single environment. Libero IDE includes Synplify® for Microsemi from Synplicity®, ViewDraw for Microsemi from Mentor Graphics, ModelSim® HDL Simulator from Mentor Graphics®, WaveFormer Lite™ from SynaptiCAD™, and Designer software from Microsemi. Refer to the *Libero IDE flow* (located on Microsemi SoC Product Group's website) diagram for more information.

2.5 V LVCMOS2 Electrical Specifications

Symbol	Parameter		Commercial Min.	Commercial Max.	Industrial Min.	Industrial Max.	Units
VOH	VCCI = MIN, VI = VIH or VIL	(IOH = –100 mA)	2.1		2.1		V
	VCCI = MIN, VI = VIH or VIL	(IOH = –1 mA)	2.0		2.0		V
	VCCI = MIN, VI = VIH or VIL	(IOH = –2 mA)	1.7		1.7		V
VOL	VCCI = MIN, VI = VIH or VIL	(IOL = 100 mA)		0.2		0.2	V
	VCCI = MIN, VI = VIH or VIL	(IOL = 1mA)		0.4		0.4	V
	VCCI = MIN,VI = VIH or VIL	(IOL = 2 mA)		0.7		0.7	V
VIL	Input Low Voltage, VOUT ≤ VOL (max.)		–0.3	0.7	-0.3	0.7	V
VIH	Input High Voltage, VOUT ≥ VOH (min.)		1.7	VCCI + 0.3	1.7	VCCI + 0.3	V
IIL/ IIH	Input Leakage Current, VIN = VCCI or GND		–10	10	–10	10	μA
IOZ	3-State Output Leakage Current, VOUT = VCCI or GND		–10	10	–10	10	μA
t_R, $t_{F1,2}$	Input Transition Time			10		10	ns
C_{IO}	I/O Capacitance			10		10	pF
ICC[3,4]	Standby Current			1.0		3.0	mA
IV Curve	Can be derived from the IBIS model at www.microsemi.com/soc/custsup/models/ibis.html.						

Notes:

1. t_R is the transition time from 0.7 V to 1.7 V.
2. t_F is the transition time from 1.7 V to 0.7 V.
3. I_{CC} max Commercial –F = 5.0 mA
4. $I_{CC} = I_{CCI} + I_{CCA}$

3.3 V LVTTL Electrical Specifications

Symbol	Parameter		Commercial		Industrial		Units
			Min.	Max.	Min.	Max.	
VOH	VCCI = MIN, VI = VIH or VIL	(IOH = –8 mA)	2.4		2.4		V
VOL	VCCI = MIN, VI = VIH or VIL	(IOL = 12 mA)		0.4		0.4	V
VIL	Input Low Voltage			0.8		0.8	V
VIH	Input High Voltage		2.0	VCCI +0.5	2.0	VCCI +0.5	V
IIL/ IIH	Input Leakage Current, VIN = VCCI or GND		–10	10	–10	10	µA
IOZ	3-State Output Leakage Current, VOUT = VCCI or GND		–10	10	–10	10	µA
t_R, $t_{F1,2}$	Input Transition Time			10		10	ns
C_{IO}	I/O Capacitance			10		10	pF
$ICC^{3,4}$	Standby Current			1.5		10	mA
IV Curve	Can be derived from the IBIS model at www.microsemi.com/soc/custsup/models/ibis.html.						

Notes:

1. t_R is the transition time from 0.8 V to 2.0 V.
2. t_F is the transition time from 2.0 V to 0.8 V.
3. ICC max Commercial –F = 5.0 mA
4. ICC = ICCI + ICCA
5. JTAG pins comply with LVTTL/TTL I/O specification regardless of whether they are used as a user I/O or a JTAG I/O.

5.0 V TTL Electrical Specifications

Symbol	Parameter		Commercial		Industrial		Units
			Min.	Max.	Min.	Max.	
VOH	VCCI = MIN, VI = VIH or VIL	(IOH = –8 mA)	2.4		2.4		V
VOL	VCCI = MIN, VI = VIH or VIL	(IOL= 12 mA)		0.4		0.4	V
VIL	Input Low Voltage			0.8		0.8	V
VIH	Input High Voltage		2.0	VCCI +0.5	2.0	VCCI +0.5	V
IIL/ IIH	Input Leakage Current, VIN = VCCI or GND		–10	10	–10	10	µA
IOZ	3-State Output Leakage Current, VOUT = VCCI or GND		–10	10	–10	10	µA
t_R, $t_{F1,2}$	Input Transition Time			10		10	ns
C_{IO}	I/O Capacitance			10		10	pF
$ICC^{3,4}$	Standby Current			15		20	mA
IV Curve	Can be derived from the IBIS model at www.microsemi.com/soc/custsup/models/ibis.html.						

Note:

1. t_R is the transition time from 0.8 V to 2.0 V.
2. t_F is the transition time from 2.0 V to 0.8 V.
3. ICC max Commercial –F=20mA
4. ICC = ICCI + ICCA
5. JTAG pins comply with LVTTL/TTL I/O specification regardless of whether they are used as a user I/O or a JTAG I/O.

Thermal Characteristics

The temperature variable in the Designer software refers to the junction temperature, not the ambient temperature. This is an important distinction because the heat generated from dynamic power consumption is usually hotter than the ambient temperature. EQ 1, shown below, can be used to calculate junction temperature.

EQ 1

Junction Temperature = $\Delta T + T_a(1)$

Where:

T_a = Ambient Temperature

ΔT = Temperature gradient between junction (silicon) and ambient = θ_{ja} * P

P = Power

θ_{ja} = Junction to ambient of package. θ_{ja} numbers are located in the "Package Thermal Characteristics" section below.

Package Thermal Characteristics

The device junction-to-case thermal characteristic is θ_{jc}, and the junction-to-ambient air characteristic is θ_{ja}. The thermal characteristics for θ_{ja} are shown with two different air flow rates. θ_{jc} is provided for reference. The maximum junction temperature is 150°C.

The maximum power dissipation allowed for eX devices is a function of θ_{ja}. A sample calculation of the absolute maximum power dissipation allowed for a TQFP 100-pin package at commercial temperature and still air is as follows:

$$\text{Maximum Power Allowed} = \frac{\text{Max. junction temp. } (°C) - \text{Max. ambient temp. } (°C)}{\theta_{ja}(°C/W)} = \frac{150°C - 70°C}{33.5°C/W} = 2.39W$$

Package Type	Pin Count	θ_{jc}	θ_{ja}			Units
			Still Air	1.0 m/s 200 ft/min	2.5 m/s 500 ft/min	
Thin Quad Flat Pack (TQFP)	64	12.0	42.4	36.3	34.0	°C/W
Thin Quad Flat Pack (TQFP)	100	14.0	33.5	27.4	25.0	°C/W
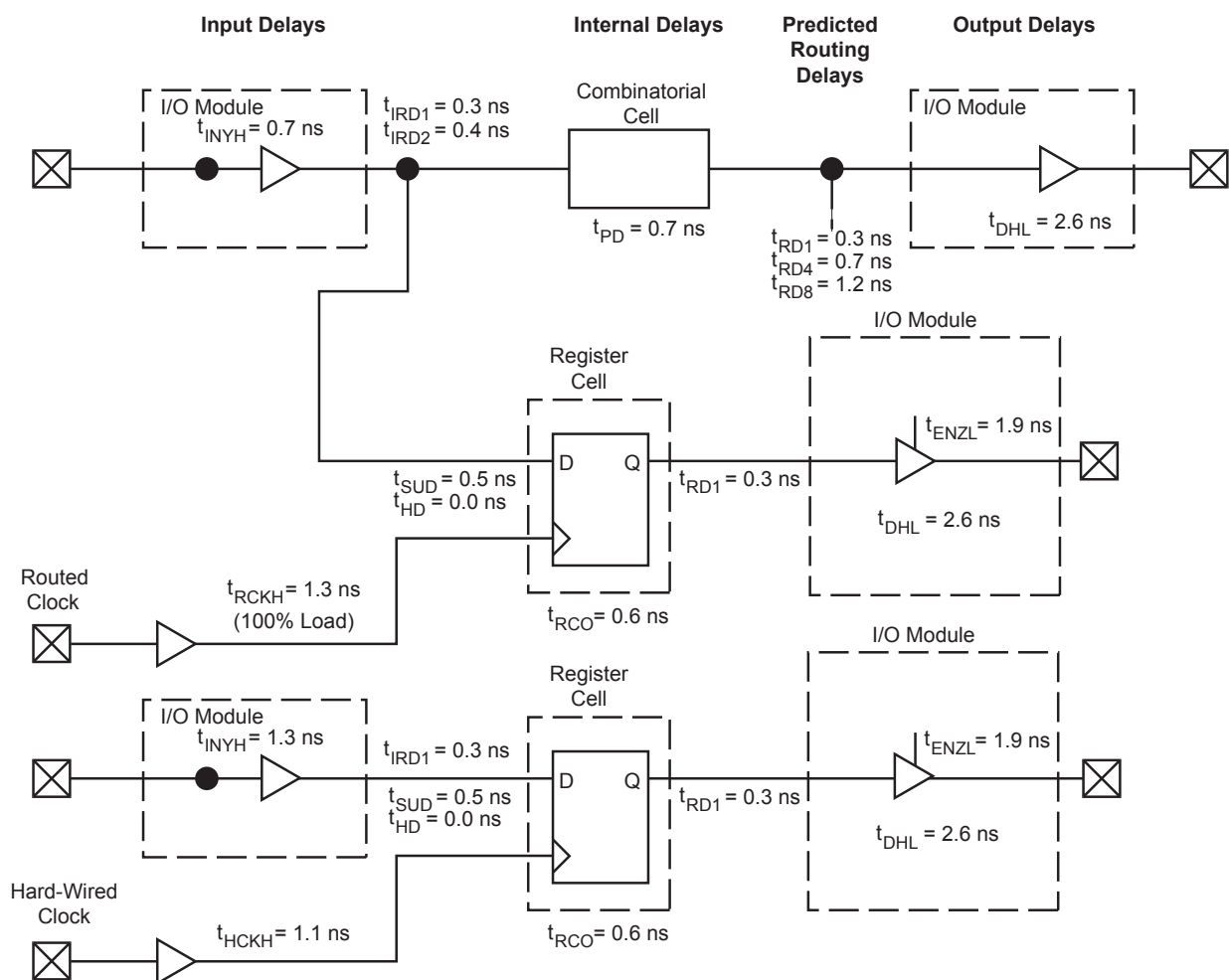
eX Timing Model

Note: *Values shown for eX128–P, worst-case commercial conditions (5.0 V, 35 pF Pad Load).*

*Figure 1-14 • **eX Timing Model***

Hardwired Clock

External Setup = $t_{INYH} + t_{IRD1} + t_{SUD} - t_{HCKH}$

    = 0.7 + 0.3 + 0.5 − 1.1 = 0.4 ns

Clock-to-Out (Pad-to-Pad), typical

    = $t_{HCKH} + t_{RCO} + t_{RD1} + t_{DHL}$

    = 1.1 + 0.6 + 0.3 + 2.6 = 4.6 ns

Routed Clock

External Setup = $t_{INYH} + t_{IRD2} + t_{SUD} - t_{RCKH}$

    = 0.7 + 0.4 + 0.5 − 1.3= 0.3 ns

Clock-to-Out (Pad-to-Pad), typical

    = $t_{RCKH} + t_{RCO} + t_{RD1} + t_{DHL}$
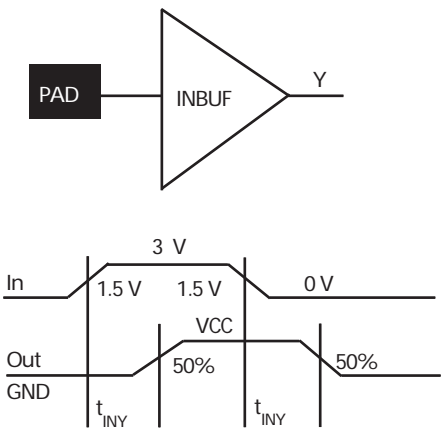
    = 1.3+ 0.6 + 0.3 + 2.6 = 4.8 ns

Input Buffer Delays

Table 1-14 • **Input Buffer Delays**
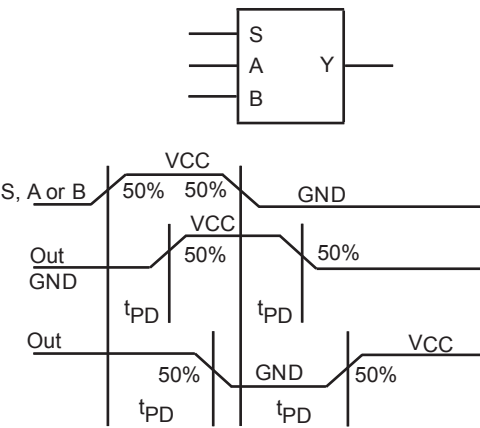
C-Cell Delays

Table 1-15 • **C-Cell Delays**

Timing Characteristics

Timing characteristics for eX devices fall into three categories: family-dependent, device-dependent, and design-dependent. The input and output buffer characteristics are common to all eX family members. Internal routing delays are device-dependent. Design dependency means actual delays are not determined until after placement and routing of the user's design are complete. Delay values may then be determined by using the Timer utility or performing simulation with post-layout delays.

Critical Nets and Typical Nets

Propagation delays are expressed only for typical nets, which are used for initial design performance evaluation. Critical net delays can then be applied to the most timing critical paths. Critical nets are determined by net property assignment prior to placement and routing. Up to six percent of the nets in a design may be designated as critical.

Long Tracks

Some nets in the design use long tracks. Long tracks are special routing resources that span multiple rows, columns, or modules. Long tracks employ three to five antifuse connections. This increases capacitance and resistance, resulting in longer net delays for macros connected to long tracks. Typically, no more than six percent of nets in a fully utilized device require long tracks. Long tracks contribute approximately 4 ns to 8.4 ns delay. This additional delay is represented statistically in higher fanout routing delays.

Timing Derating

eX devices are manufactured with a CMOS process. Therefore, device performance varies according to temperature, voltage, and process changes. Minimum timing parameters reflect maximum operating voltage, minimum operating temperature, and best-case processing. Maximum timing parameters reflect minimum operating voltage, maximum operating temperature, and worst-case processing.

Temperature and Voltage Derating Factors

Table 1-16 • **Temperature and Voltage Derating Factors
(Normalized to Worst-Case Commercial, T_J = 70°C, VCCA = 2.3V)**

VCCA	Junction Temperature (T_J)						
	−55	**−40**	**0**	**25**	**70**	**85**	**125**
2.3	0.79	0.80	0.87	0.88	1.00	1.04	1.13
2.5	0.74	0.74	0.81	0.83	0.93	0.97	1.06
2.7	0.69	0.70	0.76	0.78	0.88	0.91	1.00

Table 1-20 • **eX Family Timing Characteristics**
       (Worst-Case Commercial Conditions VCCA = 2.3 V, T$_J$ = 70°C)

Parameter	Description	–P Speed Min.	–P Speed Max.	Std Speed Min.	Std Speed Max.	–F Speed Min.	–F Speed Max.	Units
2.5 V LVCMOS Output Module Timing[1] (VCCI = 2.3 V)								
t$_{DLH}$	Data-to-Pad LOW to HIGH		3.3		4.7		6.6	ns
t$_{DHL}$	Data-to-Pad HIGH to LOW		3.5		5.0		7.0	ns
t$_{DHLS}$	Data-to-Pad HIGH to LOW—Low Slew		11.6		16.6		23.2	ns
t$_{ENZL}$	Enable-to-Pad, Z to L		2.5		3.6		5.1	ns
t$_{ENZLS}$	Enable-to-Pad Z to L—Low Slew		11.8		16.9		23.7	ns
t$_{ENZH}$	Enable-to-Pad, Z to H		3.4		4.9		6.9	ns
t$_{ENLZ}$	Enable-to-Pad, L to Z		2.1		3.0		4.2	ns
t$_{ENHZ}$	Enable-to-Pad, H to Z		2.4		5.67		7.94	ns
d$_{TLH}$	Delta Delay vs. Load LOW to HIGH		0.034		0.046		0.066	ns/pF
d$_{THL}$	Delta Delay vs. Load HIGH to LOW		0.016		0.022		0.05	ns/pF
d$_{THLS}$	Delta Delay vs. Load HIGH to LOW—Low Slew		0.05		0.072		0.1	ns/pF
3.3 V LVTTL Output Module Timing[1] (VCCI = 3.0 V)								
t$_{DLH}$	Data-to-Pad LOW to HIGH		2.8		4.0		5.6	ns
t$_{DHL}$	Data-to-Pad HIGH to LOW		2.7		3.9		5.4	ns
t$_{DHLS}$	Data-to-Pad HIGH to LOW—Low Slew		9.7		13.9		19.5	ns
t$_{ENZL}$	Enable-to-Pad, Z to L		2.2		3.2		4.4	ns
t$_{ENZLS}$	Enable-to-Pad Z to L—Low Slew		9.7		13.9		19.6	ns
t$_{ENZH}$	Enable-to-Pad, Z to H		2.8		4.0		5.6	ns
t$_{ENLZ}$	Enable-to-Pad, L to Z		2.8		4.0		5.6	ns
t$_{ENHZ}$	Enable-to-Pad, H to Z		2.6		3.8		5.3	ns
d$_{TLH}$	Delta Delay vs. Load LOW to HIGH		0.02		0.03		0.046	ns/pF
d$_{THL}$	Delta Delay vs. Load HIGH to LOW		0.016		0.022		0.05	ns/pF
d$_{THLS}$	Delta Delay vs. Load HIGH to LOW—Low Slew		0.05		0.072		0.1	ns/pF
5.0 V TTL Output Module Timing* (VCCI = 4.75 V)								
t$_{DLH}$	Data-to-Pad LOW to HIGH		2.0		2.9		4.0	ns
t$_{DHL}$	Data-to-Pad HIGH to LOW		2.6		3.7		5.2	ns
t$_{DHLS}$	Data-to-Pad HIGH to LOW—Low Slew		6.8		9.7		13.6	ns
t$_{ENZL}$	Enable-to-Pad, Z to L		1.9		2.7		3.8	ns
t$_{ENZLS}$	Enable-to-Pad Z to L—Low Slew		6.8		9.8		13.7	ns
t$_{ENZH}$	Enable-to-Pad, Z to H		2.1		3.0		4.1	ns
t$_{ENLZ}$	Enable-to-Pad, L to Z		3.3		4.8		6.6	ns

*Note: *Delays based on 35 pF loading.*

Pin Description

CLKA/B   **Routed Clock A and B**

These pins are clock inputs for clock distribution networks. Input levels are compatible with standard TTL or LVTTL specifications. The clock input is buffered prior to clocking the R-cells. If not used, this pin must be set LOW or HIGH on the board. It must not be left floating.

GND   **Ground**

LOW supply voltage.

HCLK   **Dedicated (Hardwired)**
          Array Clock

This pin is the clock input for sequential modules. Input levels are compatible with standard TTL or LVTTL specifications. This input is directly wired to each R-cell and offers clock speeds independent of the number of R-cells being driven. If not used, this pin must be set LOW or HIGH on the board. It must not be left floating.

I/O   **Input/Output**

The I/O pin functions as an input, output, tristate, or bidirectional buffer. Based on certain configurations, input and output levels are compatible with standard TTL or LVTTL specifications. Unused I/O pins are automatically tristated by the Designer software.

LP   **Low Power Pin**

Controls the low power mode of the eX devices. The device is placed in the low power mode by connecting the LP pin to logic HIGH. In low power mode, all I/Os are tristated, all input buffers are turned OFF, and the core of the device is turned OFF. To exit the low power mode, the LP pin must be set LOW. The device enters the low power mode 800 ns after the LP pin is driven to a logic HIGH. It will resume normal operation 200 μs after the LP pin is driven to a logic LOW. LP pin should not be left floating. Under normal operating condition it should be tied to GND via 10 kΩ resistor.

NC   **No Connection**

This pin is not connected to circuitry within the device. These pins can be driven to any voltage or can be left floating with no effect on the operation of the device.

PRA/PRB, I/O   **Probe A/B**

The Probe pin is used to output data from any user-defined design node within the device. This diagnostic pin can be used independently or in conjunction with the other probe pin to allow real-time diagnostic output of any signal path within the device. The Probe pin can be used as a user-defined I/O when verification has been completed. The pin's probe capabilities can be permanently disabled to protect programmed design confidentiality.

TCK, I/O   **Test Clock**

Test clock input for diagnostic probe and device programming. In flexible mode, TCK becomes active when the TMS pin is set LOW (refer to Table 1-4 on page 1-10). This pin functions as an I/O when the boundary scan state machine reaches the "logic reset" state.

TDI, I/O   **Test Data Input**

Serial input for boundary scan testing and diagnostic probe. In flexible mode, TDI is active when the TMS pin is set LOW (refer to Table 1-4 on page 1-10). This pin functions as an I/O when the boundary scan state machine reaches the "logic reset" state.

TDO, I/O   **Test Data Output**

Serial output for boundary scan testing. In flexible mode, TDO is active when the TMS pin is set LOW (refer to Table 1-4 on page 1-10). This pin functions as an I/O when the boundary scan state machine reaches the "logic reset" state. When Silicon Explorer is being used, TDO will act as an output when the "checksum" command is run. It will return to user I/O when "checksum" is complete.

TQ64			TQ64		
Pin Number	eX64 Function	eX128 Function	Pin Number	eX64 Function	eX128 Function
1	GND	GND	33	GND	GND
2	TDI, I/O	TDI, I/O	34	I/O	I/O
3	I/O	I/O	35	I/O	I/O
4	TMS	TMS	36	VCCA	VCCA
5	GND	GND	37	VCCI	VCCI
6	VCCI	VCCI	38	I/O	I/O
7	I/O	I/O	39	I/O	I/O
8	I/O	I/O	40	NC	I/O
9	NC	I/O	41	NC	I/O
10	NC	I/O	42	I/O	I/O
11	TRST, I/O	TRST, I/O	43	I/O	I/O
12	I/O	I/O	44	VCCA	VCCA
13	NC	I/O	45*	GND/LP	GND/ LP
14	GND	GND	46	GND	GND
15	I/O	I/O	47	I/O	I/O
16	I/O	I/O	48	I/O	I/O
17	I/O	I/O	49	I/O	I/O
18	I/O	I/O	50	I/O	I/O
19	VCCI	VCCI	51	I/O	I/O
20	I/O	I/O	52	VCCI	VCCI
21	PRB, I/O	PRB, I/O	53	I/O	I/O
22	VCCA	VCCA	54	I/O	I/O
23	GND	GND	55	CLKA	CLKA
24	I/O	I/O	56	CLKB	CLKB
25	HCLK	HCLK	57	VCCA	VCCA
26	I/O	I/O	58	GND	GND
27	I/O	I/O	59	PRA, I/O	PRA, I/O
28	I/O	I/O	60	I/O	I/O
29	I/O	I/O	61	VCCI	VCCI
30	I/O	I/O	62	I/O	I/O
31	I/O	I/O	63	I/O	I/O
32	TDO, I/O	TDO, I/O	64	TCK, I/O	TCK, I/O

*Note: *Please read the LP pin descriptions for restrictions on their use.*

TQ100			
Pin Number	eX64 Function	eX128 Function	eX256 Function
71	I/O	I/O	I/O
72	NC	I/O	I/O
73	NC	NC	I/O
74	NC	NC	I/O
75	NC	NC	I/O
76	NC	I/O	I/O
77	I/O	I/O	I/O
78	I/O	I/O	I/O
79	I/O	I/O	I/O
80	I/O	I/O	I/O
81	I/O	I/O	I/O
82	VCCI	VCCI	VCCI
83	I/O	I/O	I/O
84	I/O	I/O	I/O
85	I/O	I/O	I/O
86	I/O	I/O	I/O
87	CLKA	CLKA	CLKA
88	CLKB	CLKB	CLKB
89	NC	NC	NC
90	VCCA	VCCA	VCCA
91	GND	GND	GND
92	PRA, I/O	PRA, I/O	PRA, I/O
93	I/O	I/O	I/O
94	I/O	I/O	I/O
95	I/O	I/O	I/O
96	I/O	I/O	I/O
97	I/O	I/O	I/O
98	I/O	I/O	I/O
99	I/O	I/O	I/O
100	TCK, I/O	TCK, I/O	TCK, I/O

*Note: *Please read the LP pin descriptions for restrictions on their use.*

3 – Datasheet Information

List of Changes

The following table lists critical changes that were made in the current version of the document.

Revision	Changes	Page
Revision 10 (October 2012)	The "User Security" section was revised to clarify that although no existing security measures can give an absolute guarantee, Microsemi FPGAs implement industry standard security (SAR 34677).	1-5
	Package names used in the "Product Profile" section and "Package Pin Assignments" section were revised to match standards given in *Package Mechanical Drawings* (SAR 34779).	I 2-1
Revision 9 (June 2011)	The versioning system for datasheets has been changed. Datasheets are assigned a revision number that increments each time the datasheet is revised. The "eX Device Status" table indicates the status for each device in the device family.	II
	The Chip Scale packages (CS49, CS128, CS181) are no longer offered for eX devices. They have been removed from the product family information. Pin tables for CSP packages have been removed from the datasheet (SAR 32002).	N/A
Revision 8 (v4.3, June 2006)	The "Ordering Information" was updated with RoHS information. The TQFP measurement was also updated.	II
	The "Dedicated Test Mode" was updated.	1-10
	Note 5 was added to the "3.3 V LVTTL Electrical Specifications" and "5.0 V TTL Electrical Specifications" tables	1-18
	The "LP Low Power Pin" description was updated.	1-31
Revision 7 (v4.2, June 2004)	The "eX Timing Model" was updated.	1-22
v4.1	The "Development Tool Support" section was updated.	1-13
	The "Package Thermal Characteristics" section was updated.	1-21
v4.0	The "Product Profile" section was updated.	1-I
	The "Ordering Information" section was updated.	1-II
	The "Temperature Grade Offerings" section is new.	1-III
	The "Speed Grade and Temperature Grade Matrix" section is new.	1-III
	The "eX FPGA Architecture and Characteristics" section was updated.	1-1
	The "Clock Resources" section was updated.	1-3
	Table 1-1 •Connections of Routed Clock Networks, CLKA and CLKB is new.	1-4
	The "User Security" section was updated.	1-5
	The "I/O Modules" section was updated.	1-5
	The "Hot-Swapping" section was updated.	1-6
	The "Power Requirements" section was updated.	1-6
	The "Low Power Mode" section was updated.	1-6
	The "Boundary Scan Testing (BST)" section was updated.	1-10
	The "Dedicated Test Mode" section was updated.	1-10

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5172154-10/10.12