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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

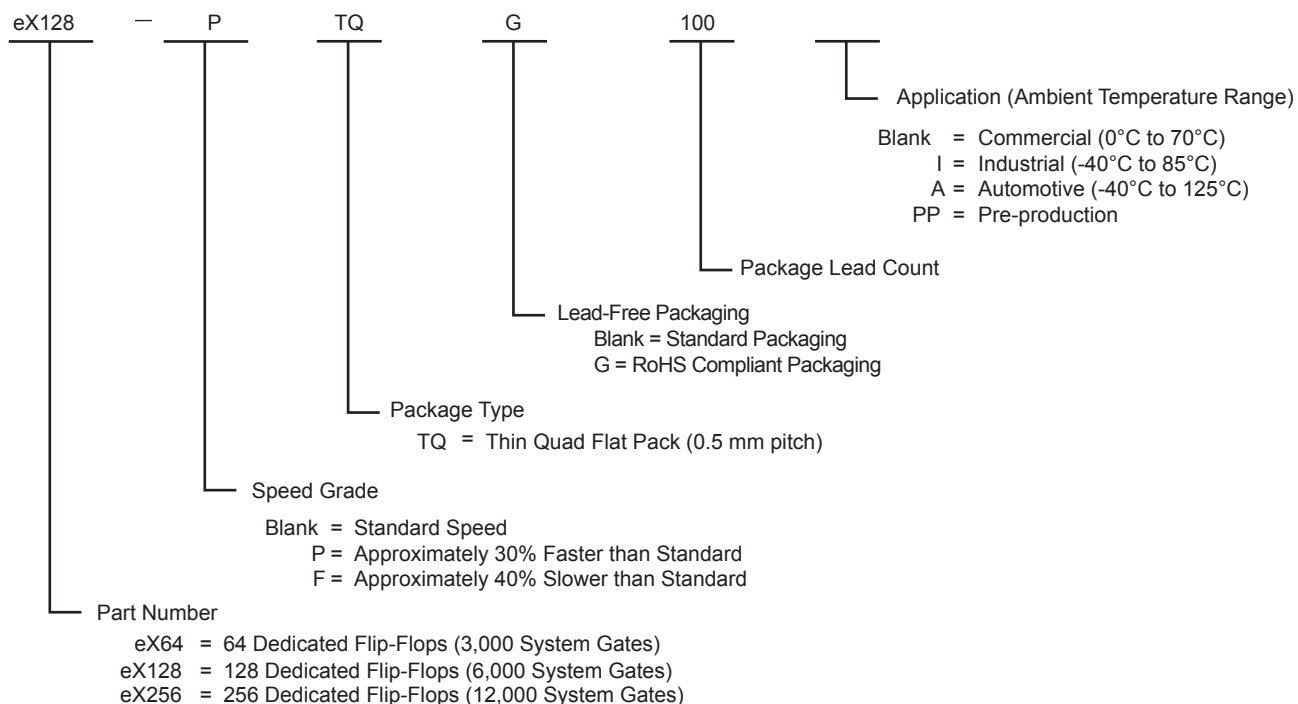
Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	128
Total RAM Bits	-
Number of I/O	56
Number of Gates	3000
Voltage - Supply	2.3V ~ 2.7V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	100-LQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microsemi/ex64-tqg100

Ordering Information



eX Device Status

eX Devices	Status
eX64	Production
eX128	Production
eX256	Production

Plastic Device Resources

Device	User I/Os (Including Clock Buffers)	
	TQ64	TQ100
eX64	41	56
eX128	46	70
eX256	—	81

Note: TQ = Thin Quad Flat Pack

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Module Organization

C-cell and R-cell logic modules are arranged into horizontal banks called Clusters, each of which contains two C-cells and one R-cell in a C-R-C configuration.

Clusters are further organized into modules called SuperClusters for improved design efficiency and device performance, as shown in Figure 1-3. Each SuperCluster is a two-wide grouping of Clusters.

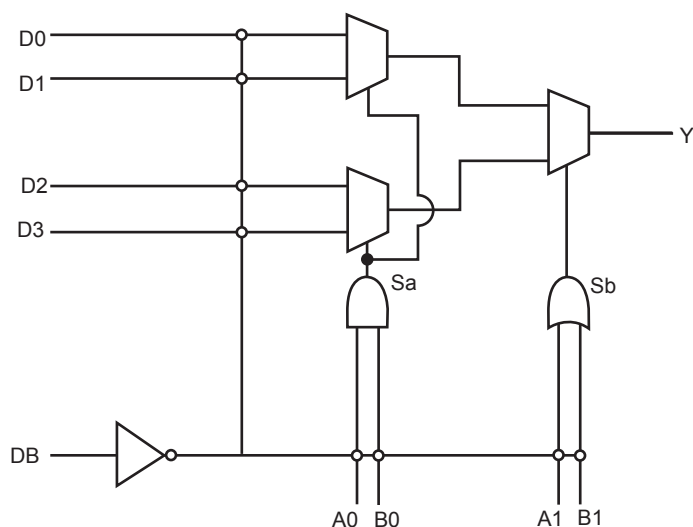


Figure 1-2 • C-Cell

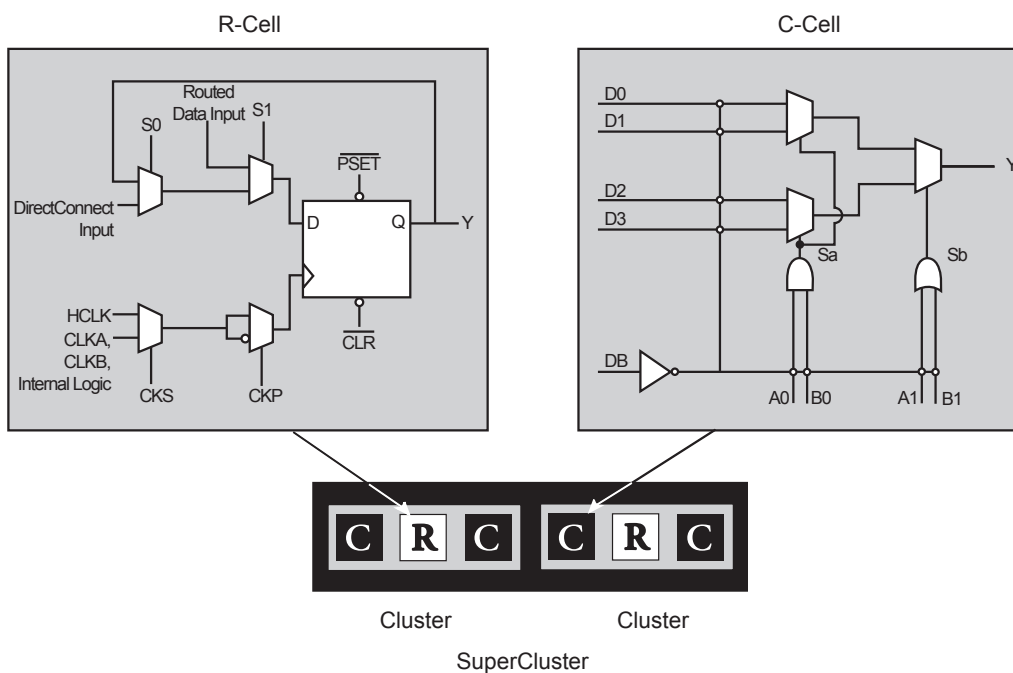


Figure 1-3 • Cluster Organization

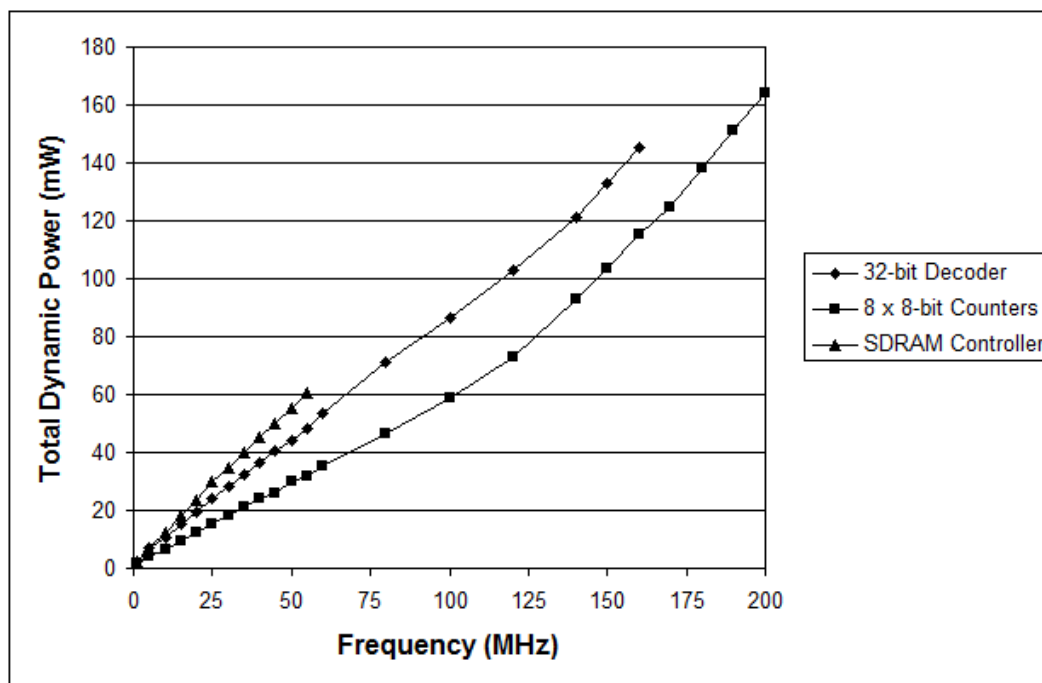


Figure 1-10 • Total Dynamic Power (mW)

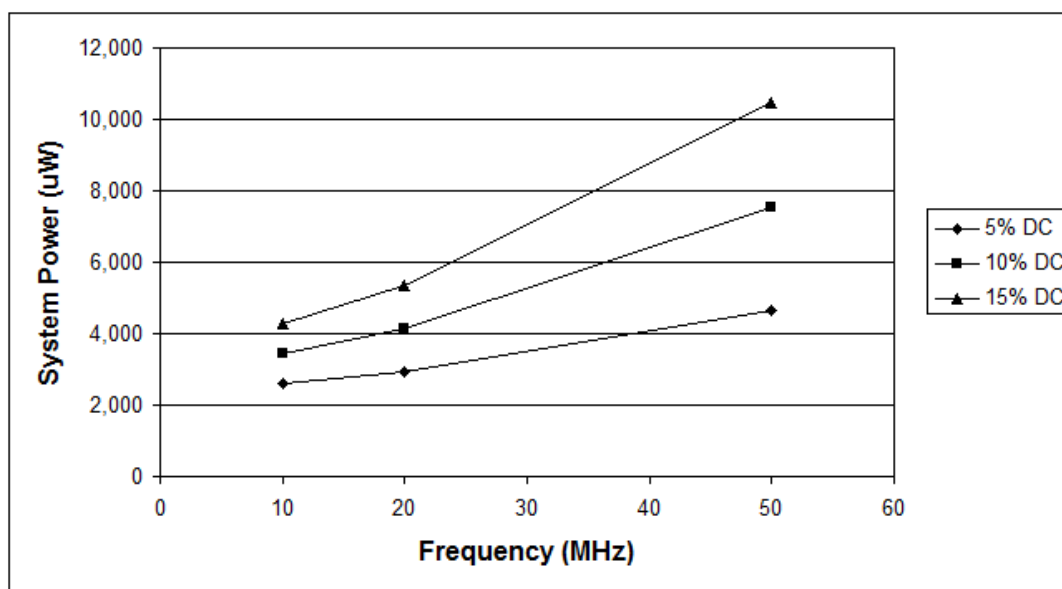


Figure 1-11 • System Power at 5%, 10%, and 15% Duty Cycle

Programming

Device programming is supported through Silicon Sculptor series of programmers. In particular, Silicon Sculptor II is a compact, robust, single-site and multi-site device programmer for the PC.

With standalone software, Silicon Sculptor II allows concurrent programming of multiple units from the same PC, ensuring the fastest programming times possible. Each fuse is subsequently verified by Silicon Sculptor II to insure correct programming. In addition, integrity tests ensure that no extra fuses are programmed. Silicon Sculptor II also provides extensive hardware self-testing capability.

The procedure for programming an eX device using Silicon Sculptor II is as follows:

1. Load the *.AFM file
2. Select the device to be programmed
3. Begin programming

When the design is ready to go to production, Microsemi offers device volume-programming services either through distribution partners or via in-house programming from the factory.

For more details on programming eX devices, please refer to the [Programming Antifuse Devices](#) application note and the [Silicon Sculptor II User's Guide](#).

Probing Capabilities

eX devices provide internal probing capability that is accessed with the JTAG pins. The Silicon Explorer II Diagnostic hardware is used to control the TDI, TCK, TMS and TDO pins to select the desired nets for debugging. The user simply assigns the selected internal nets in the Silicon Explorer II software to the PRA/PRB output pins for observation. Probing functionality is activated when the BST pins are in JTAG mode and the TRST pin is driven HIGH or left floating. If the TRST pin is held LOW, the TAP controller will remain in the Test-Logic-Reset state so no probing can be performed. The Silicon Explorer II automatically places the device into JTAG mode, but the user must drive the TRST pin HIGH or allow the internal pull-up resistor to pull TRST HIGH.

When you select the **Reserve Probe Pin** box, as shown in [Figure 1-12 on page 1-10](#), the layout tool reserves the PRA and PRB pins as dedicated outputs for probing. This reserve option is merely a guideline. If the Layout tool requires that the PRA and PRB pins be user I/Os to achieve successful layout, the tool will use these pins for user I/Os. If you assign user I/Os to the PRA and PRB pins and select the **Reserve Probe Pin** option, Designer Layout will override the "Reserve Probe Pin" option and place your user I/Os on those pins.

To allow for probing capabilities, the security fuse must not be programmed. Programming the security fuse will disable the probe circuitry. [Table 1-8 on page 1-13](#) summarizes the possible device configurations for probing once the device leaves the Test-Logic-Reset JTAG state.

Silicon Explorer II Probe

Silicon Explorer II is an integrated hardware and software solution that, in conjunction with Microsemi Designer software tools, allow users to examine any of the internal nets of the device while it is operating in a prototype or a production system. The user can probe into an eX device via the PRA and PRB pins without changing the placement and routing of the design and without using any additional resources. Silicon Explorer II's noninvasive method does not alter timing or loading effects, thus shortening the debug cycle.

Silicon Explorer II does not require re-layout or additional MUXes to bring signals out to an external pin, which is necessary when using programmable logic devices from other suppliers.

Silicon Explorer II samples data at 100 MHz (asynchronous) or 66 MHz (synchronous). Silicon Explorer II attaches to a PC's standard COM port, turning the PC into a fully functional 18-channel logic analyzer. Silicon Explorer II allows designers to complete the design verification process at their desks and reduces verification time from several hours per cycle to a few seconds.

The Silicon Explorer II tool uses the boundary scan ports (TDI, TCK, TMS and TDO) to select the desired nets for verification. The selected internal nets are assigned to the PRA/PRB pins for observation. [Figure 1-13 on page 1-13](#) illustrates the interconnection between Silicon Explorer II and the eX device to perform in-circuit verification.

Designer software is a place-and-route tool and provides a comprehensive suite of backend support tools for FPGA development. The Designer software includes timing-driven place-and-route, and a world-class integrated static timing analyzer and constraints editor. With the Designer software, a user can lock his/her design pins before layout while minimally impacting the results of place-and-route. Additionally, the back-annotation flow is compatible with all the major simulators and the simulation results can be cross-probed with Silicon Explorer II, Microsemi integrated verification and logic analysis tool. Another tool included in the Designer software is the SmartGen core generator, which easily creates popular and commonly used logic functions for implementation into your schematic or HDL design. Microsemi's Designer software is compatible with the most popular FPGA design entry and verification tools from companies such as Mentor Graphics, Synplicity, Synopsys, and Cadence Design Systems. The Designer software is available for both the Windows and UNIX operating systems.

3.3 V LVTTTL Electrical Specifications

Symbol	Parameter		Commercial		Industrial		Units
			Min.	Max.	Min.	Max.	
VOH	VCCI = MIN, VI = VIH or VIL	(IOH = -8 mA)	2.4		2.4		V
VOL	VCCI = MIN, VI = VIH or VIL	(IOL = 12 mA)		0.4		0.4	V
VIL	Input Low Voltage			0.8		0.8	V
VIH	Input High Voltage		2.0	VCCI +0.5	2.0	VCCI +0.5	V
IIL/ IIH	Input Leakage Current, VIN = VCCI or GND		-10	10	-10	10	μA
IOZ	3-State Output Leakage Current, VOUT = VCCI or GND		-10	10	-10	10	μA
t _R , t _{F1,2}	Input Transition Time			10		10	ns
C _{IO}	I/O Capacitance			10		10	pF
ICC ^{3,4}	Standby Current			1.5		10	mA
IV Curve	Can be derived from the IBIS model at www.microsemi.com/soc/custsup/models/ibis.html .						

Notes:

1. t_R is the transition time from 0.8 V to 2.0 V.
2. t_F is the transition time from 2.0 V to 0.8 V.
3. ICC max Commercial -F = 5.0 mA
4. ICC = ICCI + ICCA
5. JTAG pins comply with LVTTTL/TTL I/O specification regardless of whether they are used as a user I/O or a JTAG I/O.

5.0 V TTL Electrical Specifications

Symbol	Parameter		Commercial		Industrial		Units
			Min.	Max.	Min.	Max.	
VOH	VCCI = MIN, VI = VIH or VIL	(IOH = -8 mA)	2.4		2.4		V
VOL	VCCI = MIN, VI = VIH or VIL	(IOL = 12 mA)		0.4		0.4	V
VIL	Input Low Voltage			0.8		0.8	V
VIH	Input High Voltage		2.0	VCCI +0.5	2.0	VCCI +0.5	V
IIL/ IIH	Input Leakage Current, VIN = VCCI or GND		-10	10	-10	10	μA
IOZ	3-State Output Leakage Current, VOUT = VCCI or GND		-10	10	-10	10	μA
t _R , t _{F1,2}	Input Transition Time			10		10	ns
C _{IO}	I/O Capacitance			10		10	pF
ICC ^{3,4}	Standby Current			15		20	mA
IV Curve	Can be derived from the IBIS model at www.microsemi.com/soc/custsup/models/ibis.html .						

Note:

1. t_R is the transition time from 0.8 V to 2.0 V.
2. t_F is the transition time from 2.0 V to 0.8 V.
3. ICC max Commercial -F=20mA
4. ICC = ICCI + ICCA
5. JTAG pins comply with LVTTTL/TTL I/O specification regardless of whether they are used as a user I/O or a JTAG I/O.

The estimation of the dynamic power dissipation is a piece-wise linear summation of the power dissipation of each component.

$$\begin{aligned} \text{Dynamic power dissipation} = & V_{CCA}^2 * [(m_c * C_{eqcm} * f_{mC})_{\text{Comb Modules}} + (m_s * C_{eqsm} * f_{mS})_{\text{Seq Modules}} \\ & + (n * C_{eqi} * f_n)_{\text{Input Buffers}} + (0.5 * (q1 * C_{eqcr} * f_{q1}) + (r1 * f_{q1}))_{\text{RCLKA}} + (0.5 * (q2 * C_{eqcr} * f_{q2}) \\ & + (r2 * f_{q2}))_{\text{RCLKB}} + (0.5 * (s1 * C_{eqhv} * f_{s1}) + (C_{eqhf} * f_{s1}))_{\text{HCLK}}] + V_{CCI}^2 * [(p * (C_{eqo} + C_L) \\ & * f_p)_{\text{Output Buffers}}] \end{aligned}$$

where:

- m_c = Number of combinatorial cells switching at frequency f_m , typically 20% of C-cells
- m_s = Number of sequential cells switching at frequency f_m , typically 20% of R-cells
- n = Number of input buffers switching at frequency f_n , typically number of inputs / 4
- p = Number of output buffers switching at frequency f_p , typically number of outputs / 4
- $q1$ = Number of R-cells driven by routed array clock A
- $q2$ = Number of R-cells driven by routed array clock B
- $r1$ = Fixed capacitance due to routed array clock A
- $r2$ = Fixed capacitance due to routed array clock B
- $s1$ = Number of R-cells driven by dedicated array clock
- C_{eqcm} = Equivalent capacitance of combinatorial modules
- C_{eqsm} = Equivalent capacitance of sequential modules
- C_{eqi} = Equivalent capacitance of input buffers
- C_{eqcr} = Equivalent capacitance of routed array clocks
- C_{eqhv} = Variable capacitance of dedicated array clock
- C_{eqhf} = Fixed capacitance of dedicated array clock
- C_{eqo} = Equivalent capacitance of output buffers
- C_L = Average output loading capacitance, typically 10 pF
- f_{mC} = Average C-cell switching frequency, typically $F/10$
- f_{mS} = Average R-cell switching frequency, typically $F/10$
- f_n = Average input buffer switching frequency, typically $F/5$
- f_p = Average output buffer switching frequency, typically $F/5$
- f_{q1} = Frequency of routed clock A
- f_{q2} = Frequency of routed clock B
- f_{s1} = Frequency of dedicated array clock

The eX, SX-A and RTSX-S Power Calculator can be used to estimate the total power dissipation (static and dynamic) of eX devices: www.microsemi.com/soc/techdocs/calculators.aspx.

Thermal Characteristics

The temperature variable in the Designer software refers to the junction temperature, not the ambient temperature. This is an important distinction because the heat generated from dynamic power consumption is usually hotter than the ambient temperature. EQ 1, shown below, can be used to calculate junction temperature.

EQ 1

$$\text{Junction Temperature} = \Delta T + T_a(1)$$

Where:

T_a = Ambient Temperature

ΔT = Temperature gradient between junction (silicon) and ambient = $\theta_{ja} * P$

P = Power

θ_{ja} = Junction to ambient of package. θ_{ja} numbers are located in the "Package Thermal Characteristics" section below.

Package Thermal Characteristics

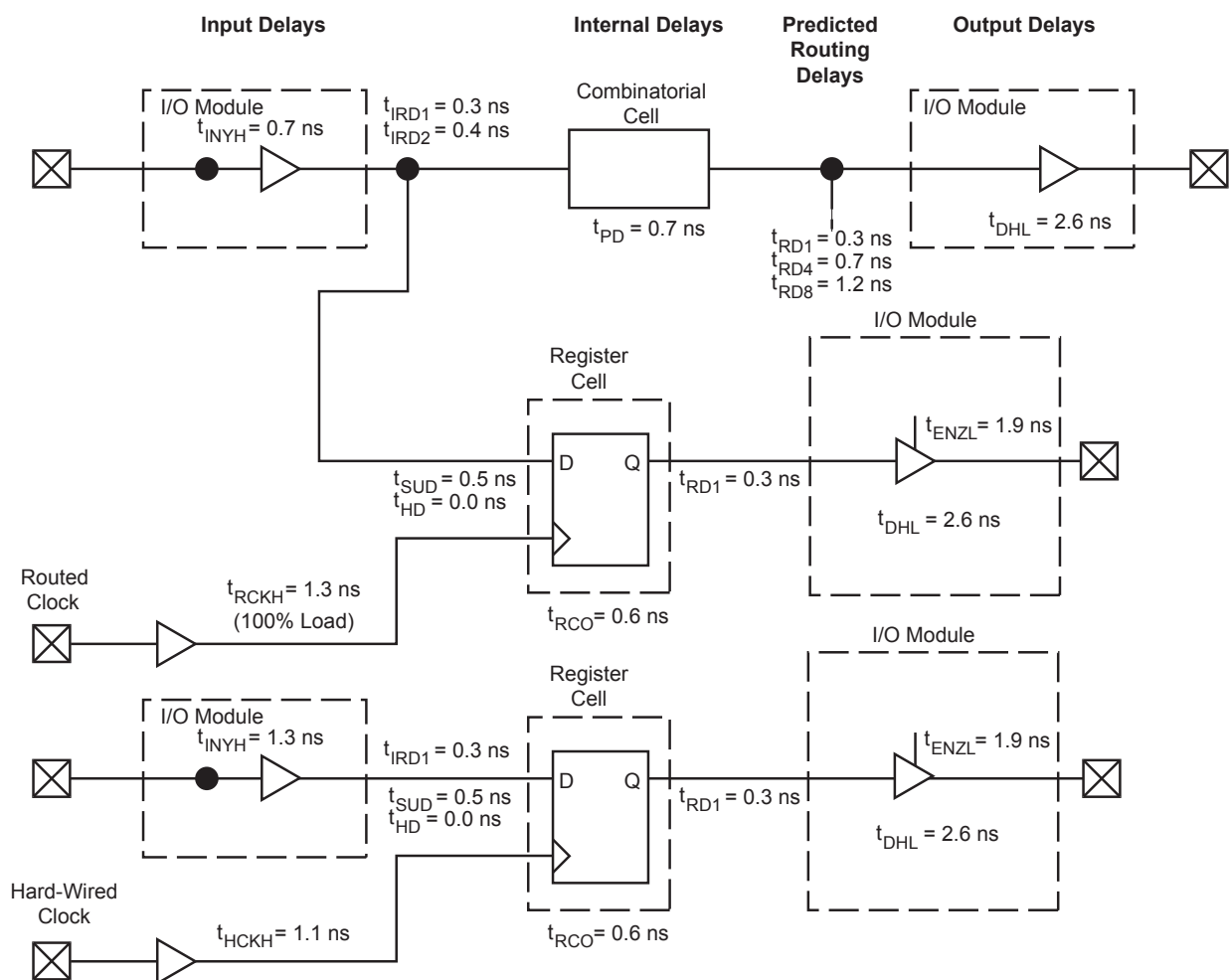
The device junction-to-case thermal characteristic is θ_{jc} , and the junction-to-ambient air characteristic is θ_{ja} . The thermal characteristics for θ_{ja} are shown with two different air flow rates. θ_{jc} is provided for reference. The maximum junction temperature is 150°C.

The maximum power dissipation allowed for eX devices is a function of θ_{ja} . A sample calculation of the absolute maximum power dissipation allowed for a TQFP 100-pin package at commercial temperature and still air is as follows:

$$\text{Maximum Power Allowed} = \frac{\text{Max. junction temp. (}^\circ\text{C)} - \text{Max. ambient temp. (}^\circ\text{C)}}{\theta_{ja} (^\circ\text{C/W)}} = \frac{150^\circ\text{C} - 70^\circ\text{C}}{33.5^\circ\text{C/W}} = 2.39\text{W}$$

Package Type	Pin Count	θ_{jc}	θ_{ja}			Units
			Still Air	1.0 m/s 200 ft/min	2.5 m/s 500 ft/min	
Thin Quad Flat Pack (TQFP)	64	12.0	42.4	36.3	34.0	°C/W
Thin Quad Flat Pack (TQFP)	100	14.0	33.5	27.4	25.0	°C/W

eX Timing Model



Note: Values shown for eX128-P, worst-case commercial conditions (5.0 V, 35 pF Pad Load).

Figure 1-14 • eX Timing Model

Hardwired Clock

$$\text{External Setup} = t_{INYH} + t_{IRD1} + t_{SUD} - t_{HCKH}$$

$$= 0.7 + 0.3 + 0.5 - 1.1 = 0.4 \text{ ns}$$

Clock-to-Out (Pad-to-Pad), typical

$$= t_{HCKH} + t_{RCO} + t_{RD1} + t_{DHL}$$

$$= 1.1 + 0.6 + 0.3 + 2.6 = 4.6 \text{ ns}$$

Routed Clock

$$\text{External Setup} = t_{INYH} + t_{IRD2} + t_{SUD} - t_{RCKH}$$

$$= 0.7 + 0.4 + 0.5 - 1.3 = 0.3 \text{ ns}$$

Clock-to-Out (Pad-to-Pad), typical

$$= t_{RCKH} + t_{RCO} + t_{RD1} + t_{DHL}$$

$$= 1.3 + 0.6 + 0.3 + 2.6 = 4.8 \text{ ns}$$

Output Buffer Delays

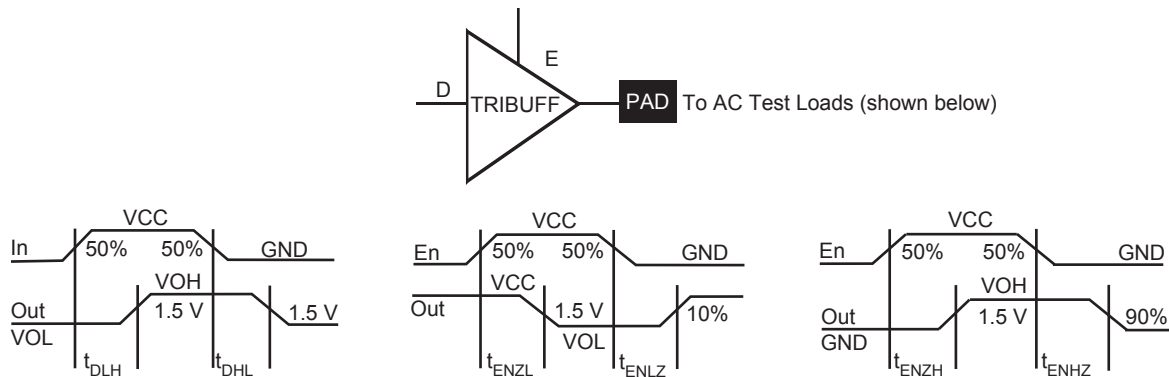


Table 1-13 • Output Buffer Delays

AC Test Loads

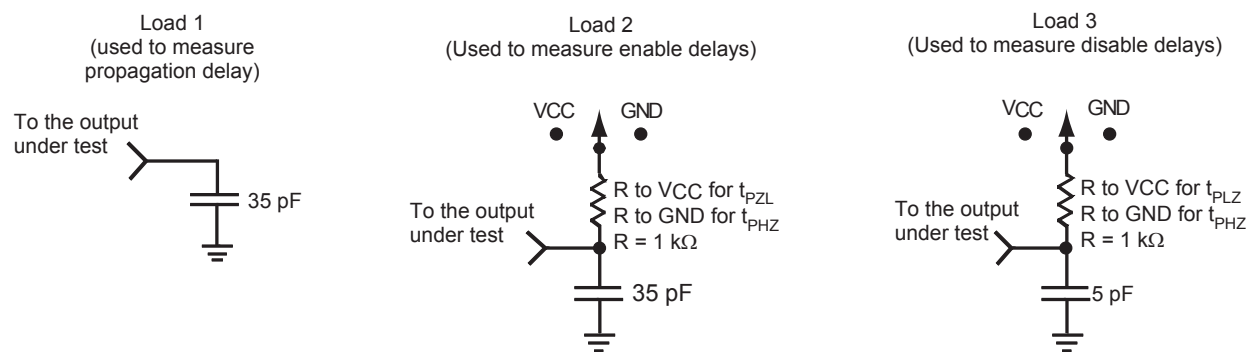


Figure 1-15 • AC Test Loads

eX Family Timing Characteristics

Table 1-17 • eX Family Timing Characteristics
(Worst-Case Commercial Conditions, VCCA = 2.3 V, T_J = 70°C)

		–P Speed		Std Speed		–F Speed		Units
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	
C-Cell Propagation Delays ¹								
t _{PD}	Internal Array Module	0.7		1.0		1.4		ns
Predicted Routing Delays ²								
t _{DC}	FO=1 Routing Delay, DirectConnect	0.1		0.1		0.2		ns
t _{FC}	FO=1 Routing Delay, FastConnect	0.3		0.5		0.7		ns
t _{RD1}	FO=1 Routing Delay	0.3		0.5		0.7		ns
t _{RD2}	FO=2 Routing Delay	0.4		0.6		0.8		ns
t _{RD3}	FO=3 Routing Delay	0.5		0.8		1.1		ns
t _{RD4}	FO=4 Routing Delay	0.7		1.0		1.3		ns
t _{RD8}	FO=8 Routing Delay	1.2		1.7		2.4		ns
t _{RD12}	FO=12 Routing Delay	1.7		2.5		3.5		ns
R-Cell Timing								
t _{RCO}	Sequential Clock-to-Q	0.6		0.9		1.3		ns
t _{CLR}	Asynchronous Clear-to-Q	0.6		0.8		1.2		ns
t _{PRESET}	Asynchronous Preset-to-Q	0.7		0.9		1.3		ns
t _{SUD}	Flip-Flop Data Input Set-Up	0.5		0.7		1.0		ns
t _{HD}	Flip-Flop Data Input Hold	0.0		0.0		0.0		ns
t _{WASYN}	Asynchronous Pulse Width	1.3		1.9		2.6		ns
t _{RECASEYN}	Asynchronous Recovery Time	0.3		0.5		0.7		ns
t _{HASYN}	Asynchronous Hold Time	0.3		0.5		0.7		ns
2.5 V Input Module Propagation Delays								
t _{INYH}	Input Data Pad-to-Y HIGH	0.6		0.9		1.3		ns
t _{INYL}	Input Data Pad-to-Y LOW	0.8		1.1		1.5		ns
3.3 V Input Module Propagation Delays								
t _{INYH}	Input Data Pad-to-Y HIGH	0.7		1.0		1.4		ns
t _{INYL}	Input Data Pad-to-Y LOW	0.9		1.3		1.8		ns
5.0 V Input Module Propagation Delays								
t _{INYH}	Input Data Pad-to-Y HIGH	0.7		1.0		1.4		ns
t _{INYL}	Input Data Pad-to-Y LOW	0.9		1.3		1.8		ns
Input Module Predicted Routing Delays ²								
t _{IRD1}	FO=1 Routing Delay	0.3		0.4		0.5		ns
t _{IRD2}	FO=2 Routing Delay	0.4		0.6		0.8		ns
t _{IRD3}	FO=3 Routing Delay	0.5		0.8		1.1		ns
t _{IRD4}	FO=4 Routing Delay	0.7		1.0		1.3		ns
t _{IRD8}	FO=8 Routing Delay	1.2		1.7		2.4		ns
t _{IRD12}	FO=12 Routing Delay	1.7		2.5		3.5		ns

Notes:

- For dual-module macros, use t_{PD} + t_{RD1} + t_{PDn}, t_{RCO} + t_{RD1} + t_{PDn} or t_{PD1} + t_{RD1} + t_{SUD}, whichever is appropriate.
- Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance.

Table 1-18 • eX Family Timing Characteristics
(Worst-Case Commercial Conditions VCCA = 2.3 V, VCCI = 4.75 V, T_J = 70°C)

		–P Speed		Std Speed		–F Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Units
Dedicated (Hard-Wired) Array Clock Networks								
t _{HCKH}	Input LOW to HIGH (Pad to R-Cell Input)		1.1		1.6		2.3	ns
t _{HCKL}	Input HIGH to LOW (Pad to R-Cell Input)		1.1		1.6		2.3	ns
t _{HPWH}	Minimum Pulse Width HIGH	1.4		2.0		2.8		ns
t _{HPWL}	Minimum Pulse Width LOW	1.4		2.0		2.8		ns
t _{HCKSW}	Maximum Skew		<0.1		<0.1		<0.1	ns
t _{HP}	Minimum Period	2.8		4.0		5.6		ns
f _{HMAX}	Maximum Frequency		357		250		178	MHz
Routed Array Clock Networks								
t _{RCKH}	Input LOW to HIGH (Light Load) (Pad to R-Cell Input) MAX.		1.1		1.6		2.2	ns
t _{RCKL}	Input HIGH to LOW (Light Load) (Pad to R-Cell Input) MAX.		1.0		1.4		2.0	ns
t _{RCKH}	Input LOW to HIGH (50% Load) (Pad to R-Cell Input) MAX.		1.2		1.7		2.4	ns
t _{RCKL}	Input HIGH to LOW (50% Load) (Pad to R-Cell Input) MAX.		1.2		1.7		2.4	ns
t _{RCKH}	Input LOW to HIGH (100% Load) (Pad to R-Cell Input) MAX.		1.3		1.9		2.6	ns
t _{RCKL}	Input HIGH to LOW (100% Load) (Pad to R-Cell Input) MAX.		1.3		1.9		2.6	ns
t _{RPWH}	Min. Pulse Width HIGH	1.5		2.1		3.0		ns
t _{RPWL}	Min. Pulse Width LOW	1.5		2.1		3.0		ns
t _{RCKSW} *	Maximum Skew (Light Load)		0.2		0.3		0.4	ns
t _{RCKSW} *	Maximum Skew (50% Load)		0.1		0.2		0.3	ns
t _{RCKSW} *	Maximum Skew (100% Load)		0.1		0.1		0.2	ns

Note: *Clock skew improves as the clock network becomes more heavily loaded.

Table 1-19 • eX Family Timing Characteristics
(Worst-Case Commercial Conditions VCCA = 2.3V, VCCI = 2.3 V or 3.0V, T_J = 70°C)

		‘P’ Speed		‘Std’ Speed		‘F’ Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Units
Dedicated (Hard-Wired) Array Clock Networks								
t _{HCKH}	Input LOW to HIGH (Pad to R-Cell Input)		1.1		1.6		2.3	ns
t _{HCKL}	Input HIGH to LOW (Pad to R-Cell Input)		1.1		1.6		2.3	ns
t _{HPWH}	Minimum Pulse Width HIGH	1.4		2.0		2.8		ns
t _{HPWL}	Minimum Pulse Width LOW	1.4		2.0		2.8		ns
t _{HCKSW}	Maximum Skew		<0.1		<0.1		<0.1	ns
t _{HP}	Minimum Period	2.8		4.0		5.6		ns
f _{HMAX}	Maximum Frequency		357		250		178	MHz
Routed Array Clock Networks								
t _{RCKH}	Input LOW to HIGH (Light Load) (Pad to R-Cell Input) MAX.		1.0		1.4		2.0	ns
t _{RCKL}	Input HIGH to LOW (Light Load) (Pad to R-Cell Input) MAX.		1.0		1.4		2.0	ns
t _{RCKH}	Input LOW to HIGH (50% Load) (Pad to R-Cell Input) MAX.		1.2		1.7		2.4	ns
t _{RCKL}	Input HIGH to LOW (50% Load) (Pad to R-Cell Input) MAX.		1.2		1.7		2.4	ns
t _{RCKH}	Input LOW to HIGH (100% Load) (Pad to R-Cell Input) MAX.		1.4		2.0		2.8	ns
t _{RCKL}	Input HIGH to LOW (100% Load) (Pad to R-Cell Input) MAX.		1.4		2.0		2.8	ns
t _{RPWH}	Min. Pulse Width HIGH	1.4		2.0		2.8		ns
t _{RPWL}	Min. Pulse Width LOW	1.4		2.0		2.8		ns
t _{RCKSW} *	Maximum Skew (Light Load)		0.2		0.3		0.4	ns
t _{RCKSW} *	Maximum Skew (50% Load)		0.2		0.2		0.3	ns
t _{RCKSW} *	Maximum Skew (100% Load)		0.1		0.1		0.2	ns

Note: *Clock skew improves as the clock network becomes more heavily loaded.

Table 1-20 • eX Family Timing Characteristics
(Worst-Case Commercial Conditions VCCA = 2.3 V, T_J = 70°C)

		–P Speed		Std Speed		–F Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Units
2.5 V LVCMOS Output Module Timing¹ (VCCI = 2.3 V)								
t _{DLH}	Data-to-Pad LOW to HIGH		3.3		4.7		6.6	ns
t _{DHL}	Data-to-Pad HIGH to LOW		3.5		5.0		7.0	ns
t _{DHLS}	Data-to-Pad HIGH to LOW—Low Slew		11.6		16.6		23.2	ns
t _{ENZL}	Enable-to-Pad, Z to L		2.5		3.6		5.1	ns
t _{ENZLS}	Enable-to-Pad Z to L—Low Slew		11.8		16.9		23.7	ns
t _{ENZH}	Enable-to-Pad, Z to H		3.4		4.9		6.9	ns
t _{ENLZ}	Enable-to-Pad, L to Z		2.1		3.0		4.2	ns
t _{ENHZ}	Enable-to-Pad, H to Z		2.4		5.67		7.94	ns
d _{TLH}	Delta Delay vs. Load LOW to HIGH		0.034		0.046		0.066	ns/pF
d _{THL}	Delta Delay vs. Load HIGH to LOW		0.016		0.022		0.05	ns/pF
d _{THLS}	Delta Delay vs. Load HIGH to LOW—Low Slew		0.05		0.072		0.1	ns/pF
3.3 V LVTTTL Output Module Timing¹ (VCCI = 3.0 V)								
t _{DLH}	Data-to-Pad LOW to HIGH		2.8		4.0		5.6	ns
t _{DHL}	Data-to-Pad HIGH to LOW		2.7		3.9		5.4	ns
t _{DHLS}	Data-to-Pad HIGH to LOW—Low Slew		9.7		13.9		19.5	ns
t _{ENZL}	Enable-to-Pad, Z to L		2.2		3.2		4.4	ns
t _{ENZLS}	Enable-to-Pad Z to L—Low Slew		9.7		13.9		19.6	ns
t _{ENZH}	Enable-to-Pad, Z to H		2.8		4.0		5.6	ns
t _{ENLZ}	Enable-to-Pad, L to Z		2.8		4.0		5.6	ns
t _{ENHZ}	Enable-to-Pad, H to Z		2.6		3.8		5.3	ns
d _{TLH}	Delta Delay vs. Load LOW to HIGH		0.02		0.03		0.046	ns/pF
d _{THL}	Delta Delay vs. Load HIGH to LOW		0.016		0.022		0.05	ns/pF
d _{THLS}	Delta Delay vs. Load HIGH to LOW—Low Slew		0.05		0.072		0.1	ns/pF
5.0 V TTL Output Module Timing* (VCCI = 4.75 V)								
t _{DLH}	Data-to-Pad LOW to HIGH		2.0		2.9		4.0	ns
t _{DHL}	Data-to-Pad HIGH to LOW		2.6		3.7		5.2	ns
t _{DHLS}	Data-to-Pad HIGH to LOW—Low Slew		6.8		9.7		13.6	ns
t _{ENZL}	Enable-to-Pad, Z to L		1.9		2.7		3.8	ns
t _{ENZLS}	Enable-to-Pad Z to L—Low Slew		6.8		9.8		13.7	ns
t _{ENZH}	Enable-to-Pad, Z to H		2.1		3.0		4.1	ns
t _{ENLZ}	Enable-to-Pad, L to Z		3.3		4.8		6.6	ns

Note: *Delays based on 35 pF loading.

Pin Description

CLKA/B Routed Clock A and B

These pins are clock inputs for clock distribution networks. Input levels are compatible with standard TTL or LVTTTL specifications. The clock input is buffered prior to clocking the R-cells. If not used, this pin must be set LOW or HIGH on the board. It must not be left floating.

GND Ground

LOW supply voltage.

HCLK Dedicated (Hardwired) Array Clock

This pin is the clock input for sequential modules. Input levels are compatible with standard TTL or LVTTTL specifications. This input is directly wired to each R-cell and offers clock speeds independent of the number of R-cells being driven. If not used, this pin must be set LOW or HIGH on the board. It must not be left floating.

I/O Input/Output

The I/O pin functions as an input, output, tristate, or bidirectional buffer. Based on certain configurations, input and output levels are compatible with standard TTL or LVTTTL specifications. Unused I/O pins are automatically tristated by the Designer software.

LP Low Power Pin

Controls the low power mode of the eX devices. The device is placed in the low power mode by connecting the LP pin to logic HIGH. In low power mode, all I/Os are tristated, all input buffers are turned OFF, and the core of the device is turned OFF. To exit the low power mode, the LP pin must be set LOW. The device enters the low power mode 800 ns after the LP pin is driven to a logic HIGH. It will resume normal operation 200 μ s after the LP pin is driven to a logic LOW. LP pin should not be left floating. Under normal operating condition it should be tied to GND via 10 k Ω resistor.

NC No Connection

This pin is not connected to circuitry within the device. These pins can be driven to any voltage or can be left floating with no effect on the operation of the device.

PRA/PRB, I/O Probe A/B

The Probe pin is used to output data from any user-defined design node within the device. This diagnostic pin can be used independently or in conjunction with the other probe pin to allow real-time diagnostic output of any signal path within the device. The Probe pin can be used as a user-defined I/O when verification has been completed. The pin's probe capabilities can be permanently disabled to protect programmed design confidentiality.

TCK, I/O Test Clock

Test clock input for diagnostic probe and device programming. In flexible mode, TCK becomes active when the TMS pin is set LOW (refer to [Table 1-4 on page 1-10](#)). This pin functions as an I/O when the boundary scan state machine reaches the "logic reset" state.

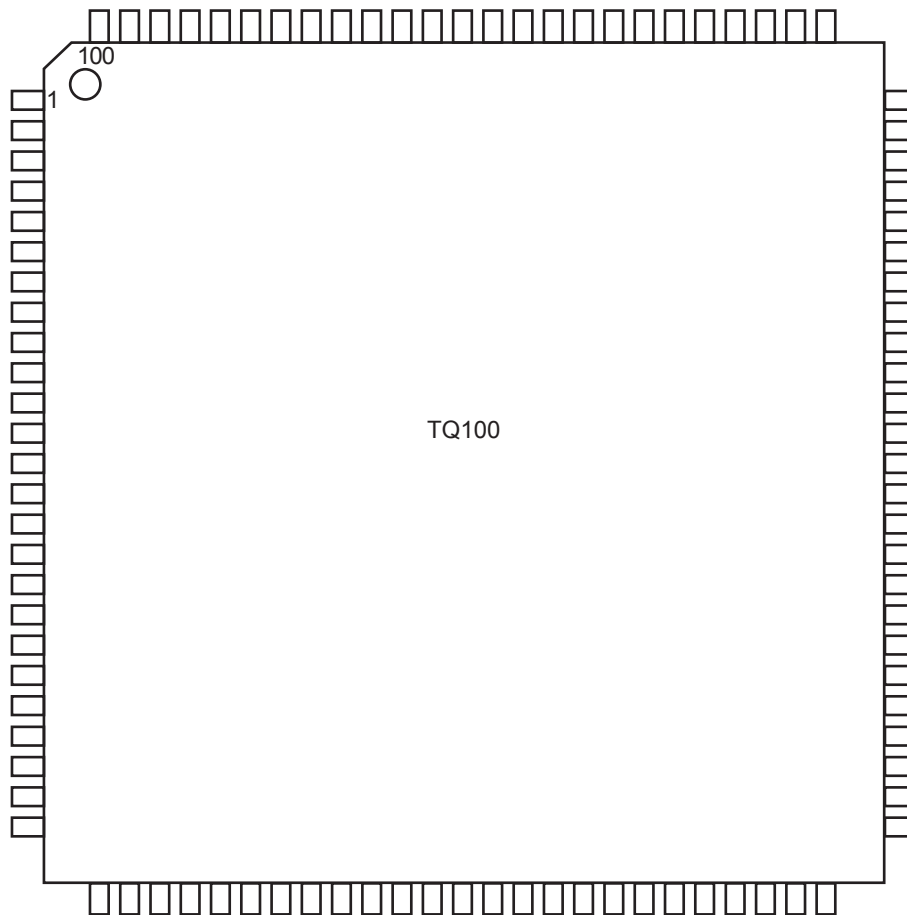
TDI, I/O Test Data Input

Serial input for boundary scan testing and diagnostic probe. In flexible mode, TDI is active when the TMS pin is set LOW (refer to [Table 1-4 on page 1-10](#)). This pin functions as an I/O when the boundary scan state machine reaches the "logic reset" state.

TDO, I/O Test Data Output

Serial output for boundary scan testing. In flexible mode, TDO is active when the TMS pin is set LOW (refer to [Table 1-4 on page 1-10](#)). This pin functions as an I/O when the boundary scan state machine reaches the "logic reset" state. When Silicon Explorer is being used, TDO will act as an output when the "checksum" command is run. It will return to user I/O when "checksum" is complete.

TQ100



Note: For Package Manufacturing and Environmental information, visit Resource center at www.microsemi.com/soc/products/rescenter/package/index.html.

TQ100			
Pin Number	eX64 Function	eX128 Function	eX256 Function
1	GND	GND	GND
2	TDI, I/O	TDI, I/O	TDI, I/O
3	NC	NC	I/O
4	NC	NC	I/O
5	NC	NC	I/O
6	I/O	I/O	I/O
7	TMS	TMS	TMS
8	VCCI	VCCI	VCCI
9	GND	GND	GND
10	NC	I/O	I/O
11	NC	I/O	I/O
12	I/O	I/O	I/O
13	NC	I/O	I/O
14	I/O	I/O	I/O
15	NC	I/O	I/O
16	TRST, I/O	TRST, I/O	TRST, I/O
17	NC	I/O	I/O
18	I/O	I/O	I/O
19	NC	I/O	I/O
20	VCCI	VCCI	VCCI
21	I/O	I/O	I/O
22	NC	I/O	I/O
23	NC	NC	I/O
24	NC	NC	I/O
25	I/O	I/O	I/O
26	I/O	I/O	I/O
27	I/O	I/O	I/O
28	I/O	I/O	I/O
29	I/O	I/O	I/O
30	I/O	I/O	I/O
31	I/O	I/O	I/O
32	I/O	I/O	I/O
33	I/O	I/O	I/O
34	PRB, I/O	PRB, I/O	PRB, I/O
35	VCCA	VCCA	VCCA

TQ100			
Pin Number	eX64 Function	eX128 Function	eX256 Function
36	GND	GND	GND
37	NC	NC	NC
38	I/O	I/O	I/O
39	HCLK	HCLK	HCLK
40	I/O	I/O	I/O
41	I/O	I/O	I/O
42	I/O	I/O	I/O
43	I/O	I/O	I/O
44	VCCI	VCCI	VCCI
45	I/O	I/O	I/O
46	I/O	I/O	I/O
47	I/O	I/O	I/O
48	I/O	I/O	I/O
49	TDO, I/O	TDO, I/O	TDO, I/O
50	NC	I/O	I/O
51	GND	GND	GND
52	NC	NC	I/O
53	NC	NC	I/O
54	NC	NC	I/O
55	I/O	I/O	I/O
56	I/O	I/O	I/O
57	VCCA	VCCA	VCCA
58	VCCI	VCCI	VCCI
59	NC	I/O	I/O
60	I/O	I/O	I/O
61	NC	I/O	I/O
62	I/O	I/O	I/O
63	NC	I/O	I/O
64	I/O	I/O	I/O
65	NC	I/O	I/O
66	I/O	I/O	I/O
67	VCCA	VCCA	VCCA
68	GND/LP	GND/LP	GND/LP
69	GND	GND	GND
70	I/O	I/O	I/O

Note: *Please read the LP pin descriptions for restrictions on their use.

TQ100			
Pin Number	eX64 Function	eX128 Function	eX256 Function
71	I/O	I/O	I/O
72	NC	I/O	I/O
73	NC	NC	I/O
74	NC	NC	I/O
75	NC	NC	I/O
76	NC	I/O	I/O
77	I/O	I/O	I/O
78	I/O	I/O	I/O
79	I/O	I/O	I/O
80	I/O	I/O	I/O
81	I/O	I/O	I/O
82	VCCI	VCCI	VCCI
83	I/O	I/O	I/O
84	I/O	I/O	I/O
85	I/O	I/O	I/O
86	I/O	I/O	I/O
87	CLKA	CLKA	CLKA
88	CLKB	CLKB	CLKB
89	NC	NC	NC
90	VCCA	VCCA	VCCA
91	GND	GND	GND
92	PRA, I/O	PRA, I/O	PRA, I/O
93	I/O	I/O	I/O
94	I/O	I/O	I/O
95	I/O	I/O	I/O
96	I/O	I/O	I/O
97	I/O	I/O	I/O
98	I/O	I/O	I/O
99	I/O	I/O	I/O
100	TCK, I/O	TCK, I/O	TCK, I/O

Note: *Please read the LP pin descriptions for restrictions on their use.

Datasheet Categories

Categories

In order to provide the latest information to designers, some datasheet parameters are published before data has been fully characterized from silicon devices. The data provided for a given device, as highlighted in the ["eX Device Status" table on page II](#), is designated as either "Product Brief," "Advance," "Preliminary," or "Production." The definitions of these categories are as follows:

Product Brief

The product brief is a summarized version of a datasheet (advance or production) and contains general product information. This document gives an overview of specific device and family information.

Advance

This version contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production. This label only applies to the DC and Switching Characteristics chapter of the datasheet and will only be used when the data has not been fully characterized.

Preliminary

The datasheet contains information based on simulation and/or initial characterization. The information is believed to be correct, but changes are possible.

Production

This version contains information that is considered to be final.

Export Administration Regulations (EAR)

The product described in this datasheet is subject to the Export Administration Regulations (EAR). They could require an approved export license prior to export from the United States. An export includes release of product or disclosure of technology to a foreign national inside or outside the United States.