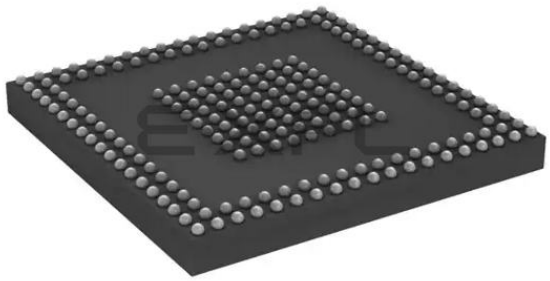


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	XCore
Core Size	32-Bit 16-Core
Speed	1000MIPS
Connectivity	Configurable
Peripherals	-
Number of I/O	73
Program Memory Size	128KB (32K x 32)
Program Memory Type	SRAM
EEPROM Size	-
RAM Size	-
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	217-LFBGA
Supplier Device Package	217-FBGA (16x16)
Purchase URL	https://www.e-xfl.com/product-detail/xmos/xs1-u16a-128-fb217-i10

3 Pin Configuration

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
A	8B X1D05	8B X1D06	8B X1D07	8A X1D08	1A X1D09	1C X1D10	1C X1D11	1C X1D12	1C X1D13	1C X1D14	1C X1D15	1C X1D16	1C X1D17	1C X1D18	1C X1D19	1C X1D20	1C X1D21	1D X1D22	1D X1D23
B	1B X1D04	10A X1D53	10A X1D54	10A X1D55	10A X1D56	10A X1D57	10A X1D58	10A X1D61	10A X1D62	10A X1D63	10A X1D64	10A X1D65	10A X1D66	10A X1D67	10A X1D68	10A X1D69	10A X1D70	1B X1D24	1B X1D25
C	4A X1D03	32A X1D52																4E X1D26	4E X1D27
D	4A X1D02	32A X1D51																4E X1D33	4E X1D32
E	1B X1D01	32A X1D50																1L X1D35	1K X1D34
F	1 X1D00	32A X1D49				GND	GND	GND	GND	GND	GND	GND	GND	GND				VDDIO_ OUT	1J X1D36
G	USB_ DN	USB VBUS				GND	GND	GND	GND	GND	GND	GND	GND	GND				MODE[4]	1H X1D37
H	USB_ DP	USB_ ID				GND	GND	GND	GND	GND	GND	GND	GND	GND				MODE[3]	1G X1D38
J	X0D43/ WAKE	RST_N				GND	GND	GND	GND	GND	GND	GND	GND	GND				MODE[2]	1F X1D39
K	VDDIO	VDDIO				GND	GND	GND	GND	GND	GND	GND	GND	GND				MODE[1]	TDO
L	ADC6	ADC7				OSC_ EXT_N	GND	GND	GND	GND	GND	GND	GND	GND				MODE[0]	TCK
M	ADC4	ADC5				NC	NC	GND	GND	GND	GND	GND	GND	GND				DEBUG_ N	TMS
N	AVDD	AVSS				NC	NC	GND	GND	GND	GND	GND	GND	GND				NC	TDI
P	ADC2	ADC3				AVSS	GND	GND	GND	GND	GND	GND	GND	GND				NC	1L X0D35
R	ADC0	ADC1																NC	1A X0D00
T	NC	NC																NC	1B X0D01
U	XI/ CLK	NC																NC	1J X0D10
V	XO	NC	VDDCORE	PGND	PGND	SW1	VSUP	VDD1V8	PGND	PGND	SW2	NC	1I X0D24	4C X0D21	4D X0D19	4D X0D17	4C X0D15	NC	1D X0D11
W	VSUP	NC	VDDCORE	VDDCORE	PGND	SW1	VSUP	VDD1V8	VDD1V8	PGND	SW2	NC	1G X0D22	4C X0D20	4D X0D18	4D X0D16	4C X0D14	1F X0D13	1E X0D12

Signal	Function	Type	Properties
USB_DP	USB Serial Data	I/O	
USB_ID	USB Device ID (OTG) - Reserved	Output	
USB_VBUS	USB Power Detect Pin	Input	

Clocks pins (4)			
Signal	**Function**	**Type**	**Properties**
MODE[4:0]	Boot mode select	Input	PU, ST
OSC_EXT_N	Use Silicon Oscillator	Input	ST
XI/CLK	Crystal Oscillator/Clock Input	Input	
XO	Crystal Oscillator Output	Output	

JTAG pins (5)			
Signal	**Function**	**Type**	**Properties**
DEBUG_N	Multi-chip debug	I/O	PU
TCK	Test clock	Input	PU, ST
TDI	Test data input	Input	PU, ST
TDO	Test data output	Output	PD, OT
TMS	Test mode select	Input	PU, ST

Misc pins (1)			
Signal	**Function**	**Type**	**Properties**
RST_N	Global reset input	Input	PU, ST

I/O pins (74)			
Signal	**Function**	**Type**	**Properties**
X0D00	$1A^{0}$	I/O	PD_S, R_S
X0D01	$1B^{0}$	I/O	PD_S, R_S
X0D10	$1C^{0}$	I/O	PD_S, R_S
X0D11	$1D^{0}$	I/O	PD_S, R_S
X0D12	$1E^{0}$	I/O	PD_S
X0D13	XLB^{4}_{out} $1F^{0}$	I/O	PD_S
X0D14	XLB^{3}_{out} $4C^{0}$ $8B^{0}$ $16A^{8}$ $32A^{28}$	I/O	PD_S
X0D15	XLB^{2}_{out} $4C^{1}$ $8B^{1}$ $16A^{9}$ $32A^{29}$	I/O	PD_S
X0D16	XLB^{1}_{out} $4D^{0}$ $8B^{2}$ $16A^{10}$	I/O	PD_S
X0D17	XLB^{0}_{out} $4D^{1}$ $8B^{3}$ $16A^{11}$	I/O	PD_S
X0D18	XLB^{0}_{in} $4D^{2}$ $8B^{4}$ $16A^{12}$	I/O	PD_S
X0D19	XLB^{1}_{in} $4D^{3}$ $8B^{5}$ $16A^{13}$	I/O	PD_S
X0D20	XLB^{2}_{in} $4C^{2}$ $8B^{6}$ $16A^{14}$ $32A^{30}$	I/O	PD_S

(continued)

Feature	Bit	Description
Disable JTAG	0	The JTAG interface is disabled, making it impossible for the tile state or memory content to be accessed via the JTAG interface.
Disable Link access	1	Other tiles are forbidden access to the processor state via the system switch. Disabling both JTAG and Link access transforms an xCORE Tile into a “secure island” with other tiles free for non-secure user application code.
Secure Boot	5	The processor is forced to boot from address 0 of the OTP, allowing the processor boot ROM to be bypassed (*see* §9).
Redundant rows	7	Enables redundant rows in OTP.
Sector Lock 0	8	Disable programming of OTP sector 0.
Sector Lock 1	9	Disable programming of OTP sector 1.
Sector Lock 2	10	Disable programming of OTP sector 2.
Sector Lock 3	11	Disable programming of OTP sector 3.
OTP Master Lock	12	Disable OTP programming completely: disables updates to all sectors and security register.
Disable JTAG-OTP	13	Disable all (read & write) access from the JTAG interface to this OTP.
Disable Global Debug	14	Disables access to the DEBUG_N pin.
	21..15	General purpose software accessable security register available to end-users.
	31..22	General purpose user programmable JTAG UserID code extension.

Figure 12: Security register features

port with resource ID 0x200100, and the OTP control is on a 16-bit port with ID 0x100300. Programming is performed through `libotp` and `xburn`.

10.2 SRAM

Each xCORE Tile integrates a single 64KB SRAM bank for both instructions and data. All internal memory is 32 bits wide, and instructions are either 16-bit or 32-bit. Byte (8-bit), half-word (16-bit) or word (32-bit) accesses are supported and are executed within one tile clock cycle. There is no dedicated external memory interface, although data memory can be expanded through appropriate use of the ports.

10.3 Deep Sleep Memory

The XS1-U16A-128-FB217 device includes 128 bytes of deep sleep memory for state storage during sleep mode. Deep sleep memory is volatile and if device input power is remove, the data will be lost.

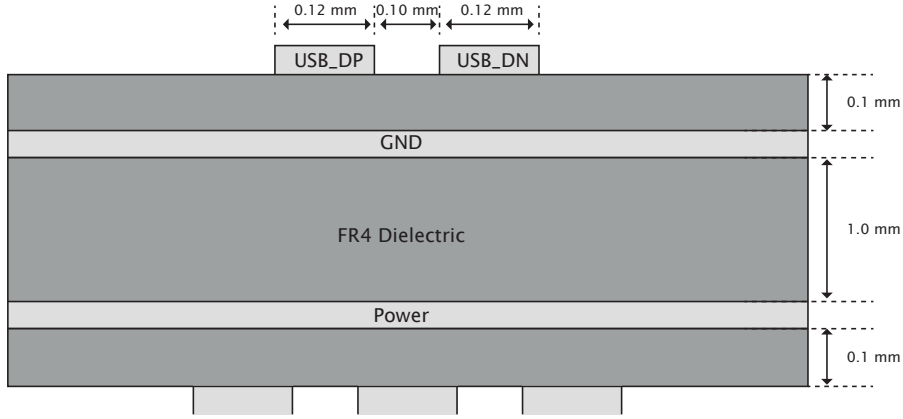


Figure 21: Example USB board stack

For best results, most of the routing should be done on the top layer (assuming the USB connector and XS1-U16A-128-FB217 are on the top layer) closest to GND. Reference planes should be below the transmission lines in order to maintain control of the trace impedance.

We recommend that the high-speed clock and high-speed USB differential pairs are routed first before any other routing. When routing high speed USB signals, the following guidelines should be followed:

- High speed differential pairs should be routed together.
- High-speed USB signal pair traces should be trace-length matched. Maximum trace-length mismatch should be no greater than 4mm.
- Ensure that high speed signals (clocks, USB differential pairs) are routed as far away from off-board connectors as possible.
- High-speed clock and periodic signal traces that run parallel should be at least 1.27mm away from USB_DP/USB_DN (see Figure 20).
- Low-speed and non-periodic signal traces that run parallel should be at least 0.5mm away from USB_DP/USB_DN (see Figure 20).
- Route high speed USB signals on the top of the PCB wherever possible.
- Route high speed USB traces over continuous power planes, with no breaks. If a trade-off must be made, changing signal layers is preferable to crossing plane splits.
- Follow the $20 \times h$ rule; keep traces $20 \times h$ (the height above the power plane) away from the edge of the power plane.
- Use a minimum of vias in high speed USB traces.

- Avoid corners in the trace. Where necessary, rather than turning through a 90 degree angle, use two 45 degree turns or an arc.
- DO NOT route USB traces near clock sources, clocked circuits or magnetic devices.
- Avoid stubs on high speed USB signals.

16.3 Land patterns and solder stencils

The land pattern recommendations in this document are based on a RoHS compliant process and derived, where possible, from the nominal *Generic Requirements for Surface Mount Design and Land Pattern Standards* IPC-7351B specifications. This standard aims to achieve desired targets of heel, toe and side fillets for solder-joints.

Solder paste and ground via recommendations are based on our engineering and development kit board production. They have been found to work and optimized as appropriate to achieve a high yield. These factors should be taken into account during design and manufacturing of the PCB.

The following land patterns and solder paste contains recommendations. Final land pattern and solder paste decisions are the responsibility of the customer. These should be tuned during manufacture to suit the manufacturing process.

The package is a 217 pin Fine Ball Grid Array package on a 0.8mm pitch with 0.4mm balls.

An example land pattern is shown in Figure 22.

Pad widths and spacings are such that solder mask can still be applied between the pads using standard design rules. This is highly recommended to reduce solder shorts.

16.4 Ground and Thermal Vias

Vias next to every other ground ball into the ground plane of the PCB are recommended for a low inductance ground connection and good thermal performance. Vias with with a 0.6mm diameter annular ring and a 0.3mm drill would be suitable.

16.5 Moisture Sensitivity

XMOS devices are, like all semiconductor devices, susceptible to moisture absorption. When removed from the sealed packaging, the devices slowly absorb moisture from the surrounding environment. If the level of moisture present in the device is too high during reflow, damage can occur due to the increased internal vapour pressure of moisture. Example damage can include bond wire damage, die lifting, internal or external package cracks and/or delamination.

All XMOS devices are Moisture Sensitivity Level (MSL) 3 - devices have a shelf life of 168 hours between removal from the packaging and reflow, provided they

17 Example XS1-U16A-128-FB217 Board Designs

This section shows example schematics and layout for a 2-layer PCB.

- Figures 23 shows example schematics and layout. It uses a 24 MHz crystal for the clock, and an SPI flash for booting. The XS1-U16A-128-FB217 is powered directly from 5V. An optional ESD protection device is included to increase ESD protection from 2 to 15 kV.
- Figures 24 shows example schematics and layout for a design that uses an oscillator rather than a crystal. If required a 3V3 oscillator can be used (for example when sharing an oscillator with other parts of the design), but a resistor bridge must be included to reduce the XI/CLK input from 3V3 to 1V8.
- Figure 25 shows example schematics and layout for a design that does not use USB and that runs off the internal 20 MHz oscillator. The XS1-U16A-128-FB217 is powered directly from 3V3.

Flash, AVDD, RST, and JTAG connectivity are all optional. Flash can be removed if the processor boots from OTP. The AVDD decoupler and wiring can be removed if the ADC is not used. RST_N and all JTAG wiring can be removed if debugging is not required (see Appendix M)

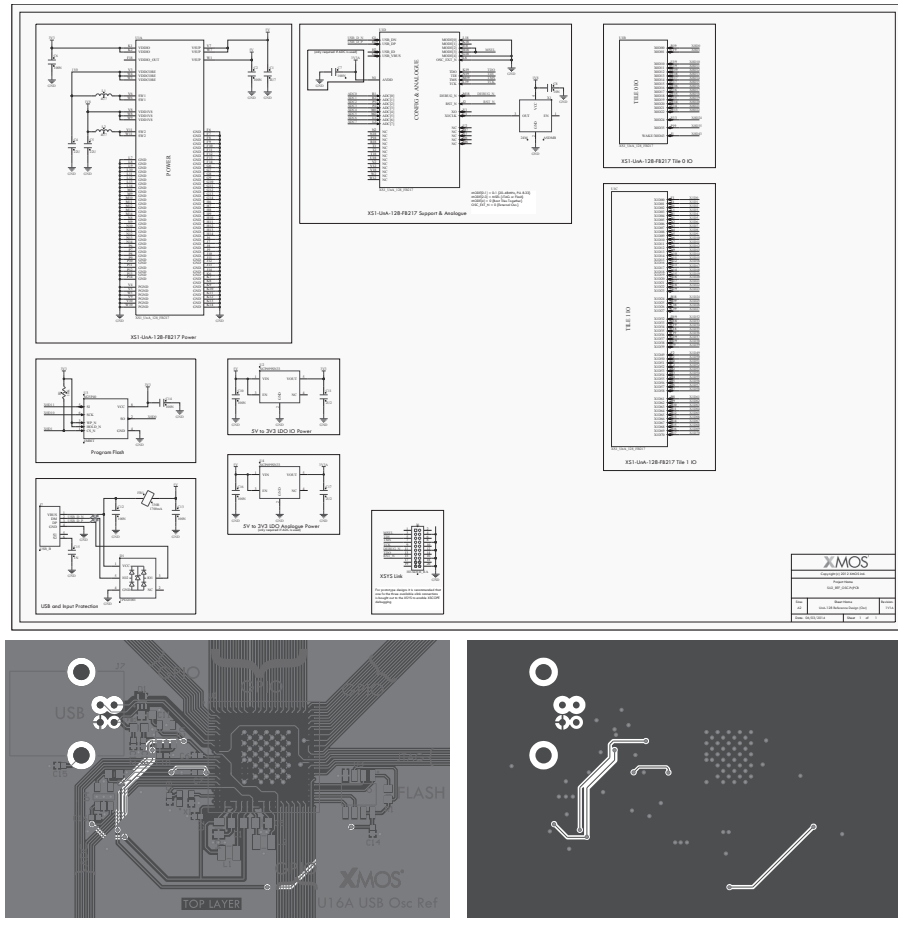


Figure 24: Example Oscillator schematic, with top and bottom layout of a 2-layer PCB

18.10 External Oscillator Characteristics

Figure 35: External oscillator characteristics

Symbol	Parameter	MIN	TYP	MAX	UNITS	Notes
F(EXT)	External Frequency			100	MHz	A
V(IH)	Input high voltage	1.62		1.98	V	
V(IL)	Input low voltage			0.4	V	

A For use with USB, the design should use a 12 or 24 MHz +/- 150 ppm crystal.

18.11 Power Consumption

Figure 36: xCORE Tile currents

Symbol	Parameter	MIN	TYP	MAX	UNITS	Notes
P(AWAKE)	Active Power for awake states	TBC	600	TBC	mW	
P(SLEEP)	Power when asleep	TBC	500	TBC	µW	

18.12 Clock

Figure 37: Clock

Symbol	Parameter	MIN	TYP	MAX	UNITS	Notes
f(MAX)	Processor clock frequency			500	MHz	A

A Assumes typical tile and I/O voltages with nominal activity.

18.13 Processor I/O AC Characteristics

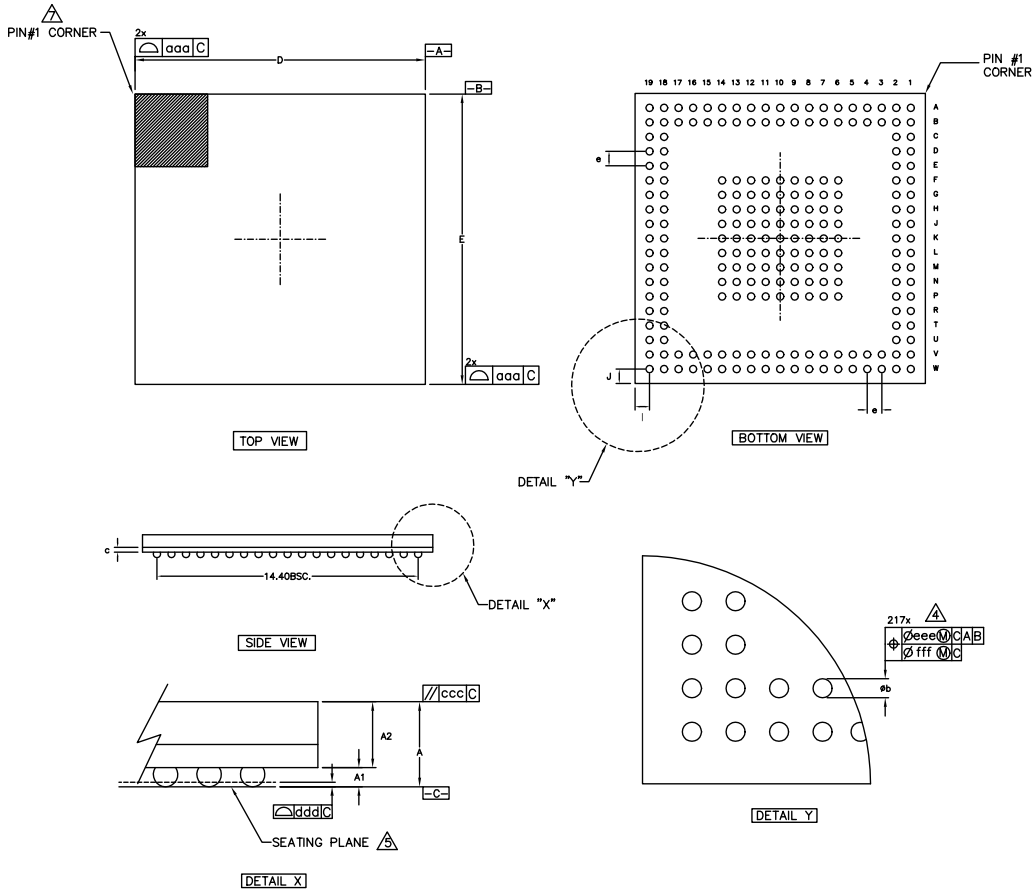
Figure 38: I/O AC characteristics

Symbol	Parameter	MIN	TYP	MAX	UNITS	Notes
T(XOVALID)	Input data valid window	8			ns	
T(XOINVALID)	Output data invalid window	9			ns	
T(XIFMAX)	Rate at which data can be sampled with respect to an external clock			60	MHz	

The input valid window parameter relates to the capability of the device to capture data input to the chip with respect to an external clock source. It is calculated as the sum of the input setup time and input hold time with respect to the external clock as measured at the pins. The output invalid window specifies the time for which an output is invalid with respect to the external clock. Note that these parameters are specified as a window rather than absolute numbers since the device provides functionality to delay the incoming clock with respect to the incoming data.

Information on interfacing to high-speed synchronous interfaces can be found in the XS1 Port I/O Timing document, X5821.

19 Package Information



NOTE:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. "e" REPRESENTS THE BASIC SOLDER BALL GRID PITCH.
3. "M" REPRESENTS THE MAXIMUM SOLDER BALL MATRIX SIZE.
4. DEMENSIONS "b" IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER PARALLEL TO PRIMARY DATUM -C- .
5. PRIMARY DATUM -C- AND SEATING PLANE ARE DESIGNED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
6. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994
7. A1 CORNER MUST BE IDENTIFIED BY INK OR LASER MARK.
8. PACKAGE DIMENSIONS CONFORM TO JEDEC REGISTRATION MO–275.

SYMBOL	MIN.	NOM.	MAX.
A	1.16	1.26	1.36
A1	0.25	0.30	0.35
A2	0.91	0.96	1.01
D	15.90	16.00	16.10
E	15.90	16.00	16.10
I		0.80 REF.	
J		0.80 REF.	
M		19 X 19<DEPOPULATED>	
aaa			0.15
ccc			0.20
ddd			0.10
eee			0.15
fff			0.08
b	0.35	0.40	0.45
e		0.80 BSC.	
c		0.26 REF.	

19.1 Part Marking

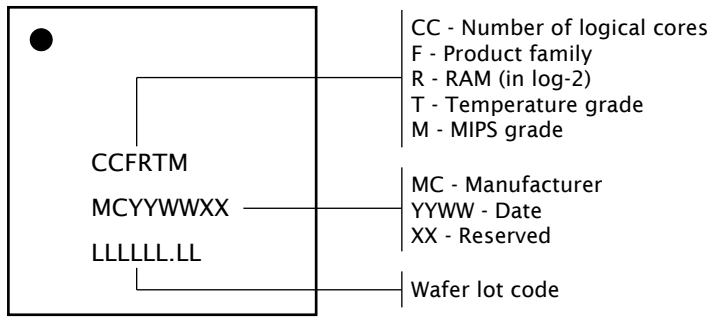


Figure 41: Part marking scheme

20 Ordering Information

Figure 42: Orderable part numbers

Product Code	Marking	Qualification	Speed Grade
XS1-U16A-128-FB217-C10	16U7C10	Commercial	1000 MIPS
XS1-U16A-128-FB217-I10	16U7I10	Industrial	1000 MIPS

B Processor Status Configuration

The processor status control registers can be accessed directly by the processor using processor status reads and writes (use `getps(reg)` and `setps(reg,value)` for reads and writes).

Number	Perm	Description
0x00	RW	RAM base address
0x01	RW	Vector base address
0x02	RW	xCORE Tile control
0x03	RO	xCORE Tile boot status
0x05	RO	Security configuration
0x06	RW	Ring Oscillator Control
0x07	RO	Ring Oscillator Value
0x08	RO	Ring Oscillator Value
0x09	RO	Ring Oscillator Value
0x0A	RO	Ring Oscillator Value
0x10	DRW	Debug SSR
0x11	DRW	Debug SPC
0x12	DRW	Debug SSP
0x13	DRW	DGETREG operand 1
0x14	DRW	DGETREG operand 2
0x15	DRW	Debug interrupt type
0x16	DRW	Debug interrupt data
0x18	DRW	Debug core control
0x20 .. 0x27	DRW	Debug scratch
0x30 .. 0x33	DRW	Instruction breakpoint address
0x40 .. 0x43	DRW	Instruction breakpoint control
0x50 .. 0x53	DRW	Data watchpoint address 1
0x60 .. 0x63	DRW	Data watchpoint address 2
0x70 .. 0x73	DRW	Data breakpoint control register
0x80 .. 0x83	DRW	Resources breakpoint mask
0x90 .. 0x93	DRW	Resources breakpoint value
0x9C .. 0x9F	DRW	Resources breakpoint control register

Figure 44: Summary

D.13 PLink status and network: 0x40 .. 0x43

These registers contain status information and the network number that each processor-link belongs to.

0x40 .. 0x43: PLink status and network

Bits	Perm	Init	Description
31:26	RO	-	Reserved
25:24	RO		If this link is currently routing data into the switch, this field specifies the type of link that the data is routed to: 0: plink 1: external link 2: internal control link
23:16	RO	0	If the link is routing data into the switch, this field specifies the destination link number to which all tokens are sent.
15:6	RO	-	Reserved
5:4	RW	0	Determines the network to which this link belongs, set for quality of service.
3	RO	-	Reserved
2	RO	0	Set to 1 if the current packet is junk and being thrown away. A packet is considered junk if, for example, it is not routable.
1	RO	0	Set to 1 if the switch is routing data into the link, and if a route exists from another link.
0	RO	0	Set to 1 if the link is routing data into the switch, and if a route is created to another link on the switch.

D.14 Link configuration and initialization: 0x80 .. 0x87

These registers contain configuration and debugging information specific to external links. The link speed and width can be set, the link can be initialized, and the link status can be monitored. The registers control links C, D, A, B, G, H, E, and F in that order.

E Analogue Node Configuration

The analogue node control registers can be accessed using configuration reads and writes (use `write_node_config_reg(device, ...)` and `read_node_config_reg(device, ...)` for reads and writes).

Figure 47: Summary

Number	Perm	Description
0x00	RO	Device identification register
0x04	RW	Node configuration register
0x05	RW	Node identifier
0x50	RW	Reset and Mode Control
0x51	RW	System clock frequency
0x80	RW	Link Control and Status
0xD6	RW	1 KHz Watchdog Control
0xD7	RW	Watchdog Disable

E.1 Device identification register: 0x00

This register contains version information, and information on power-on behavior.

0x00: Device identification register

Bits	Perm	Init	Description
31:24	RO	0x0F	Chip identifier
23:17	RO	-	Reserved
16	RO	pin	Oscillator used on power-up. This is set by the OSC_EXT_N pin: 0: boot from crystal; 1: boot from on-silicon 20 MHz oscillator.
15:8	RO	0x02	Revision number of the analogue block
7:0	RO	0x00	Version number of the analogue block

E.2 Node configuration register: 0x04

This register is used to set the communication model to use (1 or 3 byte headers), and to prevent any further updates.

0x20: UIFM Sticky flags

Bits	Perm	Init	Description
31:7	RO	-	Reserved
6:0	RW	0	Stickyness for each flag.

F.10 UIFM port masks: 0x24

Set of masks that identify how port 1N, port 1O and port 1P are affected by changes to the flags in FLAGS

0x24: UIFM port masks

Bits	Perm	Init	Description
31:23	RO	-	Reserved
22:16	RW	0	Bit mask that determines which flags in UIFM_IFM_FLAG[6:0] contribute to port 1P. If any flag listed in this bitmask is high, port 1P will be high.
15	RO	-	Reserved
14:8	RW	0	Bit mask that determines which flags in UIFM_IFM_FLAG[6:0] contribute to port 1O. If any flag listed in this bitmask is high, port 1O will be high.
7	RO	-	Reserved
6:0	RW	0	Bit mask that determines which flags in UIFM_IFM_FLAG[6:0] contribute to port 1N. If any flag listed in this bitmask is high, port 1N will be high.

F.11 UIFM SOF value: 0x28

USB Start-Of-Frame counter

0x28: UIFM SOF value

Bits	Perm	Init	Description
31:11	RO	-	Reserved
10:8	RW	0	Most significant 3 bits of SOF counter
7:0	RW	0	Least significant 8 bits of SOF counter

F.12 UIFM PID: 0x2C

The last USB packet identifier received

0x2C: UIFM PID

Bits	Perm	Init	Description
31:4	RO	-	Reserved
3:0	RO	0	Value of the last received PID.

F.13 UIFM Endpoint: 0x30

The last endpoint seen

0x30: UIFM Endpoint

Bits	Perm	Init	Description
31:5	RO	-	Reserved
4	RO	0	1 if endpoint contains a valid value.
3:0	RO	0	A copy of the last received endpoint.

F.14 UIFM Endpoint match: 0x34

This register can be used to mark UIFM endpoints as special.

0x34: UIFM Endpoint match

Bits	Perm	Init	Description
31:16	RO	-	Reserved
15:0	RW	0	This register contains a bit for each endpoint. If its bit is set, the endpoint will be supplied on the RX port when ORed with 0x10.

F.15 UIFM power signalling: 0x38

0x38: UIFM power signalling

Bits	Perm	Init	Description
31:9	RO	-	Reserved
8	RW	0	Valid
7:0	RW	0	Data

0x0C: ADC Control input pin 3

Bits	Perm	Init	Description
31:8	RW	0	The node and channel-end identifier to which data for this ADC input pin should be send to. This is the top 24 bits of the channel-end identifier as allocated on an xCORE Tile.
7:1	RO	-	Reserved
0	RW	0	Set to 1 to enable this input pin on the ADC.

G.5 ADC Control input pin 4: 0x10

Controls specific to ADC input pin 4.

0x10: ADC Control input pin 4

Bits	Perm	Init	Description
31:8	RW	0	The node and channel-end identifier to which data for this ADC input pin should be send to. This is the top 24 bits of the channel-end identifier as allocated on an xCORE Tile.
7:1	RO	-	Reserved
0	RW	0	Set to 1 to enable this input pin on the ADC.

G.6 ADC Control input pin 5: 0x14

Controls specific to ADC input pin 5.

0x14: ADC Control input pin 5

Bits	Perm	Init	Description
31:8	RW	0	The node and channel-end identifier to which data for this ADC input pin should be send to. This is the top 24 bits of the channel-end identifier as allocated on an xCORE Tile.
7:1	RO	-	Reserved
0	RW	0	Set to 1 to enable this input pin on the ADC.

G.7 ADC Control input pin 6: 0x18

Controls specific to ADC input pin 6.

Number	Perm	Description
0x00	RW	General control
0x04	RW	Time to wake-up, least significant 32 bits
0x08	RW	Time to wake-up, most significant 32 bits
0x0C	RW	Power supply states whilst ASLEEP
0x10	RW	Power supply states whilst WAKING1
0x14	RW	Power supply states whilst WAKING2
0x18	RW	Power supply states whilst AWAKE
0x1C	RW	Power supply states whilst SLEEPING1
0x20	RW	Power supply states whilst SLEEPING2
0x24	RW	Power sequence status
0x2C	RW	DCDC control
0x30	RW	Power supply status
0x34	RW	VDDCORE level control
0x40	RW	LDO5 level control

Figure 53: Summary

K.1 General control: 0x00

This register controls the basic settings for power modes.

Bits	Perm	Init	Description
31:21	RO	-	Reserved
20:16	RW	16	Log2 number of cycles to stay in this state: 0: 1 clock cycles 1: 2 clock cycles 2: 4 clock cycles ... 31: 2147483648 clock cycles
15	RO	-	Reserved
14	RW	0	Set to 1 to disable clock to the xCORE Tile.
13:10	RO	-	Reserved
9	RW	0	Sets modulation used by DCDC2: 0: PWM modulation (max 475 mA) 1: PFM modulation (max 50 mA)
8	RW	0	Sets modulation used by DCDC1: 0: PWM modulation (max 700 mA) 1: PFM modulation (max 50 mA)
7:6	RO	-	Reserved
5	RW	1	Set to 1 to enable VOUT6 (IO supply).
4	RW	1	Set to 1 to enable LDO5 (core PLL supply).
3:2	RO	-	Reserved
1	RO	1	Set to 1 to enable DCDC2 (analogue supply).
0	RW	1	Set to 1 to enable DCDC1 (core supply).

0x14: Power supply states whilst WAKING2

K.7 Power supply states whilst AWAKE: 0x18

This register controls what state the power control block should be in when in the AWAKE state.

Bits	Perm	Init	Description
31:21	RO	-	Reserved
20:16	RW	16	Log2 number of cycles to stay in this state: 0: 1 clock cycles 1: 2 clock cycles 2: 4 clock cycles ... 31: 2147483648 clock cycles
15	RO	-	Reserved
14	RW	0	Set to 1 to disable clock to the xCORE Tile.
13:10	RO	-	Reserved
9	RW	0	Sets modulation used by DCDC2: 0: PWM modulation (max 475 mA) 1: PFM modulation (max 50 mA)
8	RW	0	Sets modulation used by DCDC1: 0: PWM modulation (max 700 mA) 1: PFM modulation (max 50 mA)
7:6	RO	-	Reserved
5	RW	0	Set to 1 to enable VOUT6 (IO supply).
4	RW	0	Set to 1 to enable LDO5 (core PLL supply).
3:2	RO	-	Reserved
1	RO	1	Set to 1 to enable DCDC2 (analogue supply).
0	RW	0	Set to 1 to enable DCDC1 (core supply).

0x20: Power supply states whilst SLEEPING2

K.10 Power sequence status: 0x24

This register defines the current status of the power supply controller.