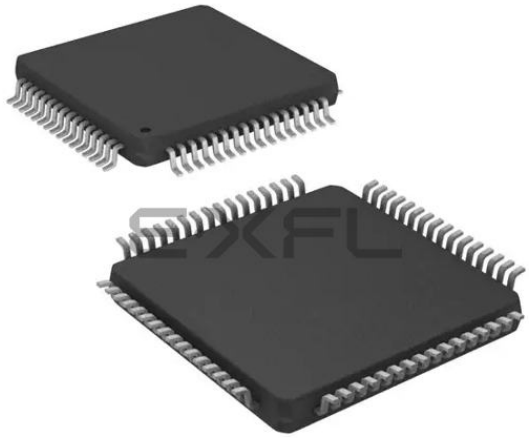

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	64MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	60
Program Memory Size	64KB (32K x 16)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	3.5K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 45x10b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18lf66k40-i-pt

2.0 GUIDELINES FOR GETTING STARTED WITH PIC18(L)F6XK40 MICROCONTROLLERS

2.1 Basic Connection Requirements

Getting started with the PIC18(L)F6xK40 family of 8-bit microcontrollers requires attention to a minimal set of device pin connections before proceeding with development.

The following pins must always be connected:

- All VDD and VSS pins (see **Section 2.2 "Power Supply Pins"**)
- $\overline{\text{MCLR}}$ pin (see **Section 2.3 "Master Clear (MCLR) Pin"**)

These pins must also be connected if they are being used in the end application:

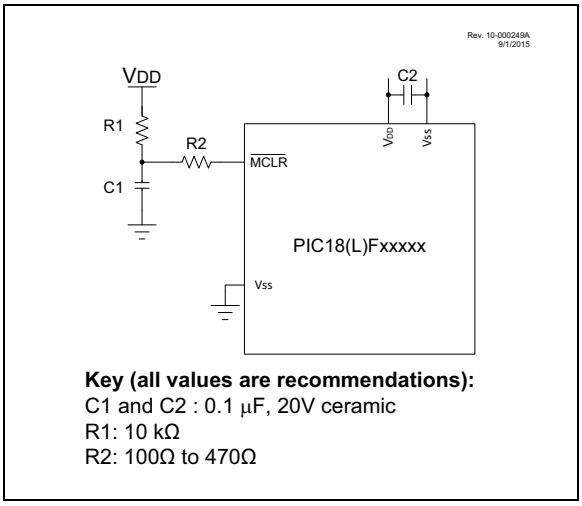
- PGC/PGD pins used for In-Circuit Serial Programming™ (ICSP™) and debugging purposes (see **Section 2.4 "ICSP™ Pins"**)
- OSCI and OSCO pins when an external oscillator source is used (see **Section 2.5 "External Oscillator Pins"**)

Additionally, the following pins may be required:

- VREF+/VREF- pins are used when external voltage reference for analog modules is implemented

The minimum mandatory connections are shown in Figure 2-1.

FIGURE 2-1: RECOMMENDED MINIMUM CONNECTIONS



Key (all values are recommendations):
C1 and C2 : 0.1 μF, 20V ceramic
R1: 10 kΩ
R2: 100Ω to 470Ω

2.2 Power Supply Pins

2.2.1 DECOUPLING CAPACITORS

The use of decoupling capacitors on every pair of power supply pins (VDD and VSS) is required.

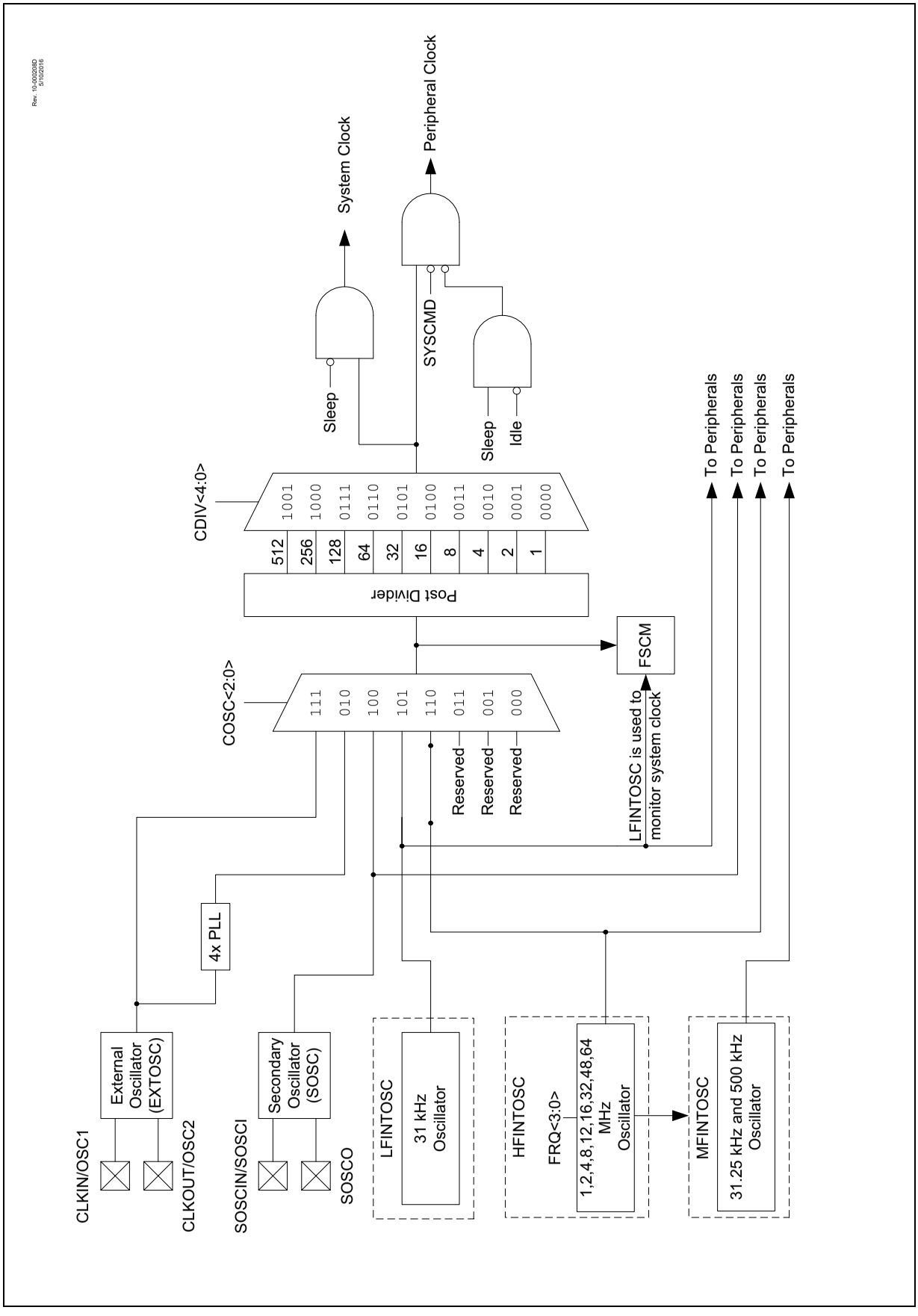
Consider the following criteria when using decoupling capacitors:

- **Value and type of capacitor:** A 0.1 μF (100 nF), 10-20V capacitor is recommended. The capacitor should be a low-ESR device, with a resonance frequency in the range of 200 MHz and higher. Ceramic capacitors are recommended.
- **Placement on the printed circuit board:** The decoupling capacitors should be placed as close to the pins as possible. It is recommended to place the capacitors on the same side of the board as the device. If space is constricted, the capacitor can be placed on another layer on the PCB using a via; however, ensure that the trace length from the pin to the capacitor is no greater than 0.25 inch (6 mm).
- **Handling high-frequency noise:** If the board is experiencing high-frequency noise (upward of tens of MHz), add a second ceramic type capacitor in parallel to the above described decoupling capacitor. The value of the second capacitor can be in the range of 0.01 μF to 0.001 μF. Place this second capacitor next to each primary decoupling capacitor. In high-speed circuit designs, consider implementing a decade pair of capacitances as close to the power and ground pins as possible (e.g., 0.1 μF in parallel with 0.001 μF).
- **Maximizing performance:** On the board layout from the power supply circuit, run the power and return traces to the decoupling capacitors first, and then to the device pins. This ensures that the decoupling capacitors are first in the power chain. Equally important is to keep the trace length between the capacitor and the power pins to a minimum, thereby reducing PCB trace inductance.

2.2.2 TANK CAPACITORS

On boards with power traces running longer than six inches in length, it is suggested to use a tank capacitor for integrated circuits, including microcontrollers, to supply a local power source. The value of the tank capacitor should be determined based on the trace resistance that connects the power supply source to the device, and the maximum current drawn by the device in the application. In other words, select the tank capacitor so that it meets the acceptable voltage sag at the device. Typical values range from 4.7 μF to 47 μF.

FIGURE 4-1: SIMPLIFIED PIC® MCU CLOCK SOURCE BLOCK DIAGRAM



4.3 Clock Source Types

External clock sources rely on external circuitry for the clock source to function. Examples are: oscillator modules (ECH, ECM, ECL mode), quartz crystal resonators or ceramic resonators (LP, XT and HS modes).

A 4x PLL is provided that can be used in conjunction with the external clock. See **Section 4.3.1.4 "4x PLL"** for more details.

Internal clock sources are contained within the oscillator module. The internal oscillator block has two internal oscillators that are used to generate internal system clock sources. The High-Frequency Internal Oscillator (HFINTOSC) can produce 1, 2, 4, 8, 12, 16, 32, 48 and 64 MHz clock. The frequency can be controlled through the OSCFRQ register (Register 4-5). The Low-Frequency Internal Oscillator (LFINTOSC) generates a fixed 31 kHz frequency.

The system clock can be selected between external or internal clock sources via the NOSC bits in the OSCCON1 register. See **Section 4.4 "Clock Switching"** for additional information. The system clock can be made available on the OSC2/CLKOUT pin for any of the modes that do not use the OSC2 pin. The clock out functionality is governed by the $\overline{\text{CLKOUTEN}}$ bit in the CONFIG1H register (Register 3-2). If enabled, the clock out signal is always at a frequency of FOSC/4.

4.3.1 EXTERNAL CLOCK SOURCES

An external clock source can be used as the device system clock by performing one of the following actions:

- Program the RSTOSC<2:0> and FEXTOSC<2:0> bits in the Configuration Words to select an external clock source that will be used as the default system clock upon a device Reset.
- Write the NOSC<2:0> and NDIV<3:0> bits in the OSCCON1 register to switch the system clock source.

See **Section 4.4 "Clock Switching"** for more information.

4.3.1.1 EC Mode

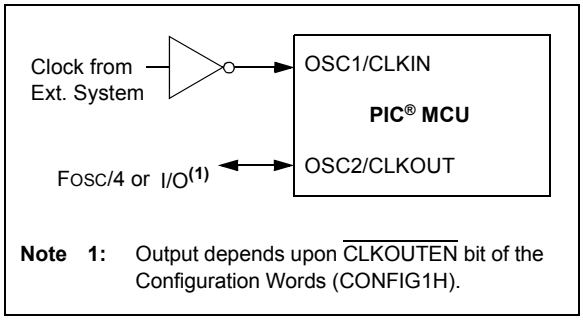
The External Clock (EC) mode allows an externally generated logic level signal to be the system clock source. When operating in this mode, an external clock source is connected to the OSC1 input. OSC2/CLKOUT is available for general purpose I/O or CLKOUT. Figure 4-2 shows the pin connections for EC mode.

EC mode has three power modes to select from through Configuration Words:

- ECH – High power, above 8 MHz
- ECM – Medium power, 100 kHz-8 MHz
- ECL – Low power, below 100 MHz

The Oscillator Start-up Timer (OST) is disabled when EC mode is selected. Therefore, there is no delay in operation after a Power-on Reset (POR) or wake-up from Sleep. Because the PIC® MCU design is fully static, stopping the external clock input will have the effect of halting the device while leaving all data intact. Upon restarting the external clock, the device will resume operation as if no time had elapsed.

FIGURE 4-2: EXTERNAL CLOCK (EC) MODE OPERATION



Note 1: Output depends upon $\overline{\text{CLKOUTEN}}$ bit of the Configuration Words (CONFIG1H).

4.3.1.2 LP, XT, HS Modes

The LP, XT and HS modes support the use of quartz crystal resonators or ceramic resonators connected to OSC1 and OSC2 (Figure 4-3). The three modes select a low, medium or high gain setting of the internal inverter-amplifier to support various resonator types and speed.

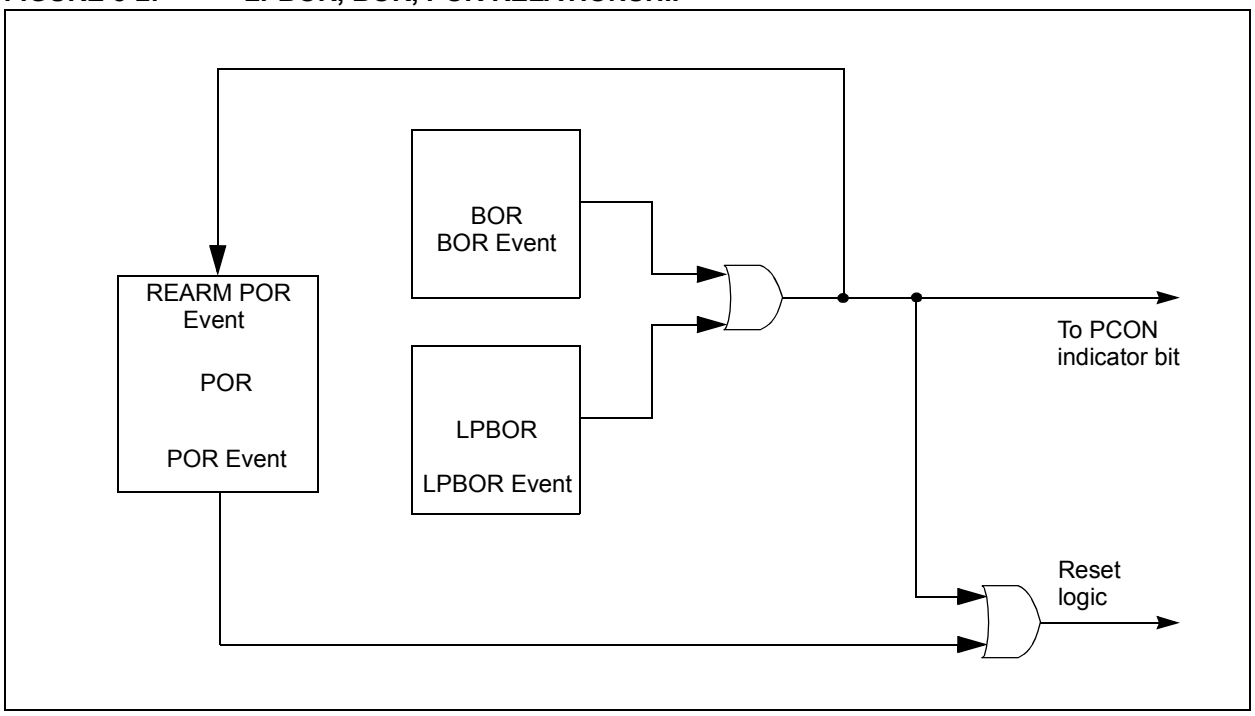
LP Oscillator mode selects the lowest gain setting of the internal inverter-amplifier. LP mode current consumption is the least of the three modes. This mode is designed to drive only 32.768 kHz tuning-fork type crystals (watch crystals).

XT Oscillator mode selects the intermediate gain setting of the internal inverter-amplifier. XT mode current consumption is the medium of the three modes. This mode is best suited to drive resonators with a medium drive level specification (above 100 kHz - 8 MHz).

HS Oscillator mode selects the highest gain setting of the internal inverter-amplifier. HS mode current consumption is the highest of the three modes. This mode is best suited for resonators that require a high drive setting (above 8 MHz).

Figure 4-3 and Figure 4-4 show typical circuits for quartz crystal and ceramic resonators, respectively.

FIGURE 8-2: LPBOR, BOR, POR RELATIONSHIP



8.1 Register Definitions: BOR Control

REGISTER 8-1: BORCON: BROWN-OUT RESET CONTROL REGISTER

R/W-1/u	U-0	U-0	U-0	U-0	U-0	U-0	R-q/u
SBOREN	—	—	—	—	—	—	BORRDY
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	q = Value depends on condition

bit 7 **SBOREN:** Software Brown-out Reset Enable bit
If BOREN ≠ 01:
SBOREN is read/write, but has no effect on the BOR.
If BOREN = 01:
1 = BOR Enabled
0 = BOR Disabled

bit 6-1 **Unimplemented:** Read as '0'

bit 0 **BORRDY:** Brown-out Reset Circuit Ready Status bit
1 = The Brown-out Reset Circuit is active and armed
0 = The Brown-out Reset Circuit is disabled or is warming up

EXAMPLE 11-4: WRITING TO PROGRAM FLASH MEMORY (CONTINUED)

```
WRITE_BYTE_TO_HREGS
             MOVF     POSTINC0, W              ; get low byte of buffer data
             MOVWF    TABLAT                   ; present data to table latch
             TBLWT+*                           ; write data, perform a short write
                                               ; to internal TBLWT holding register.
             DECFSZ   COUNTER                  ; loop until holding registers are full
             BRA      WRITE_WORD_TO_HREGS
PROGRAM_MEMORY
             BCF      NVMCON1, NVMREG0         ; point to Program Flash Memory
             BSF      NVMCON1, NVMREG1         ; point to Program Flash Memory
             BSF      NVMCON1, WREN            ; enable write to memory
             BCF      NVMCON1, FREE            ; enable write to memory
             BCF      INTCON, GIE              ; disable interrupts
             MOVLW    55h
Required     MOVWF    NVMCON2                  ; write 55h
Sequence     MOVLW    0AAh
             MOVWF    NVMCON2                  ; write 0AAh
             BSF      NVMCON1, WR              ; start program (CPU stall)
             DCFSZ    COUNTER2                 ; repeat for remaining write blocks
             BRA      WRITE_BYTE_TO_HREGS
             BSF      INTCON, GIE              ; re-enable interrupts
             BCF      NVMCON1, WREN            ; disable write to memory
```

REGISTER 14-19: PIE7: PERIPHERAL INTERRUPT ENABLE REGISTER 7

U-0	U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
—	—	—	CCP5IE	CCP4IE	CCP3IE	CCP2IE	CCP1IE
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-5 **Unimplemented:** Read as '0'

bit 4 **CCP5IE:** ECCP5 Interrupt Enable bit
1 = Enabled
0 = Disabled

bit 3 **CCP4IE:** ECCP4 Interrupt Enable bit
1 = Enabled
0 = Disabled

bit 2 **CCP3IE:** ECCP3 Interrupt Enable bit
1 = Enabled
0 = Disabled

bit 1 **CCP2IE:** ECCP2 Interrupt Enable bit
1 = Enabled
0 = Disabled

bit 0 **CCP1IE:** ECCP1 Interrupt Enable bit
1 = Enabled
0 = Disabled

REGISTER 14-27: IPR5: PERIPHERAL INTERRUPT PRIORITY REGISTER 5

R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1
TMR8IP	TMR7IP	TMR6IP	TMR5IP	TMR4IP	TMR3IP	TMR2IP	TMR1IP
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **TMR8IP:** TMR8 to PR8 Match Interrupt Priority bit
1 = High priority
0 = Low priority

bit 6 **TMR7IP:** TMR7 to PR7 Match Interrupt Priority bit
1 = High priority
0 = Low priority

bit 5 **TMR6IP:** TMR6 to PR6 Match Interrupt Priority bit
1 = High priority
0 = Low priority

bit 4 **TMR5IP:** TMR5 to PR5 Match Interrupt Priority bit
1 = High priority
0 = Low priority

bit 3 **TMR4IP:** TMR4 to PR4 Match Interrupt Priority bit
1 = High priority
0 = Low priority

bit 2 **TMR3IP:** TMR3 to PR3 Match Interrupt Priority bit
1 = High priority
0 = Low priority

bit 1 **TMR2IP:** TMR2 to PR2 Match Interrupt Priority bit
1 = High priority
0 = Low priority

bit 0 **TMR1IP:** TMR1 to PR1 Match Interrupt Priority bit
1 = High priority
0 = Low priority

TABLE 14-1: SUMMARY OF REGISTERS ASSOCIATED WITH INTERRUPTS

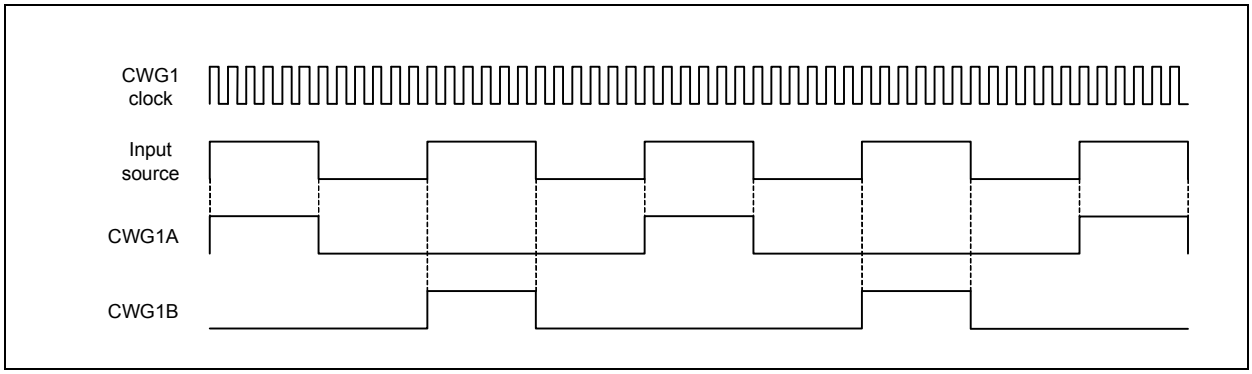
Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
INTCON	GIE/GIEH	PEIE/GIEL	IPEN	—	INT3EDG	INT2EDG	INT1EDG	INT0EDG	173
PIE0	—	—	TMR0IE	IOCIE	INT3IE	INT2IE	INT1IE	INT0IE	185
PIE1	OSCFIE	CSWIE	—	—	—	—	ADTIE	ADIE	186
PIE2	HLVDIE	ZCDIE	—	—	—	C3IE	C2IE	C1IE	187
PIE3	RC2IE	TX2IE	RC1IE	TX1IE	BCL2IE	SSP2IE	BCL1IE	SSP1IE	188
PIE4	—	—	RC5IE	TX5IE	RC4IE	TX4IE	RC3IE	TX3IE	189
PIE5	TMR8IE	TMR7IE	TMR6IE	TMR5IE	TMR4IE	TMR3IE	TMR2IE	TMR1IE	190
PIE6	—	—	—	—	TMR7GIE	TMR5GIE	TMR3GIE	TMR1GIE	191
PIE7	—	—	—	CCP5IE	CCP4IE	CCP3IE	CCP2IE	CCP1IE	192
PIE8	SCANIE	CRCIE	NVMIE	—	—	—	—	CWG1IE	193
PIE9	—	—	SMT2PWAIE	SMT2PRAIE	SMT2IE	SMT1PWAIE	SMT1PRAIE	SMT1IE	194
PIR0	—	—	TMR0IF	IOCIF	INT3IF	INT2IF	INT1IF	INT0IF	174
PIR1	OSCFIF	CSWIF	—	—	—	—	ADTIF	ADIF	175
PIR2	HLVDIF	ZCDIF	—	—	—	C3IF	C2IF	C1IF	176
PIR3	RC2IF	TX2IF	RC1IF	TX1IF	BCL2IF	SSP2IF	BCL1IF	SSP1IF	177
PIR4	—	—	RC5IF	TX5IF	RC4IF	TX4IF	RC3IF	TX3IF	178
PIR5	TMR8IF	TMR7IF	TMR6IF	TMR5IF	TMR4IF	TMR3IF	TMR2IF	TMR1IF	179
PIR6	—	—	—	—	TMR7GIF	TMR5GIF	TMR3GIF	TMR1GIF	180
PIR7	—	—	—	CCP5IF	CCP4IF	CCP3IF	CCP2IF	CCP1IF	181
PIR8	SCANIF	CRCIF	NVMIF	—	—	—	—	CWG1IF	183
PIR9	—	—	SMT2PWAIF	SMT2PRAIF	SMT2IF	SMT1PWAIF	SMT1PRAIF	SMT1IF	184
IPR0	—	—	TMR0IP	IOCIP	INT3IP	INT2IP	INT1IP	INT0IP	195
IPR1	OSCFIP	CSWIP	—	—	—	—	ADTIP	ADIP	196
IPR2	HLVDIP	ZCDIP	—	—	—	C3IP	C2IP	C1IP	197
IPR3	RC2IP	TX2IP	RC1IP	TX1IP	BCL2IP	SSP2IP	BCL1IP	SSP1IP	198
IPR4	—	—	RC5IP	TX5IP	RC4IP	TX4IP	RC3IP	TX3IP	199
IPR5	TMR8IP	TMR7IP	TMR6IP	TMR5IP	TMR4IP	TMR3IP	TMR2IP	TMR1IP	200
IPR6	—	—	—	—	TMR7GIP	TMR5GIP	TMR3GIP	TMR1GIP	201
IPR7	—	—	—	CCP5IP	CCP4IP	CCP3IP	CCP2IP	CCP1IP	202
IPR8	SCANIP	CRCIP	NVMIP	—	—	—	—	CWG1IP	203
IPR9	—	—	SMT2PWAIP	SMT2PRAIP	SMT2IP	SMT1PWAIP	SMT1PRAIP	SMT1IP	204

Legend: — = unimplemented locations, read as '0'. Shaded bits are not used for Interrupts.

TABLE 17-1: PPS INPUT REGISTER DETAILS (CONTINUED)

Peripheral	PPS Input Register	Default Pin Selection at POR	Register Reset Value at POR	Input Available from Selected PORTx							
EUSART3 Transmit	TX3PPS	RE0	0x20	—	B	—	—	E	—	—	—
EUSART4 Receive	RX4PPS	RC1	0x11	—	B	C	—	—	—	—	—
EUSART4 Transmit	TX4PPS	RC0	0x10	—	B	C	—	—	—	—	—
EUSART5 Receive	RX5PPS	RE3	0x23	—	—	—	—	E	—	G	—
EUSART5 Transmit	TX5PPS	RE2	0x22	—	—	—	—	E	—	G	—
MSSP1 Clock	SSP1CLKPPS	RC3	0x13	—	B	C	—	—	—	—	—
MSSP1 Data	SSP1DATPPS	RC4	0x14	—	B	C	—	—	—	—	—
MSSP1 Slave Select	SSP1SSPPS	RF7	0x2F	—	B	—	—	—	F	—	—
MSSP2 Clock	SSP2CLKPPS	RD6	0x1E	—	B	—	D	—	—	—	—
MSSP2 Data	SSP2DATPPS	RD5	0x1D	—	B	—	D	—	—	—	—
MSSP2 Slave Select	SSP2SSPPS	RD7	0x1F	—	B	—	D	—	—	—	—

FIGURE 24-4: CWG1 PUSH-PULL MODE OPERATION



24.2.3 FULL-BRIDGE MODES

In Forward and Reverse Full-Bridge modes, three outputs drive static values while the fourth is modulated by the input data signal. The mode selection may be toggled between forward and reverse by toggling the MODE<0> bit of the CWG1CON0 while keeping MODE<2:1> static, without disabling the CWG module. When connected as shown in Figure 24-5, the outputs are appropriate for a full-bridge motor driver. Each CWG output signal has independent polarity control, so the circuit can be adapted to high-active and low-active drivers. A simplified block diagram for the Full-Bridge modes is shown in Figure 24-6.

FIGURE 24-5: EXAMPLE OF FULL-BRIDGE APPLICATION

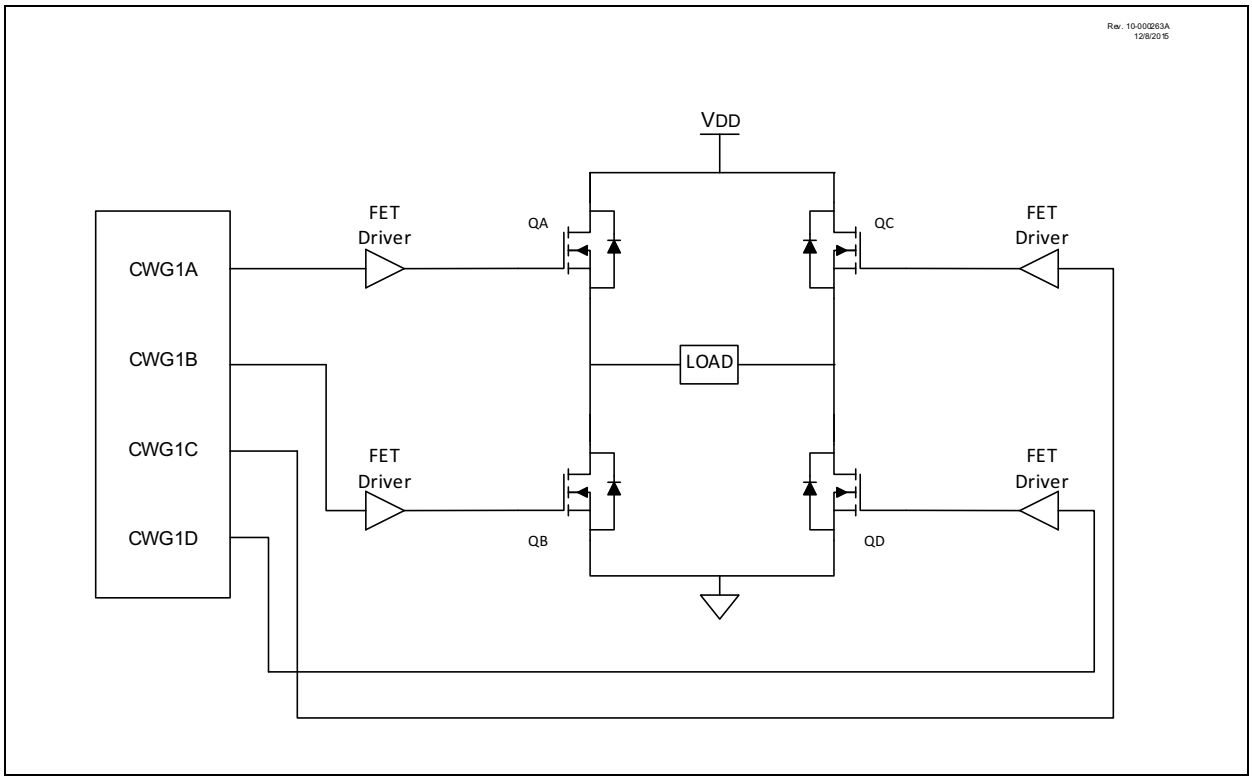


TABLE 25-2: SUMMARY OF REGISTERS ASSOCIATED WITH SMTx

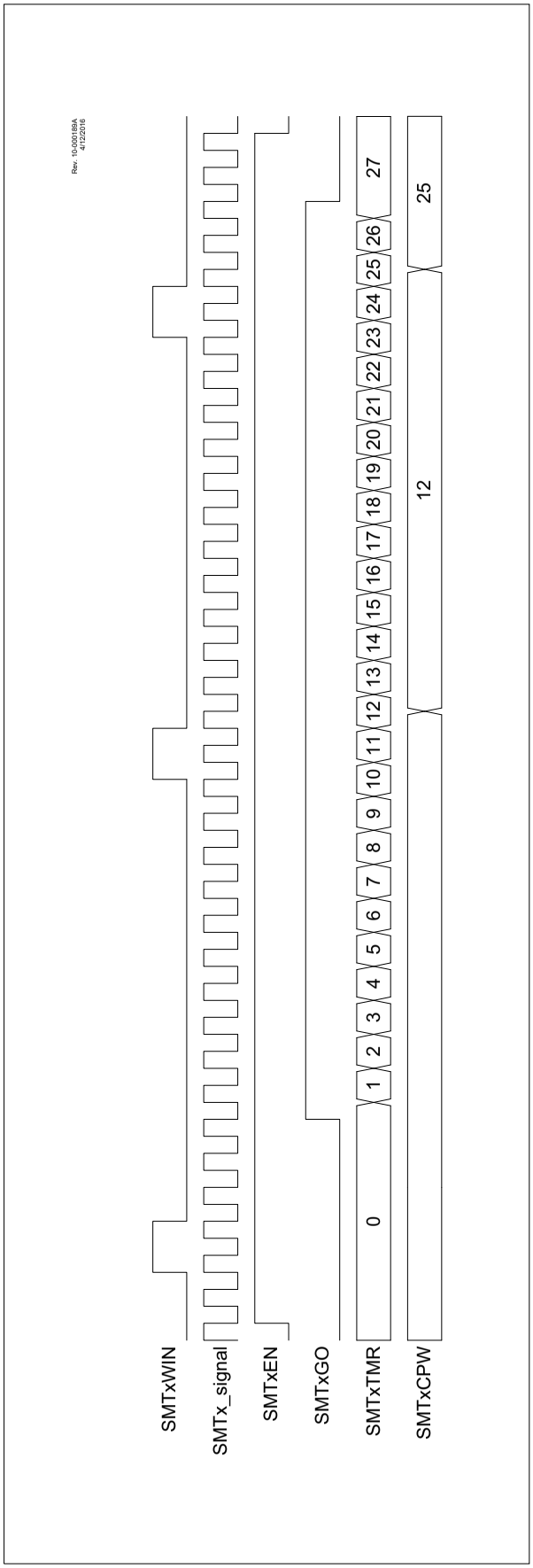
Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
PIE9	—	—	SMT2PWAIE	SMT2PRAIE	SMT2IE	SMT1PWAIE	SMT1PRAIE	SMT1IE	189
PIR9	—	—	SMT2PWAIF	SMT2PRAIF	SMT2IF	SMT1PWAIF	SMT1PRAIF	SMT1IF	176
IPR9	—	—	SMT2PWAIP	SMT2PRAIP	SMT2IP	SMT1PWAIP	SMT1PRAIP	SMT1IP	201
SMT1CLK	—	—	—	—	—	CSEL<2:0>			340
SMT1CON0	EN	—	STP	WPOL	SPOL	CPOL	SMT1PS<1:0>		337
SMT1CON1	SMT1GO	REPEAT	—	—	MODE<3:0>				338
SMT1CPRH	SMT1CPR<15:8>								344
SMT1CPRL	SMT1CPR<7:0>								344
SMT1CPRU	SMT1CPR<23:16>								344
SMT1CPWH	SMT1CPW<15:8>								345
SMT1CPWL	SMT1CPW<7:0>								345
SMT1CPWU	SMT1CPW<23:16>								345
SMT1PRH	SMT1PR<15:8>								346
SMT1PRL	SMT1PR<7:0>								346
SMT1PRU	SMT1PR<23:16>								346
SMT1SIG	—	—	—	SSEL<4:0>					342
SMT1STAT	CPRUP	CPWUP	RST	—	—	TS	WS	AS	339
SMT1TMRH	SMT1TMR<15:8>								343
SMT1TMRL	SMT1TMR<7:0>								343
SMT1TMRU	SMT1TMR<23:16>								343
SMT1WIN	—	—	—	WSEL<4:0>					341
SMT2CLK	—	—	—	—	—	CSEL<2:0>			340
SMT2CON0	EN	—	STP	WPOL	SPOL	CPOL	SMT2PS<1:0>		337
SMT2CON1	SMT2GO	REPEAT	—	—	MODE<3:0>				338
SMT2CPRH	SMT2CPR<15:8>								344
SMT2CPRL	SMT2CPR<7:0>								344
SMT2CPRU	SMT2CPR<23:16>								344
SMT2CPWH	SMT2CPW<15:8>								345
SMT2CPWL	SMT2CPW<7:0>								345
SMT2CPWU	SMT2CPW<23:16>								345
SMT2PRH	SMT2PR<15:8>								346
SMT2PRL	SMT2PR<7:0>								346
SMT2PRU	SMT2PR<23:16>								346
SMT2SIG	—	—	—	SSEL<4:0>					342
SMT2STAT	CPRUP	CPWUP	RST	—	—	TS	WS	AS	339
SMT2TMRH	SMT2TMR<15:8>								343
SMT2TMRL	SMT2TMR<7:0>								343
SMT2TMRU	SMT2TMR<23:16>								343
SMT2WIN	—	—	—	WSEL<4:0>					340

Legend: x = unknown, u = unchanged, – = unimplemented read as '0', q = value depends on condition. Shaded cells are not used for SMTx module.

25.7.7 TIME OF FLIGHT MEASURE MODE

This mode measures the time interval between a rising edge on the SMTWINx input and a rising edge on the SMTx_signal input, beginning to increment the timer upon observing a rising edge on the SMTWINx input, while updating the SMTxCPR register and resetting the timer upon observing a rising edge on the SMTx_signal input. In the event of two SMTWINx rising edges without an SMTx_signal rising edge, it will update the SMTxCPW register with the current value of the timer and reset the timer value. See Figure 25-14 and Figure 25-15.

FIGURE 25-18: COUNTER MODE TIMING DIAGRAM



27.5.5 SPI OPERATION IN SLEEP MODE

In SPI Master mode, module clocks may be operating at a different speed than when in Full-Power mode; in the case of the Sleep mode, all clocks are halted.

Special care must be taken by the user when the MSSP clock is much faster than the system clock.

In Slave mode, when MSSP interrupts are enabled, after the master completes sending data, an MSSP interrupt will wake the controller from Sleep.

If an exit from Sleep mode is not desired, MSSP interrupts should be disabled.

In SPI Master mode, when the Sleep mode is selected, all module clocks are halted and the transmission/reception will remain in that state until the device wakes. After the device returns to Run mode, the module will resume transmitting and receiving data.

In SPI Slave mode, the SPI Transmit/Receive Shift register operates asynchronously to the device. This allows the device to be placed in Sleep mode and data to be shifted into the SPI Transmit/Receive Shift register. When all eight bits have been received, the MSSP interrupt flag bit will be set and if enabled, will wake the device.

TABLE 27-1: SUMMARY OF REGISTERS ASSOCIATED WITH SPI OPERATION

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
INTCON	GIE/GIEH	PEIE/GIEL	IPEN	—	INT3EDG	INT2EDG	INT1EDG	INT0EDG	173
PIE3	RC2IE	TX2IE	RC1IE	TX1IE	BCL2IE	SSP2IE	BCL1IE	SSP1IE	188
PIR3	RC2IF	TX2IF	RC1IF	TX1IF	BCL2IF	SSP2IF	BCL1IF	SSP1IF	177
IPR3	RC2IP	TX2IP	RC1IP	TX1IP	BCL2IP	SSP2IP	BCL1IP	SSP1IP	198
RxyPPS	—	—	RxyPPS<5:0>						228
SSPxBUF	BUF<7:0>								392*
SSPxCLKPPS	—	—	SSPxCLKPPS<<5:0>						225
SSPxCON1	WCOL	SSPOV	SSPEN	CKP	SSPM<3:0>				394
SSPxCON3	ACKTIM	PCIE	SCIE	BOEN	SDAHT	SBCDE	AHEN	DHEN	395
SSPxDATPPS	—	—	SSPDATPPS<5:0>						225
SSPxSSPPS	—	—	SSPSSPPS<5:0>						225
SSPxSTAT	SMP	CKE	D/$\overline{A}$	P	S	R/$\overline{W}$	UA	BF	409

Legend: — = Unimplemented location, read as '0'. Shaded cells are not used by the MSSP in SPI mode.
* Page provides register information.

28.2.2.8 Asynchronous Reception Setup:

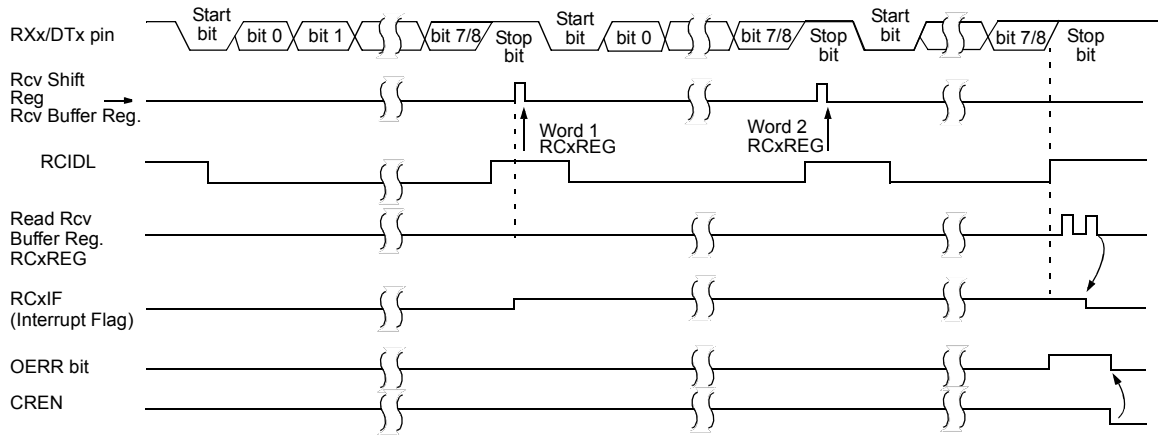
1. Initialize the SPxBRGH:SPxBRGL register pair and the BRGH and BRG16 bits to achieve the desired baud rate (see **Section 28.4 "EUSART Baud Rate Generator (BRG)"**).
2. Clear the ANSEL bit for the RXx pin (if applicable).
3. Enable the serial port by setting the SPEN bit. The SYNC bit must be clear for asynchronous operation.
4. If interrupts are desired, set the RCxIE bit of the PIE3/4 registers and the GIE and PEIE bits of the INTCON register.
5. If 9-bit reception is desired, set the RX9 bit.
6. Enable reception by setting the CREN bit.
7. The RCxIF interrupt flag bit will be set when a character is transferred from the RSR to the receive buffer. An interrupt will be generated if the RCxIE interrupt enable bit was also set.
8. Read the RCxSTA register to get the error flags and, if 9-bit data reception is enabled, the ninth data bit.
9. Get the received eight Least Significant data bits from the receive buffer by reading the RCxREG register.
10. If an overrun occurred, clear the OERR flag by clearing the CREN receiver enable bit.

28.2.2.9 9-Bit Address Detection Mode Setup

This mode would typically be used in RS-485 systems. To set up an Asynchronous Reception with Address Detect Enable:

1. Initialize the SPxBRGH:SPxBRGL register pair and the BRGH and BRG16 bits to achieve the desired baud rate (see **Section 28.4 "EUSART Baud Rate Generator (BRG)"**).
2. Clear the ANSEL bit for the RXx pin (if applicable).
3. Enable the serial port by setting the SPEN bit. The SYNC bit must be clear for asynchronous operation.
4. If interrupts are desired, set the RCxIE bit of the PIE3/4 registers and the GIE and PEIE bits of the INTCON register.
5. Enable 9-bit reception by setting the RX9 bit.
6. Enable address detection by setting the ADDEN bit.
7. Enable reception by setting the CREN bit.
8. The RCxIF interrupt flag bit will be set when a character with the ninth bit set is transferred from the RSR to the receive buffer. An interrupt will be generated if the RCxIE interrupt enable bit was also set.
9. Read the RCxSTA register to get the error flags. The ninth data bit will always be set.
10. Get the received eight Least Significant data bits from the receive buffer by reading the RCxREG register. Software determines if this is the device's address.
11. If an overrun occurred, clear the OERR flag by clearing the CREN receiver enable bit.
12. If the device has been addressed, clear the ADDEN bit to allow all received data into the receive buffer and generate interrupts.

FIGURE 28-5: ASYNCHRONOUS RECEPTION



Note: This timing diagram shows three words appearing on the RXx input. The RCxREG (receive buffer) is read after the third word, causing the OERR (overrun) bit to be set.

31.0 5-BIT DIGITAL-TO-ANALOG CONVERTER (DAC) MODULE

The Digital-to-Analog Converter supplies a variable voltage reference, ratiometric with the input source, with 32 selectable output levels.

The positive input source (VSOURCE+) of the DAC can be connected to:

- FVR Buffer
- External VREF+ pin
- VDD supply voltage

The negative input source (VSOURCE-) of the DAC can be connected to:

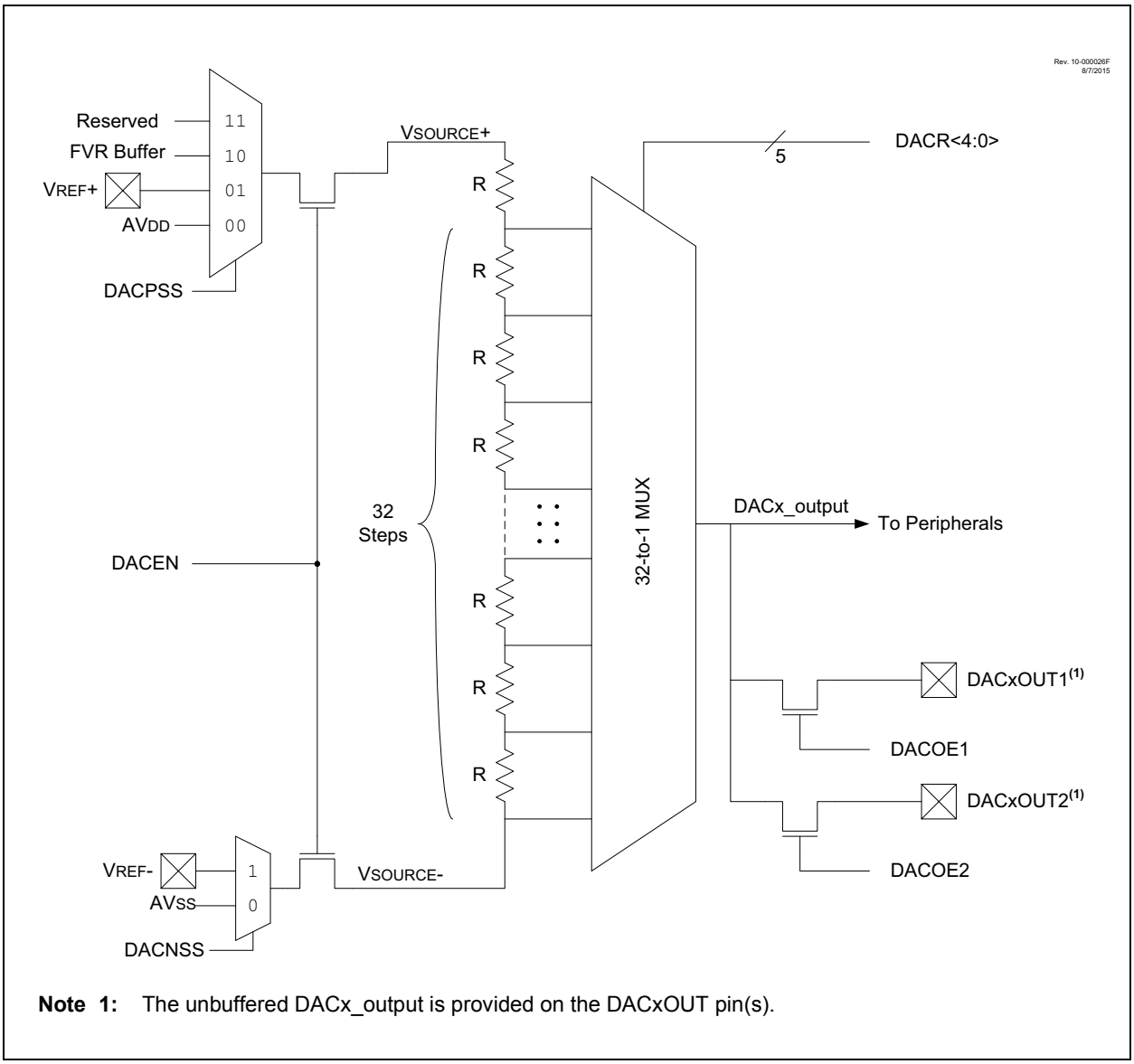
- External VREF- pin
- Vss

The output of the DAC (DACx_output) can be selected as a reference voltage to the following:

- Comparator positive input
- ADC input channel
- DACxOUT1 pin
- DACxOUT2 pin

The Digital-to-Analog Converter (DAC) can be enabled by setting the DACEN bit of the DAC1CON0 register.

FIGURE 31-1: DIGITAL-TO-ANALOG CONVERTER BLOCK DIAGRAM



Note 1: The unbuffered DACx_output is provided on the DACxOUT pin(s).

32.3 ADC Acquisition Requirements

For the ADC to meet its specified accuracy, the charge holding capacitor (CHOLD) must be allowed to fully charge to the input channel voltage level. The Analog Input model is shown in Figure 32-4. The source impedance (RS) and the internal sampling switch (RSS) impedance directly affect the time required to charge the capacitor CHOLD. The sampling switch (RSS) impedance varies over the device voltage (VDD), refer to Figure 32-4. **The maximum recommended impedance for analog sources is 10 kΩ.** As the source impedance is decreased, the acquisition time may be decreased. After the analog input channel is selected (or changed), an ADC acquisition must be completed before the conversion can be started. To calculate the minimum acquisition time, Equation 32-1 may be used. This equation assumes that 1/2 LSb error is used (1,024 steps for the ADC). The 1/2 LSb error is the maximum error allowed for the ADC to meet its specified resolution.

EQUATION 32-1: ACQUISITION TIME EXAMPLE

Assumptions: $Temperature = 50°C$ *and external impedance of* $10k\Omega$ *5.0V* V_{DD}

$$T_{ACQ} = \text{Amplifier Settling Time} + \text{Hold Capacitor Charging Time} + \text{Temperature Coefficient}$$
$$= T_{AMP} + T_C + T_{COFF}$$
$$= 2\mu s + T_C + [(Temperature - 25°C)(0.05\mu s/°C)]$$

The value for T_C *can be approximated with the following equations:*

$$V_{APPLIED}\left(1 - \frac{1}{(2^{n+1}) - 1}\right) = V_{CHOLD}$$;[1] V_{CHOLD} *charged to within 1/2 lsb*

$$V_{APPLIED}\left(1 - e^{\frac{-T_C}{RC}}\right) = V_{CHOLD}$$;[2] V_{CHOLD} *charge response to* $V_{APPLIED}$

$$V_{APPLIED}\left(1 - e^{\frac{-T_C}{RC}}\right) = V_{APPLIED}\left(1 - \frac{1}{(2^{n+1}) - 1}\right)$$;*combining [1] and [2]*

Note: Where n = number of bits of the ADC.

Solving for T_C*:*

$$T_C = -C_{HOLD}(R_{IC} + R_{SS} + R_S)\ ln(1/2047)$$
$$= -10pF(1k\Omega + 7k\Omega + 10k\Omega)\ ln(0.0004885)$$
$$= 1.37\mu s$$

Therefore:

$$T_{ACQ} = 2\mu s + 892ns + [(50°C - 25°C)(0.05\mu s/°C)]$$
$$= 4.62\mu s$$

Note 1: The reference voltage (VREF) has no effect on the equation, since it cancels itself out.

2: The charge holding capacitor (CHOLD) is not discharged after each conversion.

3: The maximum recommended impedance for analog sources is 10 kΩ. This is required to meet the pin leakage specification.

TABLE 32-5: SUMMARY OF REGISTERS ASSOCIATED WITH ADC

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
INTCON	GIE/GIEH	PEIE/GIEL	IPEN	—	INT3EDG	INT2EDG	INT1EDG	INT0EDG	173
PIE1	OSCFIE	CSWIE	—	—	—	—	ADTIE	ADIE	186
PIR1	OSCFIF	CSWIF	—	—	—	—	ADTIF	ADIF	175
ADCON0	ADON	ADCON	–	ADCS	–	ADFM	–	ADGO	504
ADCON1	ADPPOL	ADIPEN	ADGPOL	—	—	—	—	ADDSEN	505
ADCON2	ADPSIS	ADCRS<2:0>			ADACLR	ADMD<2:0>			506
ADCON3	–	ADCALC<2:0>			ADSOI	ADTMD<2:0>			507
ADACT	—	—	—	—	ADACT<4:0>				506
ADRESH	ADRESH<7:0>								514, 514
ADRESL	ADRESL<7:0>								514, 515
ADPREVH	ADPREV<15:8>								515
ADPREVL	ADPREV<7:0>								516
ADACCH	ADACC<15:8>								516
ADACCL	ADACC<7:0>								516
ADSTPTH	ADSTPT<15:8>								517
ADSTPT	ADSTPT<7:0>								517
ADERRL	ADERR<7:0>								518
ADLTHH	ADLTH<15:8>								518
ADLTHL	ADLTH<7:0>								518
ADUTHH	ADUTH<15:8>								519
ADUTHL	ADUTH<7:0>								519
ADSTAT	ADAOV	ADUTHR	ADLTHR	ADMATH	ADSTAT<3:0>				508
ADCLK	—	—	ADCS<5:0>						509
ADREF	—	—	—	ADNREF	—	—	ADPREF<1:0>		509
ADPCH	—	—	ADPCH<5:0>						510
ADPRE	ADPRE<7:0>								511
ADACQ	ADACQ<7:0>								511
ADCAP	—	—	—	ADCAP<4:0>					512
ADRPT	ADRPT<7:0>								512
ADCNT	ADCNT<7:0>								513
ADFLTRH	ADFLTR<15:8>								513
ADFLTRL	ADFLTR<7:0>								513
FVRCON	FVREN	FVRRDY	TSEN	TSRNG	CDAFVR<1:0>		ADFVR<1:0>		479
DAC1CON1	—	—	—	DAC1R<4:0>					485
OSCSTAT	EXTOR	HFOR	MFOR	LFOR	SOR	ADOR	—	PLLR	37

Legend: – = unimplemented read as '0'. Shaded cells are not used for the ADC module.

34.0 HIGH/LOW-VOLTAGE DETECT (HLVD)

The PIC18(L)F6xK40 of devices has a High/Low-Voltage Detect module (HLVD). This is a programmable circuit that sets both a device voltage trip point and the direction of change from that point (positive going, negative going or both). If the device experiences an excursion past the trip point in that direction, an interrupt flag is set. If the interrupt is enabled, the program execution branches to the interrupt vector address and the software responds to the interrupt.

Complete control of the HLVD module is provided through the HLVDCON0 and HLVDCON1 register. This allows the circuitry to be “turned off” by the user under software control, which minimizes the current consumption for the device.

The module’s block diagram is shown in Figure 34-1.

Since the HLVD can be software enabled through the HLVDEN bit, setting and clearing the enable bit does not produce a false HLVD event glitch. Each time the HLVD module is enabled, the circuitry requires some time to stabilize. The RDY bit (HLVDCON0<4>) is a read-only bit used to indicate when the band gap reference voltages are stable.

The module can only generate an interrupt after the module is turned ON and the band gap reference voltages are ready.

The HLVDINTH and HLVDINTL bits determine the overall operation of the module. When HLVDINTH is set, the module monitors for rises in VDD above the trip point set by the HLVDCON1 register. When HLVDINTL is set, the module monitors for drops in VDD below the trip point set by the HLVDCON1 register. When both the HLVDINTH and HLVDINTL bits are set, any changes above or below the trip point set by the HLVDCON1 register can be monitored.

The OUT bit can be read to determine if the voltage is greater than or less than the voltage level selected by the HLVDCON1 register.

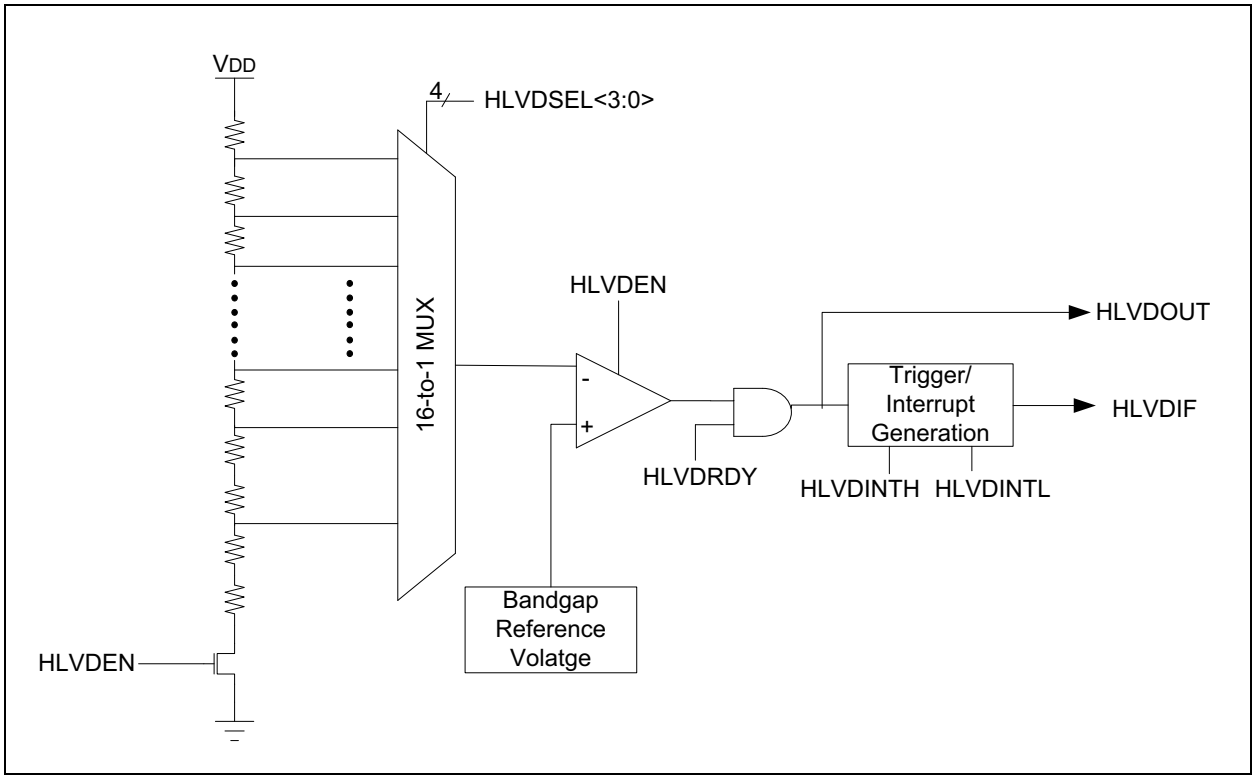
34.1 Operation

When the HLVD module is enabled, a comparator uses an internally generated voltage reference as the set point. The set point is compared with the trip point, where each node in the resistor divider represents a trip point voltage. The “trip point” voltage is the voltage level at which the device detects a high or low-voltage event, depending on the configuration of the module.

When the supply voltage is equal to the trip point, the voltage tapped off of the resistor array is equal to the internal reference voltage generated by the voltage reference module. The comparator then generates an interrupt signal by setting the HLVDIF bit.

The trip point voltage is software programmable to any of 16 values. The trip point is selected by programming the HLVDSEL<3:0> bits (HLVDCON1<3:0>).

FIGURE 34-1: HLVD MODULE BLOCK DIAGRAM



38.3 DC Characteristics

TABLE 38-1: SUPPLY VOLTAGE

PIC18LF65/66K40			Standard Operating Conditions (unless otherwise stated)				
PIC18F65/66K40							
Param. No.	Sym.	Characteristic	Min.	Typ.†	Max.	Units	Conditions
Supply Voltage							
D002	VDD		1.8 2.5 3.0	— — —	3.6 3.6 3.6	V V V	FOSC ≤ 16 MHz FOSC > 16 MHz FOSC > 32 MHz
D002	VDD		2.3 2.5 3.0	— — —	5.5 5.5 5.5	V V V	FOSC ≤ 16 MHz FOSC > 16 MHz FOSC > 32 MHz
RAM Data Retention(1)							
D003	VDR		1.5	—	—	V	Device in Sleep mode
D003	VDR		1.7	—	—	V	Device in Sleep mode
Power-on Reset Release Voltage(2)							
D004	VPOR		—	1.6	—	V	BOR or LPBOR disabled(3)
D004	VPOR		—	1.6	—	V	BOR or LPBOR disabled(3)
Power-on Reset Rearm Voltage(2)							
D005	VPORR		—	0.8	—	V	BOR or LPBOR disabled(3)
D005	VPORR		—	1.5	—	V	BOR or LPBOR disabled(3)
VDD Rise Rate to ensure internal Power-on Reset signal(2)							
D006	SVDD		0.05	—	—	V/ms	BOR or LPBOR disabled(3)
D006	SVDD		0.05	—	—	V/ms	BOR or LPBOR disabled(3)

† Data in "Typ." column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered in Sleep mode without losing RAM data.

2: See Figure 38-3, POR and POR REARM with Slow Rising VDD.

3: Please see Table 38-11 for BOR and LPBOR trip point information.