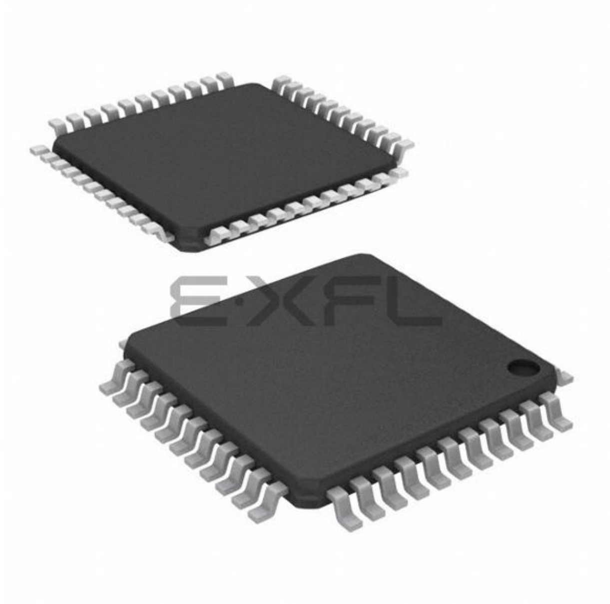

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	S08
Core Size	8-Bit
Speed	20MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	37
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 12x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LQFP
Supplier Device Package	44-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc9s08pa32avld

- Input/Output
  - Up to 57 GPIOs including one output-only pin
  - Two 8-bit keyboard interrupt modules (KBI)
  - Two true open-drain output pins
  - Eight, ultra-high current sink pins supporting 20 mA source/sink current
- Package options
  - 64-pin LQFP; 64-pin QFP
  - 48-pin LQFP
  - 44-pin LQFP
  - 32-pin LQFP

Table of Contents

4 Ratings

4.1 Thermal handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
T_{STG}	Storage temperature	–55	150	°C	1
T_{SDR}	Solder temperature, lead-free	—	260	°C	2

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

4.2 Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	—	3	—	1

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

4.3 ESD handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
V_{HBM}	Electrostatic discharge voltage, human body model	-6000	+6000	V	1
V_{CDM}	Electrostatic discharge voltage, charged-device model	-500	+500	V	2
I_{LAT}	Latch-up current at ambient temperature of 105°C	-100	+100	mA	

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
2. Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.

4.4 Voltage and current operating ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the limits specified in below table may affect device reliability or cause permanent damage to the device. For functional operating conditions, refer to the remaining tables in this document.

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for instance, either V_{SS} or V_{DD}) or the programmable pullup resistor associated with the pin is enabled.

Symbol	Description	Min.	Max.	Unit
V_{DD}	Supply voltage	–0.3	6.0	V
I_{DD}	Maximum current into V_{DD}	—	120	mA
V_{DIO}	Digital input voltage (except $\overline{\text{RESET}}$, EXTAL, XTAL, or true open drain pin PTA2 and PTA3)	–0.3	V_{DD} + 0.3	V
	Digital input voltage (true open drain pin PTA2 and PTA3)	-0.3	6	V
V_{AIO}	Analog[1], $\overline{\text{RESET}}$, EXTAL, and XTAL input voltage	–0.3	V_{DD} + 0.3	V
I_D	Instantaneous maximum current single pin limit (applies to all port pins)	–25	25	mA
V_{DDA}	Analog supply voltage	V_{DD} – 0.3	V_{DD} + 0.3	V

1. All digital I/O pins, except open-drain pin PTA2 and PTA3, are internally clamped to V_{SS} and V_{DD}. PTA2 and PTA3 is only clamped to V_{SS}.

5 General

5.1 Nonswitching electrical specifications

5.1.1 DC characteristics

This section includes information about power supply requirements and I/O pin characteristics.

Table 2. DC characteristics

Symbol	C	Descriptions			Min	Typical[1]	Max	Unit
—	—	Operating voltage		—	2.7	—	5.5	V
V_{OH}	P	Output high voltage	All I/O pins, standard-drive strength	5 V, I_{load} = -5 mA	V_{DD} - 0.8	—	—	V
	C			3 V, I_{load} = -2.5 mA	V_{DD} - 0.8	—	—	V
	P		High current drive pins, high-drive strength[2]	5 V, I_{load} = -20 mA	V_{DD} - 0.8	—	—	V
	C			3 V, I_{load} = -10 mA	V_{DD} - 0.8	—	—	V

Table continues on the next page...

Table 2. DC characteristics (continued)

Symbol	C	Descriptions			Min	Typical[1]	Max	Unit
I_{OHT}	D	Output high current	Max total I_{OH} for all ports	5 V	—	—	-100	mA
				3 V	—	—	-50	
V_{OL}	P	Output low voltage	All I/O pins, standard-drive strength	5 V, I_{load} = 5 mA	—	—	0.8	V
	C			3 V, I_{load} = 2.5 mA	—	—	0.8	V
	P		High current drive pins, high-drive strength[2]	5 V, I_{load} =20 mA	—	—	0.8	V
	C			3 V, I_{load} = 10 mA	—	—	0.8	V
I_{OLT}	D	Output low current	Max total I_{OL} for all ports	5 V	—	—	100	mA
				3 V	—	—	50	
V_{IH}	P	Input high voltage	All digital inputs	V_{DD}>4.5V	0.70 × V_{DD}	—	—	V
	C			V_{DD}>2.7V	0.75 × V_{DD}	—	—	
V_{IL}	P	Input low voltage	All digital inputs	V_{DD}>4.5V	—	—	0.30 × V_{DD}	V
	C			V_{DD}>2.7V	—	—	0.35 × V_{DD}	
V_{hys}	C	Input hysteresis	All digital inputs	—	0.06 × V_{DD}	—	—	mV
$\|I_{In}\|$	P	Input leakage current	All input only pins (per pin)	V_{IN} = V_{DD} or V_{SS}	—	0.1	1	μA
$\|I_{OZ}\|$	P	Hi-Z (off-state) leakage current	All input/output (per pin)	V_{IN} = V_{DD} or V_{SS}	—	0.1	1	μA
$\|I_{OZTOT}\|$	C	Total leakage combined for all inputs and Hi-Z pins	All input only and I/O	V_{IN} = V_{DD} or V_{SS}	—	—	2	μA
R_{PU}	P	Pullup resistors	All digital inputs, when enabled (all I/O pins other than PTA2 and PTA3)	—	30.0	—	50.0	kΩ
R_{PU}[3]	P	Pullup resistors	PTA2 and PTA3 pin	—	30.0	—	60.0	kΩ
I_{IC}	D	DC injection current[4, 5, 6]	Single pin limit	V_{IN} < V_{SS}, V_{IN} > V_{DD}	-0.2	—	2	mA
			Total MCU limit, includes sum of all stressed pins		-5	—	25	
C_{In}	C	Input capacitance, all pins		—	—	—	7	pF
V_{RAM}	C	RAM retention voltage		—	2.0	—	—	V

1. Typical values are measured at 25 °C. Characterized, not tested.
2. Only PTB4, PTB5, PTD0, PTD1, PTE0, PTE1, PTH0, and PTH1 support ultra high current output.
3. The specified resistor value is the actual value internal to the device. The pullup value may appear higher when measured externally on the pin.
4. All functional non-supply pins, except for PTA2 and PTA3, are internally clamped to V_{SS} and V_{DD}.
5. Input must be current-limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the large one.

6. Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If the positive injection current ($V_{In} > V_{DD}$) is higher than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure that external V_{DD} load will shunt current higher than maximum injection current when the MCU is not consuming power, such as no system clock is present, or clock rate is very low (which would reduce overall power consumption).

Table 3. LVD and POR Specification

Symbol	C	Description	Min	Typ	Max	Unit
V_{POR}	D	POR re-arm voltage[1, 2]	1.5	1.75	2.0	V
V_{LVDH}	C	Falling low-voltage detect threshold - high range (LVDV = 1)[3]	4.2	4.3	4.4	V
V_{LVW1H}	C	Falling low-voltage warning threshold - high range: Level 1 falling (LVWV = 00)	4.3	4.4	4.5	V
V_{LVW2H}	C	Falling low-voltage warning threshold - high range: Level 2 falling (LVWV = 01)	4.5	4.5	4.6	V
V_{LVW3H}	C	Falling low-voltage warning threshold - high range: Level 3 falling (LVWV = 10)	4.6	4.6	4.7	V
V_{LVW4H}	C	Falling low-voltage warning threshold - high range: Level 4 falling (LVWV = 11)	4.7	4.7	4.8	V
V_{HYSH}	C	High range low-voltage detect/warning hysteresis	—	100	—	mV
V_{LVDL}	C	Falling low-voltage detect threshold - low range (LVDV = 0)	2.56	2.61	2.66	V
V_{LVDW1L}	C	Falling low-voltage warning threshold - low range: Level 1 falling (LVWV = 00)	2.62	2.7	2.78	V
V_{LVDW2L}	C	Falling low-voltage warning threshold - low range: Level 2 falling (LVWV = 01)	2.72	2.8	2.88	V
V_{LVDW3L}	C	Falling low-voltage warning threshold - low range: Level 3 falling (LVWV = 10)	2.82	2.9	2.98	V
V_{LVDW4L}	C	Falling low-voltage warning threshold - low range: Level 4 falling (LVWV = 11)	2.92	3.0	3.08	V
V_{HYSDL}	C	Low range low-voltage detect hysteresis	—	40	—	mV
V_{HYSWL}	C	Low range low-voltage warning hysteresis	—	80	—	mV
V_{BG}	P	Buffered bandgap output [4]	1.14	1.16	1.18	V

1. Maximum is highest voltage that POR is guaranteed.
2. POR ramp time must be longer than 20us/V to get a stable startup.
3. Rising thresholds are falling threshold + hysteresis.
4. Voltage factory trimmed at V_{DD} = 5.0 V, Temp = 25 °C

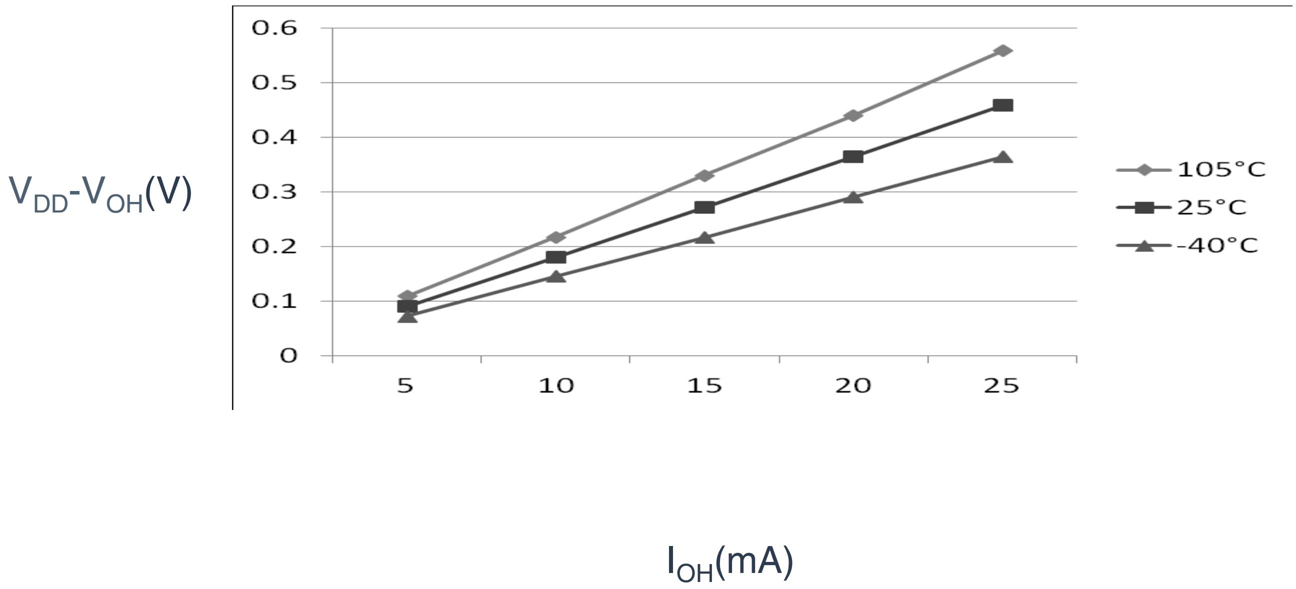

Figure 3. Typical I_{OH} Vs. V_{DD}-V_{OH} (high drive strength) (V_{DD} = 5 V)

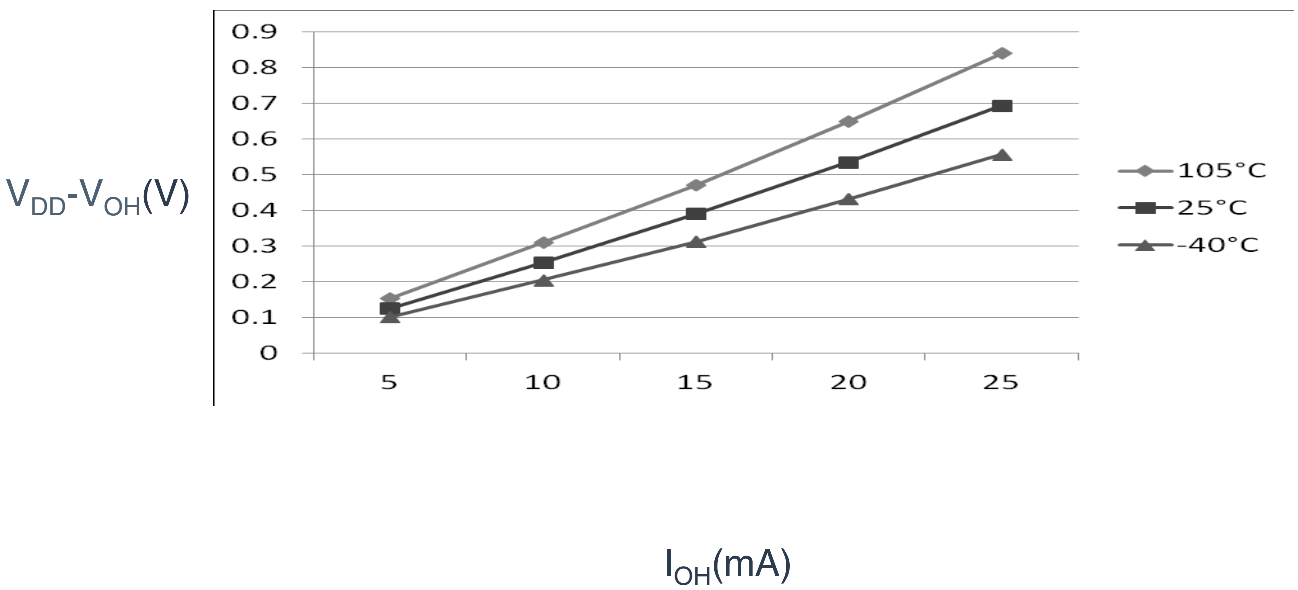

Figure 4. Typical I_{OH} Vs. V_{DD}-V_{OH} (high drive strength) (V_{DD} = 3 V)

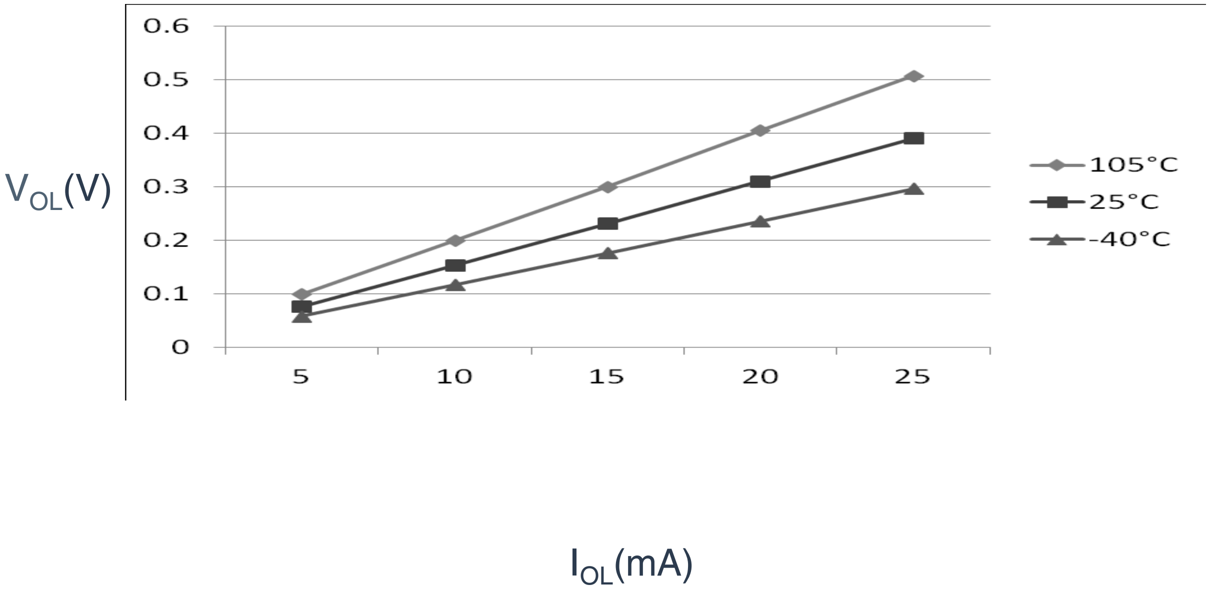

Figure 7. Typical I_{OL} Vs. V_{OL} (high drive strength) (V_{DD} = 5 V)

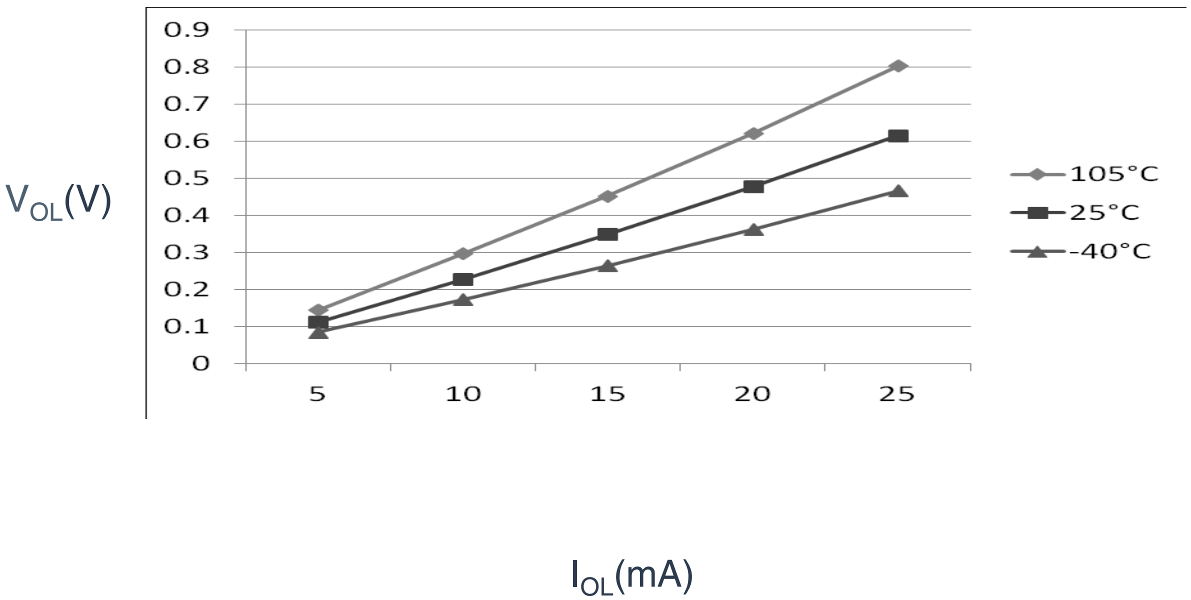

Figure 8. Typical I_{OL} Vs. V_{OL} (high drive strength) (V_{DD} = 3 V)

5.1.2 Supply current characteristics

This section includes information about power supply current in various operating modes.

Table 4. Supply current characteristics

Num	C	Parameter	Symbol	Bus Freq	V_{DD} (V)	Typical[1]	Max	Unit	Temp
1	C	Run supply current FEI mode, all modules on; run from flash	RI_{DD}	20 MHz	5	12.6	—	mA	-40 to 105 °C
	C			10 MHz		7.2	—		
				1 MHz		2.4	—		
	C			20 MHz	3	9.6	—		
	C			10 MHz		6.1	—		
				1 MHz		2.1	—		
2	C	Run supply current FEI mode, all modules off & gated; run from flash	RI_{DD}	20 MHz	5	10.5	—	mA	-40 to 105 °C
	C			10 MHz		6.2	—		
				1 MHz		2.3	—		
	C			20 MHz	3	7.4	—		
	C			10 MHz		5.0	—		
				1 MHz		2.0	—		
3	P	Run supply current FBE mode, all modules on; run from RAM	RI_{DD}	20 MHz	5	12.1	14.8	mA	-40 to 105 °C
	C			10 MHz		6.5	—		
				1 MHz		1.8	—		
	P			20 MHz	3	9.1	11.8		
	C			10 MHz		5.5	—		
				1 MHz		1.5	—		
4	P	Run supply current FBE mode, all modules off & gated; run from RAM	RI_{DD}	20 MHz	5	9.8	12.3	mA	-40 to 105 °C
	C			10 MHz		5.4	—		
				1 MHz		1.6	—		
	P			20 MHz	3	6.9	9.2		
	C			10 MHz		4.4	—		
				1 MHz		1.4	—		
5	C	Wait mode current FEI mode, all modules on	WI_{DD}	20 MHz	5	7.8	—	mA	-40 to 105 °C
	C			10 MHz		4.5	—		
				1 MHz		1.3	—		
	C			20 MHz	3	5.1	—		
				10 MHz		3.5	—		
				1 MHz		1.2	—		
6	C	Stop3 mode supply current no clocks active (except 1 kHz LPO clock)[2, 3]	$S3I_{DD}$	—	5	3.8	—	µA	-40 to 105 °C
	C			—	3	3	—		-40 to 105 °C
7	C	ADC adder to stop3	—	—	5	44	—	µA	-40 to 105 °C

Table continues on the next page...

Table 4. Supply current characteristics (continued)

Num	C	Parameter	Symbol	Bus Freq	V_{DD} (V)	Typical[1]	Max	Unit	Temp
	C	ADLPC = 1 ADLSMP = 1 ADCO = 1 MODE = 10B ADICLK = 11B			3	40	—		
8	C	LVD adder to stop3[4]	—	—	5	130	—	µA	-40 to 105 °C
	C				3	125	—		

1. Data in Typical column was characterized at 5.0 V, 25 °C or is typical recommended value.
2. RTC adder cause <1 µA I_{DD} increase typically, RTC clock source is 1 kHz LPO clock.
3. ACMP adder cause <10 µA I_{DD} increase typically.
4. LVD is periodically woken up from stop3 by 5% duty cycle. The period is equal to or less than 2 ms.

5.1.3 EMC performance

Electromagnetic compatibility (EMC) performance is highly dependent on the environment in which the MCU resides. Board design and layout, circuit topology choices, location and characteristics of external components as well as MCU software operation all play a significant role in EMC performance. The system designer should consult Freescale applications notes such as AN2321, AN1050, AN1263, AN2764, and AN1259 for advice and guidance specifically targeted at optimizing EMC performance.

5.1.3.1 EMC radiated emissions operating behaviors

Table 5. EMC radiated emissions operating behaviors for 64-pin SOIC package

Symbol	Description	Frequency band (MHz)	Typ.	Unit	Notes
V_{RE1}	Radiated emissions voltage, band 1	0.15–50	12	dBµV	1, 2
V_{RE2}	Radiated emissions voltage, band 2	50–150	10	dBµV	
V_{RE3}	Radiated emissions voltage, band 3	150–500	4	dBµV	
V_{RE4}	Radiated emissions voltage, band 4	500–1000	5	dBµV	
V_{RE_IEC}	IEC level	0.15–1000	N	—	2, 3

1. Determined according to IEC Standard 61967-1, *Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 1: General Conditions and Definitions* and IEC Standard 61967-2, *Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 2: Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method*. Measurements were made while the microcontroller was running basic application code. The reported emission level is the value of the maximum measured emission, rounded up to the next whole number, from among the measured orientations in each frequency range.
2. V_{DD} = 5.0 V, T_A = 25 °C, f_{OSC} = 10 MHz (crystal), f_{SYS} = 20 MHz, f_{BUS} = 20 MHz
3. Specified according to Annex D of IEC Standard 61967-2, *Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method*

5.2 Switching specifications

5.2.1 Control timing

Table 6. Control timing

Num	C	Rating		Symbol	Min	Typical[1]	Max	Unit
1	P	Bus frequency ($t_{cyc} = 1/f_{Bus}$)		f_{Bus}	DC	—	20	MHz
2	P	Internal low power oscillator frequency		f_{LPO}	0.67	1.0	1.25	KHz
3	D	External reset pulse width[2]		t_{extrst}	1.5 × t_{cyc}	—	—	ns
4	D	Reset low drive		t_{rstdrv}	34 × t_{cyc}	—	—	ns
5	D	BKGD/MS setup time after issuing background debug force reset to enter user or BDM modes		t_{MSSU}	500	—	—	ns
6	D	BKGD/MS hold time after issuing background debug force reset to enter user or BDM modes[3]		t_{MSH}	100	—	—	ns
7	D	IRQ pulse width	Asynchronous path[2]	t_{ILIH}	100	—	—	ns
	D		Synchronous path[4]	t_{IHIL}	1.5 × t_{cyc}	—	—	ns
8	D	Keyboard interrupt pulse width	Asynchronous path[2]	t_{ILIH}	100	—	—	ns
	D		Synchronous path	t_{IHIL}	1.5 × t_{cyc}	—	—	ns
9	C	Port rise and fall time - standard drive strength (load = 50 pF)[5]	—	t_{Rise}	—	10.2	—	ns
	C			t_{Fall}	—	9.5	—	ns
	C	Port rise and fall time - high drive strength (load = 50 pF)[5]	—	t_{Rise}	—	5.4	—	ns
	C			t_{Fall}	—	4.6	—	ns

1. Typical values are based on characterization data at V_{DD} = 5.0 V, 25 °C unless otherwise stated.
2. This is the shortest pulse that is guaranteed to be recognized as a reset pin request.
3. To enter BDM mode following a POR, BKGD/MS must be held low during the powerup and for a hold time of t_{MSH} after V_{DD} rises above V_{LVD}.
4. This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In stop mode, the synchronizer is bypassed so shorter pulses can be recognized.
5. Timing is shown with respect to 20% V_{DD} and 80% V_{DD} levels in operating temperature range.

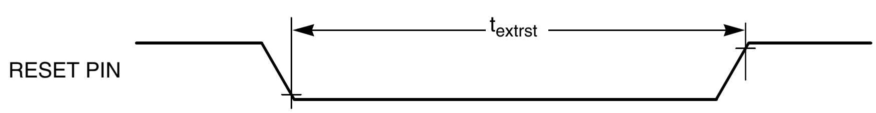

Figure 9. Reset timing

5.2.3 FTM module timing

Synchronizer circuits determine the shortest input pulses that can be recognized or the fastest clock that can be used as the optional external source to the timer counter. These synchronizers operate from the current bus rate clock.

Table 8. FTM input timing

No.	C	Function	Symbol	Min	Max	Unit
1	D	External clock frequency	f_{TCLK}	0	$f_{Bus}/4$	Hz
2	D	External clock period	t_{TCLK}	4	—	t_{cyc}
3	D	External clock high time	t_{clkh}	1.5	—	t_{cyc}
4	D	External clock low time	t_{clkl}	1.5	—	t_{cyc}
5	D	Input capture pulse width	t_{ICPW}	1.5	—	t_{cyc}

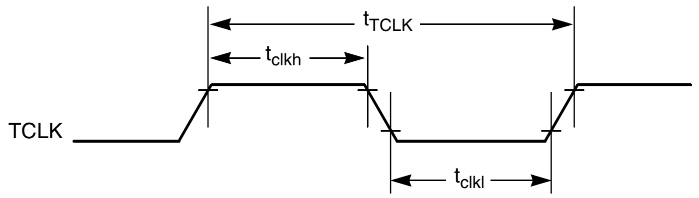

Figure 13. Timer external clock

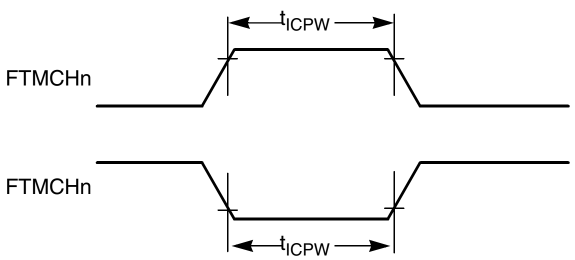

Figure 14. Timer input capture pulse

Table 10. Thermal attributes (continued)

Board type	Symbol	Description	64 LQFP	64 QFP	48 LQFP	44 LQFP	32 LQFP	Unit	Notes
—	$R_{\theta JB}$	Thermal resistance, junction to board	35	32	34	34	33	°C/W	4
—	$R_{\theta JC}$	Thermal resistance, junction to case	20	23	24	20	24	°C/W	5
—	Ψ_{JT}	Thermal characterization parameter, junction to package top outside center (natural convection)	5	8	6	5	6	°C/W	6

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-2 with the single layer board (JESD51-3) horizontal.
3. Per JEDEC JESD51-6 with the board (JESD51-7) horizontal.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the solder pad on the bottom of the package. Interface resistance is ignored.
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization.

6 Peripheral operating requirements and behaviors

6.1 External oscillator (XOSC) and ICS characteristics

Table 11. XOSC and ICS specifications (temperature range = -40 to 105 °C ambient)

Num	C	Characteristic		Symbol	Min	Typical[1]	Max	Unit
1	C	Oscillator crystal or resonator	Low range (RANGE = 0)	f_{lo}	31.25	32.768	39.0625	kHz
	C		High range (RANGE = 1) FEE or FBE mode[2]	f_{hi}	4	—	20	MHz
	C		High range (RANGE = 1), high gain (HGO = 1), FBELP mode	f_{hi}	4	—	20	MHz
	C		High range (RANGE = 1), low power (HGO = 0), FBELP mode	f_{hi}	4	—	20	MHz
2	D	Load capacitors		C1, C2	See Note[3]			
3	D	Feedback resistor	Low Frequency, Low-Power Mode[4]	R_F	—	—	—	MΩ
			Low Frequency, High-Gain Mode		—	10	—	MΩ
			High Frequency, Low-Power Mode		—	1	—	MΩ

Table continues on the next page...

Table 12. Flash characteristics (continued)

C	Characteristic	Symbol	Min[1]	Typical[2]	Max[3]	Unit[4]
D	Erase Flash Sector	t_{ERSPG}	19.10	20.05	20.08	ms
D	Erase EEPROM Sector	t_{DERSPG}	4.81	5.05	20.57	ms
D	Unsecure Flash	t_{UNSECU}	96.01	100.78	101.48	ms
D	Verify Backdoor Access Key	t_{VFYKEY}	—	—	464	t_{cyc}
D	Set User Margin Level	t_{MLOADU}	—	—	407	t_{cyc}
C	FLASH Program/erase endurance T_L to T_H = -40 °C to 105 °C	n_{FLPE}	10 k	100 k	—	Cycles
C	EEPROM Program/erase endurance TL to TH = -40 °C to 105 °C	n_{FLPE}	50 k	500 k	—	Cycles
C	Data retention at an average junction temperature of T_{Javg} = 85°C after up to 10,000 program/erase cycles	t_{D_ret}	15	100	—	years

1. Minimum times are based on maximum f_{NVMOP} and maximum f_{NVMBUS}
2. Typical times are based on typical f_{NVMOP} and maximum f_{NVMBUS}
3. Maximum times are based on typical f_{NVMOP} and typical f_{NVMBUS} plus aging
4. $t_{cyc} = 1 / f_{NVMBUS}$

Program and erase operations do not require any special power sources other than the normal V_{DD} supply. For more detailed information about program/erase operations, see the Memory section.

6.3 Analog

6.3.1 ADC characteristics

Table 13. 5 V 12-bit ADC operating conditions

Characteristic	Conditions	Symb	Min	Typ[1]	Max	Unit	Comment
Supply voltage	Absolute	V_{DDA}	2.7	—	5.5	V	—
	Delta to V_{DD} (V_{DD}-V_{DDAD})	ΔV_{DDA}	-100	0	+100	mV	
Ground voltage	Delta to V_{SS} (V_{SS}-V_{SSA})[2]	ΔV_{SSA}	-100	0	+100	mV	
Input voltage		V_{ADIN}	V_{REFL}	—	V_{REFH}	V	
Input capacitance		C_{ADIN}	—	4.5	5.5	pF	
Input resistance		R_{ADIN}	—	3	5	kΩ	—
Analog source resistance	12-bit mode • f_{ADCK} > 4 MHz • f_{ADCK} < 4 MHz	R_{AS}	— —	— —	2 5	kΩ	External to MCU

Table continues on the next page...

Table 13. 5 V 12-bit ADC operating conditions (continued)

Characteristic	Conditions	Symb	Min	Typ[1]	Max	Unit	Comment
	10-bit mode • f_{ADCK} > 4 MHz • f_{ADCK} < 4 MHz		— —	— —	5 10		
	8-bit mode (all valid f_{ADCK})		—	—	10		
ADC conversion clock frequency	High speed (ADLPC=0)	f_{ADCK}	0.4	—	8.0	MHz	—
	Low power (ADLPC=1)		0.4	—	4.0		

1. Typical values assume V_{DDA} = 5.0 V, Temp = 25°C, f_{ADCK}=1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
2. DC potential difference.

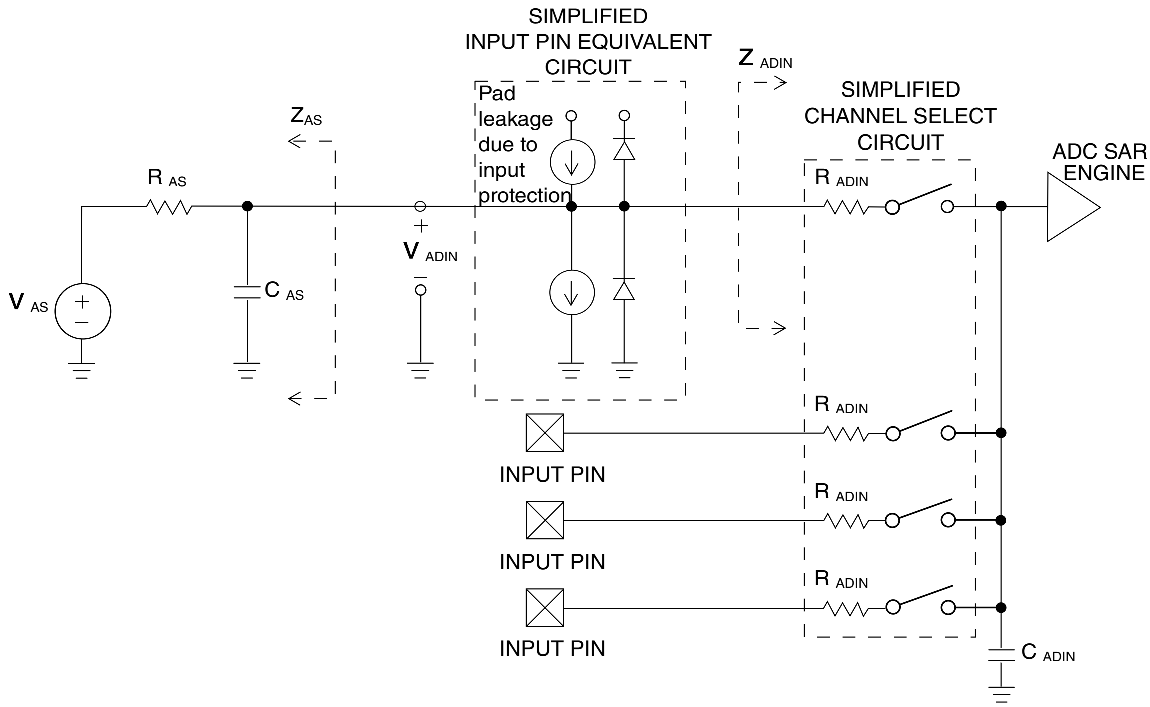

Figure 16. ADC input impedance equivalency diagram

Table 14. 12-bit ADC Characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$)

Characteristic	Conditions	C	Symb	Min	Typ[1]	Max	Unit
Supply current ADLPC = 1 ADLSMP = 1 ADCO = 1		T	I_{DDA}	—	133	—	µA
Supply current		T	I_{DDA}	—	218	—	µA

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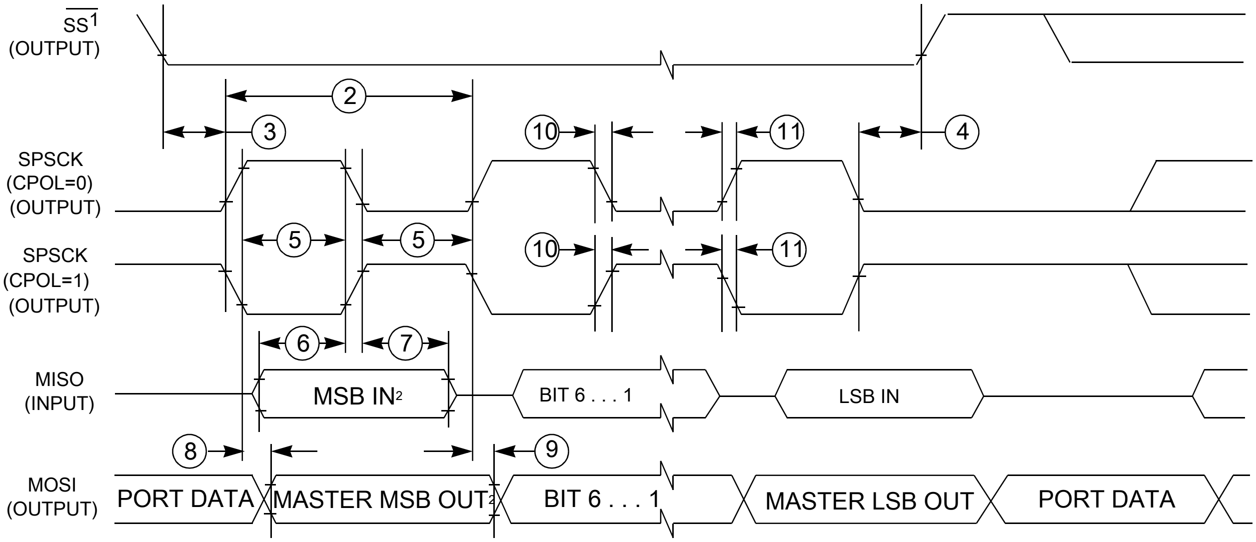

1.If configured as output

2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 18. SPI master mode timing (CPHA=1)

Table 17. SPI slave mode timing

Num.	Symbol	Description	Min.	Max.	Unit	Comment
1	f_{op}	Frequency of operation	0	$f_{Bus}/4$	Hz	f_{Bus} is the bus clock as defined in .
2	t_{SPSCK}	SPSCK period	4 x t_{Bus}	—	ns	$t_{Bus} = 1/f_{Bus}$
3	t_{Lead}	Enable lead time	1	—	t_{Bus}	—
4	t_{Lag}	Enable lag time	1	—	t_{Bus}	—
5	t_{WSPSCK}	Clock (SPSCK) high or low time	t_{Bus} - 30	—	ns	—
6	t_{SU}	Data setup time (inputs)	15	—	ns	—
7	t_{HI}	Data hold time (inputs)	25	—	ns	—
8	t_a	Slave access time	—	t_{Bus}	ns	Time to data active from high-impedance state
9	t_{dis}	Slave MISO disable time	—	t_{Bus}	ns	Hold time to high-impedance state
10	t_v	Data valid (after SPSCK edge)	—	25	ns	—
11	t_{HO}	Data hold time (outputs)	0	—	ns	—
12	t_{RI}	Rise time input	—	t_{Bus} - 25	ns	—
	t_{FI}	Fall time input				
13	t_{RO}	Rise time output	—	25	ns	—
	t_{FO}	Fall time output				

Table 18. Pin availability by package pin-count (continued)

Pin Number				Lowest Priority <-- --> Highest				
64-LQFP 64-QFP	48-LQFP	44-LQFP	32-LQFP	Port Pin	Alt 1	Alt 2	Alt 3	Alt 4
17	13	—	—	PTE5	—	—	—	—
18	14	12	9	PTB5[1]	FTM2CH5	$\overline{SS0}$	—	—
19	15	13	10	PTB4[1]	FTM2CH4	MISO0	—	—
20	16	14	11	PTC3	FTM2CH3	—	ADP11	—
21	17	15	12	PTC2	FTM2CH2	—	ADP10	—
22	18	16	—	PTD7	KBI1P7	TXD2	—	—
23	19	17	—	PTD6	KBI1P6	RXD2	—	—
24	20	18	—	PTD5	KBI1P5	—	—	—
25	21	19	13	PTC1	—	FTM2CH1	ADP9	—
26	22	20	14	PTC0	—	FTM2CH0	ADP8	—
27	—	—	—	PTF7	—	—	ADP15	—
28	—	—	—	PTF6	—	—	ADP14	—
29	—	—	—	PTF5	—	—	ADP13	—
30	—	—	—	PTF4	—	—	ADP12	—
31	23	21	15	PTB3	KBI0P7	MOSI0	ADP7	—
32	24	22	16	PTB2	KBI0P6	SPSCK0	ADP6	—
33	25	23	17	PTB1	KBI0P5	TXD0	ADP5	—
34	26	24	18	PTB0	KBI0P4	RXD0	ADP4	—
35	—	—	—	PTF3	—	—	—	—
36	—	—	—	PTF2	—	—	—	—
37	27	25	19	PTA7	FTM2FAULT2	—	ADP3	—
38	28	26	20	PTA6	FTM2FAULT1	—	ADP2	—
39	29	—	—	PTE4	—	—	—	—
40	30	27	—	—	—	—	—	V_{SS}
41	31	28	—	—	—	—	—	V_{DD}
42	—	—	—	PTF1	—	—	—	—
43	—	—	—	PTF0	—	—	—	—
44	32	29	—	PTD4	KBI1P4	—	—	—
45	33	30	21	PTD3	KBI1P3	$\overline{SS1}$	—	—
46	34	31	22	PTD2	KBI1P2	MISO1	—	—
47	35	32	23	PTA3[2]	KBI0P3	TXD0	SCL	—
48	36	33	24	PTA2[2]	KBI0P2	RXD0	SDA	—
49	37	34	25	PTA1	KBI0P1	FTM0CH1	ACMP1	ADP1
50	38	35	26	PTA0	KBI0P0	FTM0CH0	ACMP0	ADP0
51	39	36	27	PTC7	—	TxD1	—	—
52	40	37	28	PTC6	—	RxD1	—	—
53	41	—	—	PTE3	—	$\overline{SS0}$	—	—

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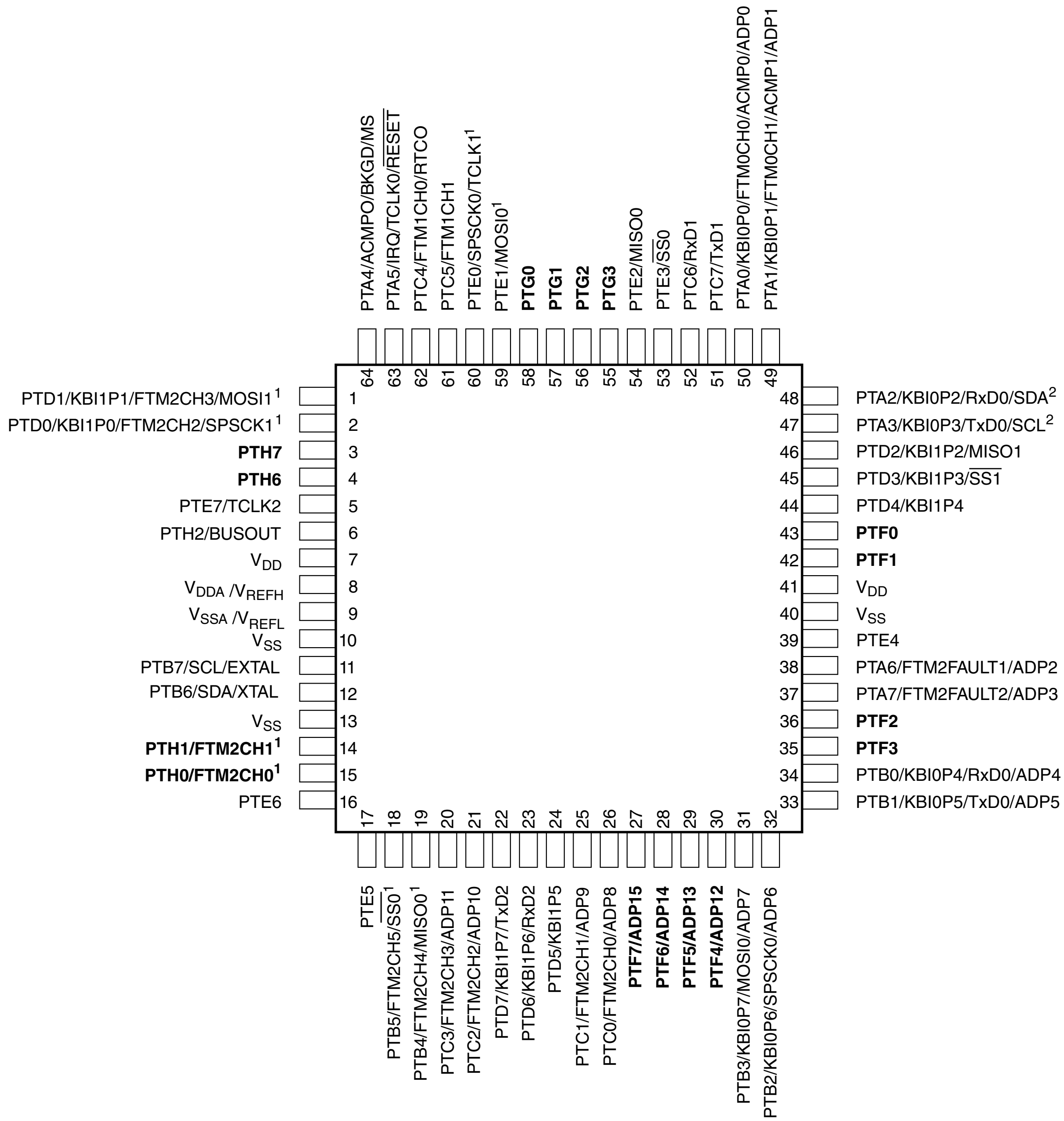
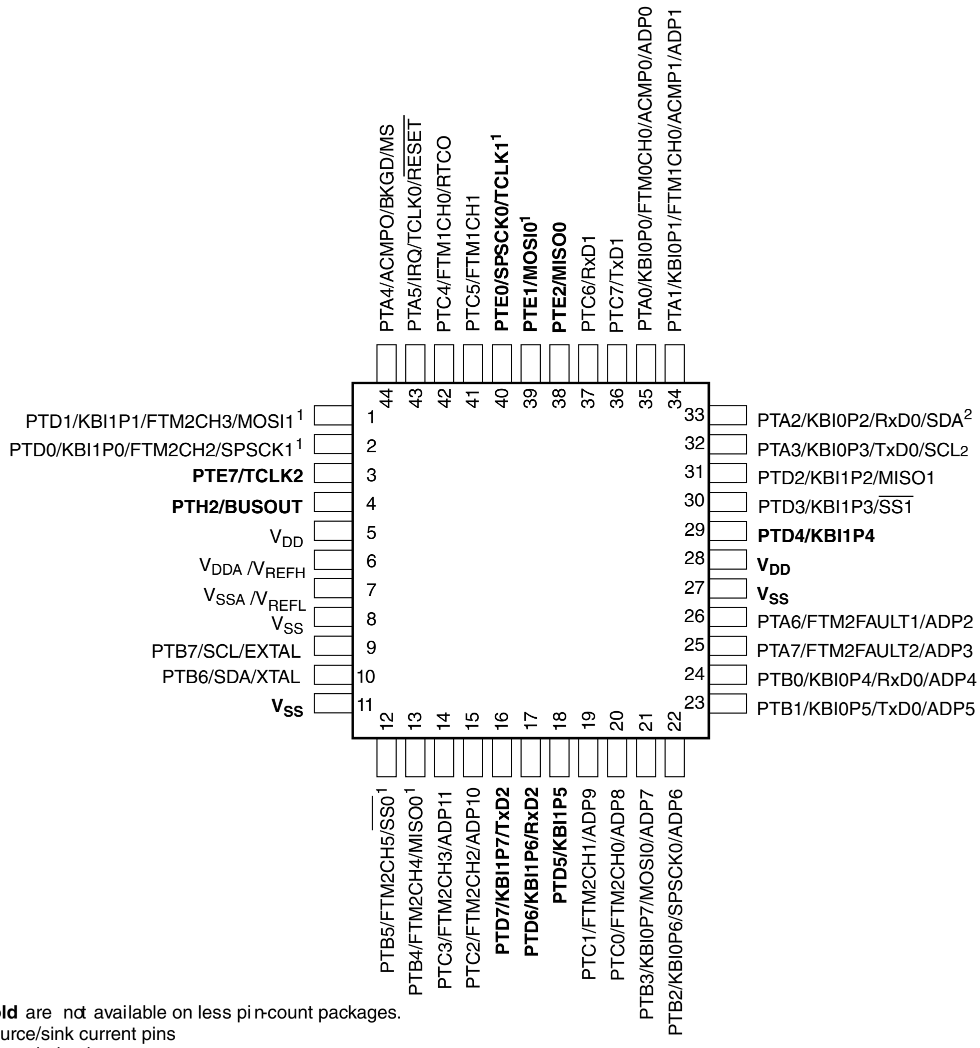


Pins in **bold** are not available on less pin-count packages.
1. High source/sink current pins
2. True open drain pins

Figure 21. MC9S08PA60 64-pin QFP and LQFP package



Pins in **bold** are not available on less pin-count packages.
1. High source/sink current pins
2. True open drain pins

Figure 23. MC9S08PA60 44-pin LQFP package

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