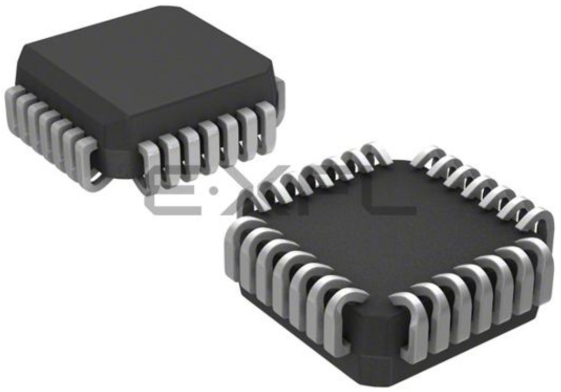

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	80C51
Core Size	8-Bit
Speed	40MHz
Connectivity	CANbus, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	20
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-LCC (J-Lead)
Supplier Device Package	28-PLCC (11.51x11.51)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/t89c51cc02ua-sisim

Description

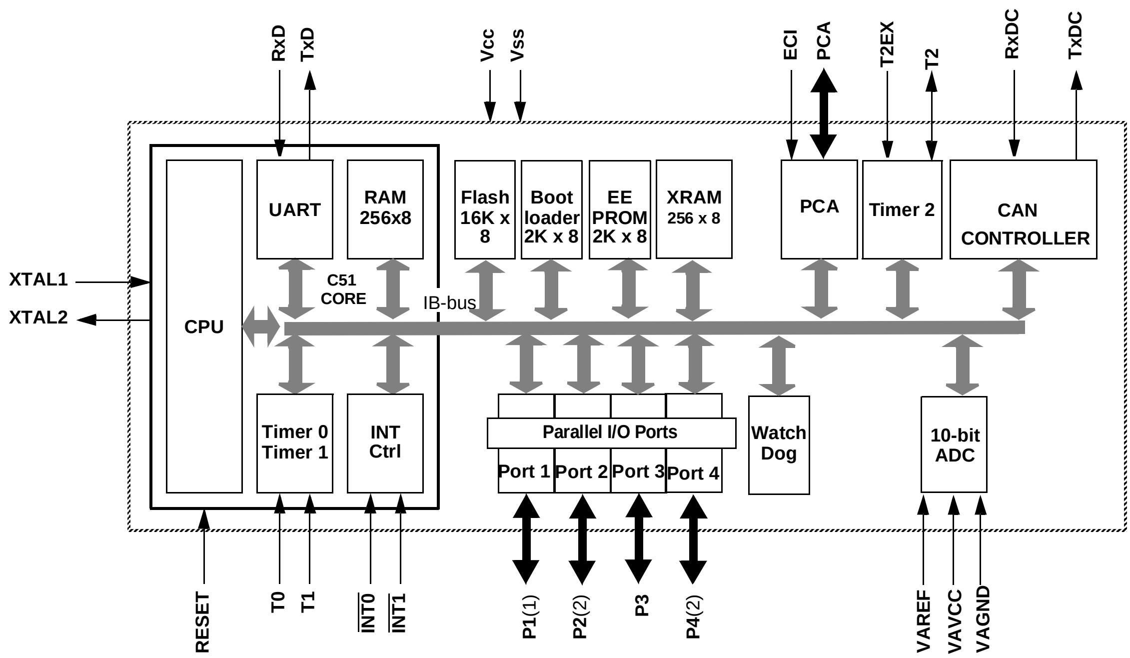
Part of the CANary™ family of 8-bit microcontrollers dedicated to CAN network applications, the T89C51CC02 is a low-pin count 8-bit Flash microcontroller.

In X2 Mode a maximum external clock rate of 20 MHz reaches a 300 ns cycle time.

Besides the full CAN controller T89C51CC02 provides 16K Bytes of Flash memory including In-System Programming (ISP), 2K Bytes Boot Flash Memory, 2K Bytes EEPROM and 512 Bytes RAM.

Special attention is payed to the reduction of the electro-magnetic emission of T89C51CC02.

Block Diagram



Note: 1. 8 analog Inputs/8 Digital I/O.
2. 2-bit I/O Port.

Table 4. Timers SFRs (Continued)

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
T2CON	C8h	Timer/Counter 2 control	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/T2#	CP/RL2#
T2MOD	C9h	Timer/Counter 2 Mode							T2OE	DCEN
RCAP2H	CBh	Timer/Counter 2 Reload/Capture High byte								
RCAP2L	CAh	Timer/Counter 2 Reload/Capture Low byte								
WDTRST	A6h	WatchDog Timer Reset								
WDTPRG	A7h	WatchDog Timer Program						S2	S1	S0

Table 5. Serial I/O Port SFRs

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
SCON	98h	Serial Control	FE/SM0	SM1	SM2	REN	TB8	RB8	TI	RI
SBUF	99h	Serial Data Buffer								
SADEN	B9h	Slave Address Mask								
SADDR	A9h	Slave Address								

Table 6. PCA SFRs

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
CCON	D8h	PCA Timer/Counter Control	CF	CR		CCF4	CCF3	CCF2	CCF1	CCF0
CMOD	D9h	PCA Timer/Counter Mode	CIDL					CPS1	CPS0	ECF
CL	E9h	PCA Timer/Counter Low byte								
CH	F9h	PCA Timer/Counter High byte								
CCAPM0 CCAPM1	DAh DBh	PCA Timer/Counter Mode 0 PCA Timer/Counter Mode 1		ECOM0 ECOM1	CAPP0 CAPP1	CAPN0 CAPN1	MAT0 MAT1	TOG0 TOG1	PWM0 PWM1	ECCF0 ECCF1
CCAP0H CCAP1H	FAh FBh	PCA Compare Capture Module 0 H PCA Compare Capture Module 1 H	CCAP0H7 CCAP1H7	CCAP0H6 CCAP1H6	CCAP0H5 CCAP1H5	CCAP0H4 CCAP1H4	CCAP0H3 CCAP1H3	CCAP0H2 CCAP1H2	CCAP0H1 CCAP1H1	CCAP0H0 CCAP1H0

Table 18. AUXR1 Register
AUXR1 (S:A2h)
Auxiliary Control Register 1

7	6	5	4	3	2	1	0
-	-	ENBOOT	-	GF3	0	-	DPS

Bit Number	Bit Mnemonic	Description
7 - 6	-	**Reserved** The value read from these bits is indeterminate. Do not set these bits.
5	ENBOOT[(1)]	**Enable Boot Flash** Set this bit to map the boot Flash between F800h -FFFFh Clear this bit to disable boot Flash.
4	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
3	GF3	**General Purpose Flag 3**
2	0	**Always Zero** This bit is stuck to logic 0 to allow INC AUXR1 instruction without affecting GF3 flag.
1	-	**Reserved for Data Pointer Extension**
0	DPS	**Data Pointer Select bit** Set to select second dual data pointer: DPTR1. Clear to select first dual data pointer: DPTR0.

Reset Value = XXXX 00X0b

Note: 1. ENBOOT is initialized with the invert BLJB at reset. See In-System Programming section.

Status of the Flash Memory

The bit FBUSY in FCON register is used to indicate the status of programming.

FBUSY is set when programming is in progress.

Selecting FM1

The bit ENBOOT in AUXR1 register is used to map FM1 from F800h to FFFFh.

Loading the Column Latches

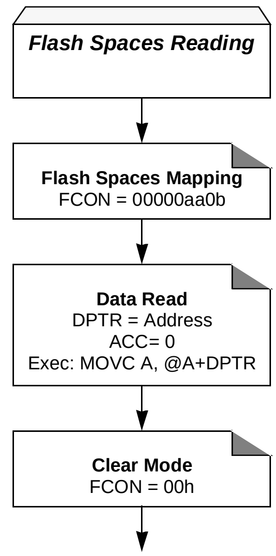
Any number of data from 1 byte to 128 Bytes can be loaded in the column latches. This provides the capability to program the whole memory by byte, by page or by any number of Bytes in a page.

When programming is launched, an automatic erase of the locations loaded in the column latches is first performed, then programming is effectively done. Thus no page or block erase is needed and only the loaded data are programmed in the corresponding page.

The following procedure is used to load the column latches and is summarized in Figure 14:

- Save then disable interrupt and map the column latch space by setting FPS bit.
- Load the DPTR with the address to load.
- Load Accumulator register with the data to load.
- Execute the MOVX @DPTR, A instruction.
- If needed loop the three last instructions until the page is completely loaded.
- unmap the column latch and Restore Interrupt

Figure 17. Reading Procedure



Note: aa = 10 for the Hardware Security Byte.

Flash Protection from Parallel Programming

The three lock bits in Hardware Security Byte (See 'In-System Programming' section) are programmed according to Table 23 provide different level of protection for the on-chip code and data located in FM0 and FM1.

The only way to write this bits are the parallel mode. They are set by default to level 3.

Table 23. Program Lock bit

Program Lock bits				
Security Level	LB0	LB1	LB2	**Protection Description**
1	U	U	U	No program lock features enabled. MOVC instruction executed from external program memory returns code data.
2	P	U	U	Parallel programming of the Flash is disabled.
3	U	P	U	Same as 2, also verify through parallel programming interface is disabled. This is the factory defaul programming.

Note: 1. Program Lock bits
U: unprogrammed
P: programmed

WARNING: Security level 2 and 3 should only be programmed after Flash and Core verification.

Preventing Flash Corruption

See Section "Power Management".

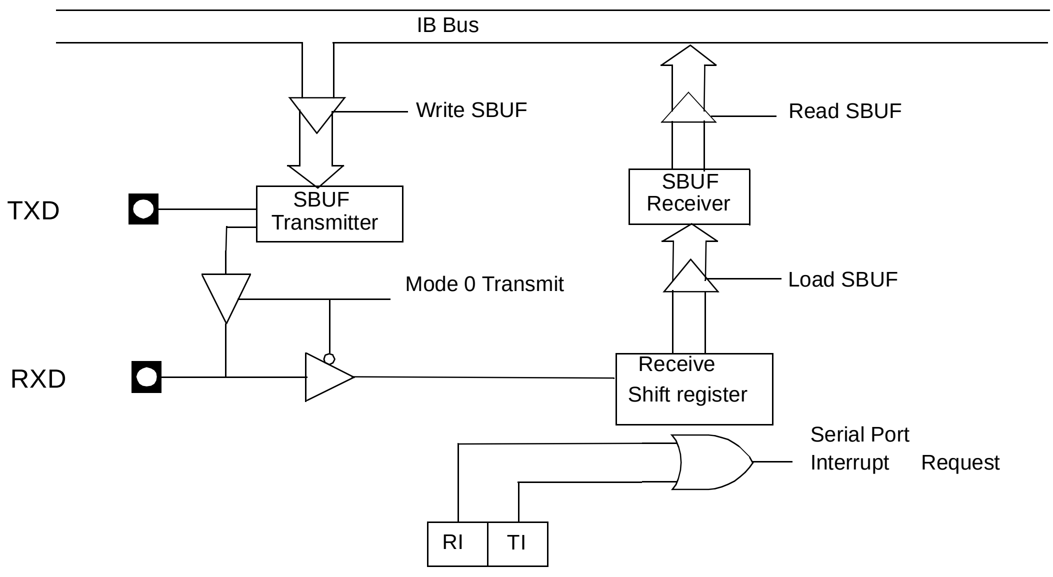
Serial I/O Port

The T89C51CC02 I/O serial port is compatible with the I/O serial port in the 80C52.
It provides both synchronous and asynchronous communication modes. It operates as a Universal Asynchronous Receiver and Transmitter (UART) in three full-duplex modes (Modes 1, 2 and 3). Asynchronous transmission and reception can occur simultaneously and at different baud rates

Serial I/O port includes the following enhancements:

- Framing error detection
- Automatic address recognition

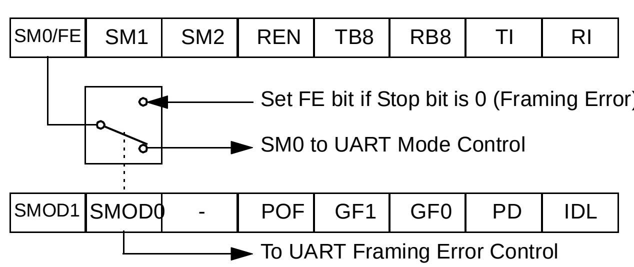
Figure 20. Serial I/O Port Block Diagram



Framing Error Detection

Framing bit error detection is provided for the three asynchronous modes. To enable the framing bit error detection feature, set SMOD0 bit in PCON register.

Figure 21. Framing Error Block Diagram



When this feature is enabled, the receiver checks each incoming data frame for a valid stop bit. An invalid stop bit may result from noise on the serial lines or from simultaneous transmission by two CPUs. If a valid stop bit is not found, the Framing Error bit (FE) in SCON register bit is set.

The software may examine the FE bit after each reception to check for data errors. Once set, only software or a reset clears the FE bit. Subsequently received frames with valid stop bits cannot clear the FE bit. When the FE feature is enabled, RI rises on the stop bit instead of the last data bit (See Figure 22 and Figure 23).

Here is an example of how to use given addresses to address different slaves:

```
Slave A:SADDR1111 0001b
    SADEN1111 1010b
    Given1111 0X0Xb

Slave B:SADDR1111 0011b
    SADEN1111 1001b
    Given1111 0XX1b

Slave C:SADDR1111 0011b
    SADEN1111 1101b
    Given1111 00X1b
```

The SADEN byte is selected so that each slave may be addressed separately.
For slave A, bit 0 (the LSB) is a don't-care bit; for slaves B and C, bit 0 is a 1. To communicate with slave A only, the master must send an address where bit 0 is clear (e.g. `1111 0000b`).
For slave A, bit 1 is a 0; for slaves B and C, bit 1 is a don't care bit. To communicate with slaves A and B, but not slave C, the master must send an address with bits 0 and 1 both set (e.g. `1111 0011b`).
To communicate with slaves A, B and C, the master must send an address with bit 0 set, bit 1 clear, and bit 2 clear (e.g. `1111 0001b`).

Broadcast Address

A broadcast address is formed from the logical OR of the SADDR and SADEN registers with zeros defined as don't-care bits, e.g.:

```
SADDR 0101 0110b
SADEN 1111 1100b
SADDR OR SADEN1111 111Xb
```

The use of don't-care bits provides flexibility in defining the broadcast address, however in most applications, a broadcast address is FFh. The following is an example of using broadcast addresses:

```
Slave A:SADDR1111 0001b
    SADEN1111 1010b
    Given1111 1X11b,

Slave B:SADDR1111 0011b
    SADEN1111 1001b
    Given1111 1X11B,

Slave C:SADDR=1111 0010b
    SADEN1111 1101b
    Given1111 1111b
```

For slaves A and B, bit 2 is a don't care bit; for slave C, bit 2 is set. To communicate with all of the slaves, the master must send an address FFh. To communicate with slaves A and B, but not slave C, the master can send and address FBh.

To enable an interrupt on Buffer-full condition:

- Enable General CAN IT in the interrupt system register
- Enable interrupt on Buffer full, ENBUF

To enable an interrupt when Timer overruns:

- Enable Overrun IT in the interrupt system register

When an interrupt occurs, the corresponding message object bit is set in the SIT register.

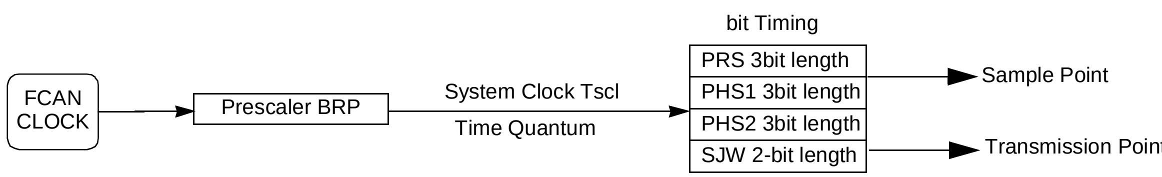
To acknowledge an interrupt, the corresponding CANSTCH bits (RXOK, TXOK,...) or CANGIT bits (OVRTIM, OVRBUF,...), must be cleared by the software application.

When the CAN node is in transmission and detects a Form Error in its frame, a bit Error will also be raised. Consequently, two consecutive interrupts can occur, both due to the same error.

When a message object error occurs and is set in CANSTCH register, no general error are set in CANGIE register.

bit Timing and Baud Rate

Figure 36. Sample and Transmission Point



The baud rate selection is made by Tbit calculation:

Tbit = Tsyns + Tprs + Tphs1 + Tphs2

1. Tsyns = Tscl = (BRP[5..0]+ 1)/Fcan = 1TQ
2. Tprs = (1 to 8) * Tscl = (PRS[2..0]+ 1) * Tscl
3. Tphs1 = (1 to 8) * Tscl = (PHS1[2..0]+ 1) * Tscl
4. Tphs2 = (1 to 8) * Tscl = (PHS2[2..0]+ 1) * Tscl
5. Tsjw = (1 to 4) * Tscl = (SJW[1..0]+ 1) * Tscl

The total number of Tscl (Time Quanta) in a bit time must be comprised between 8 to 25.

```
// Find the first message object which generate an interrupt in CANSIT
// Select the corresponding message object

// Analyse the CANSTCH register to identify which kind of interrupt is
generated

// Manage the interrupt

// Clear the status register CANSTCH = 00h;

// if it is not a channel interrupt but a general interrupt
// Manage the general interrupt and clear CANGIT register

// restore the old CANPAGE
```

Table 63. CANIE Register

CANIE (S:C3h) – CAN Enable Interrupt message object Registers 2

7	6	5	4	3	2	1	0
-	-	-	-	IECH 3	IECH 2	IECH 1	IECH 0

Bit Number	Bit Mnemonic	Description
7 - 4	-	**Reserved** The values read from these bits are indeterminate. Do not set these bits.
3 - 0	IECH3:0	**Enable Interrupt by Message Object** 0 - disable IT. 1 - enable IT. IECH3:0 = 0b 0000 1100 -> Enable IT's of message objects 3 & 2.

Reset Value = xxxx 0000b

Table 64. CANBT1 Register

CANBT1 (S:B4h) – CAN bit Timing Registers 1

7	6	5	4	3	2	1	0
-	BRP 5	BRP 4	BRP 3	BRP 2	BRP 1	BRP 0	-

Bit Number	Bit Mnemonic	Description
7	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
6 - 1	BRP5:0	**Baud Rate Prescaler** **The period of the CAN** controller system clock Tscl is programmable and determines the individual bit timing.(1) $Tscl = \frac{BRP[5..0] + 1}{F_{CAN}}$
0	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.

Note: 1. The CAN controller bit timing registers must be accessed only if the CAN controller is disabled with the ENA bit of the CANGCON register set to 0. See Figure 37.

No default value after reset.

Table 66. CANBT3 Register
CANBT3 (S:B6h)
CAN bit Timing Registers 3

7	6	5	4	3	2	1	0
-	**PHS2 2**	**PHS2 1**	**PHS2 0**	**PHS1 2**	**PHS1 1**	**PHS1 0**	**SMP**

Bit Number	Bit Mnemonic	Description
7	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
6 - 4	PHS2 2:0	**Phase Segment 2** This phase is used to compensate for phase edge errors. This segment can be shortened by the re-synchronization jump width. Tphs2 = Tscl x (PHS2[2..0] + 1)
3 - 1	PHS1 2:0	**Phase Segment 1** This phase is used to compensate for phase edge errors. This segment can be lengthened by the re-synchronization jump width. Tphs1 = Tscl x (PHS1[2..0] + 1)
0	SMP	**Sample Type** 0 - once, at the sample point. 1 - three times, the threefold sampling of the bus is the sample point and twice over a distance of a 1/2 period of the Tscl. The result corresponds to the majority decision of the three values.

Note: 1. The CAN controller bit timing registers must be accessed only if the CAN controller is disabled with the ENA bit of the CANGCON register set to 0.
See Figure 37.

No default value after reset.

Table 90. CANSTMPH Register
CANSTMPH (S:AFh Read Only)
CAN Stamp Timer High

7	6	5	4	3	2	1	0
TIMSTMP 15	TIMSTMP 14	TIMSTMP 13	TIMSTMP 12	TIMSTMP 11	TIMSTMP 10	TIMSTMP 9	TIMSTMP 8

Bit Number	Bit Mnemonic	Description
7 - 0	TIMSTMP15:8	**High byte of Time Stamp** See Figure 40.

No default value after reset

Table 91. CANSTMPL Register
CANSTMPL (S:AEh Read Only)
CAN Stamp Timer Low

7	6	5	4	3	2	1	0
TIMSTMP 7	TIMSTMP 6	TIMSTMP 5	TIMSTMP 4	TIMSTMP 3	TIMSTMP 2	TIMSTMP 1	TIMSTMP 0

Bit Number	Bit Mnemonic	Description
7 - 0	TIMSTMP7:0	**Low byte of Time Stamp** See Figure 40.

No default value after reset

Table 92. CANTTCH Register
CANTTCH (S:A5h Read Only)
CAN TTC Timer High

7	6	5	4	3	2	1	0
TIMTTC 15	TIMTTC 14	TIMTTC 13	TIMTTC 12	TIMTTC 11	TIMTTC 10	TIMTTC 9	TIMTTC 8

Bit Number	Bit Mnemonic	Description
7 - 0	TIMTTC15:8	**High byte of TTC Timer** See Figure 40.

Reset Value = 0000 0000b

Table 93. CANTTCL Register
CANTTCL (S:A4h Read Only)
CAN TTC Timer Low

7	6	5	4	3	2	1	0
TIMTTC 7	TIMTTC 6	TIMTTC 5	TIMTTC 4	TIMTTC 3	TIMTTC 2	TIMTTC 1	TIMTTC 0

Bit Number	Bit Mnemonic	Description
7 - 0	TIMTTC7:0	**Low Byte of TTC Timer** See Figure 40.

Reset Value = 0000 0000b

Programmable Counter Array (PCA)

The PCA provides more timing capabilities with less CPU intervention than the standard timer/counters. Its advantages include reduced software overhead and improved accuracy. The PCA consists of a dedicated timer/counter which serves as the time base for an array of two compare/capture modules. Its clock input can be programmed to count any of the following signals:

- PCA clock frequency/6 (See “clock” section)
- PCA clock frequency/2
- Timer 0 overflow
- External input on ECI (P1.2)

Each compare/capture modules can be programmed in any one of the following modes:

- Rising and/or falling edge capture,
- Software timer
- High-speed output
- Pulse width modulator

When the compare/capture modules are programmed in capture mode, software timer, or high speed output mode, an interrupt can be generated when the module executes its function. Both modules and the PCA timer overflow share one interrupt vector.

The PCA timer/counter and compare/capture modules share Port 1 for external I/Os. These pins are listed below. If the pin is not used for the PCA, it can still be used for standard I/O.

PCA Component	External I/O Pin
16-bit Counter	P1.2/ECI
16-bit Module 0	P1.3/CEX0
16-bit Module 1	P1.4/CEX1

PCA Timer

The PCA timer is a common time base for both modules (See Figure 9). The timer count source is determined from the CPS1 and CPS0 bits in the **CMOD SFR** (See Table 8) and can be programmed to run at:

- 1/6 the PCA clock frequency.
- 1/2 the PCA clock frequency.
- The Timer 0 overflow.
- The input on the ECI pin (P1.2).

Table 99. CH Register

CH (S:F9h)
PCA Counter Register High value

7	6	5	4	3	2	1	0
CH 7	CH 6	CH 5	CH 4	CH 3	CH 2	CH 1	CH 0

Bit Number	Bit Mnemonic	Description
7:0	CH 7:0	High byte of Timer/Counter

Reset Value = 0000 00000b

Table 100. CL Register

CL (S:E9h)
PCA counter Register Low value

7	6	5	4	3	2	1	0
CL 7	CL 6	CL 5	CL 4	CL 3	CL 2	CL 1	CL 0

Bit Number	Bit Mnemonic	Description
7:0	CL0 7:0	Low byte of Timer/Counter

Reset Value = 0000 00000b

Figure 48. ADC Description

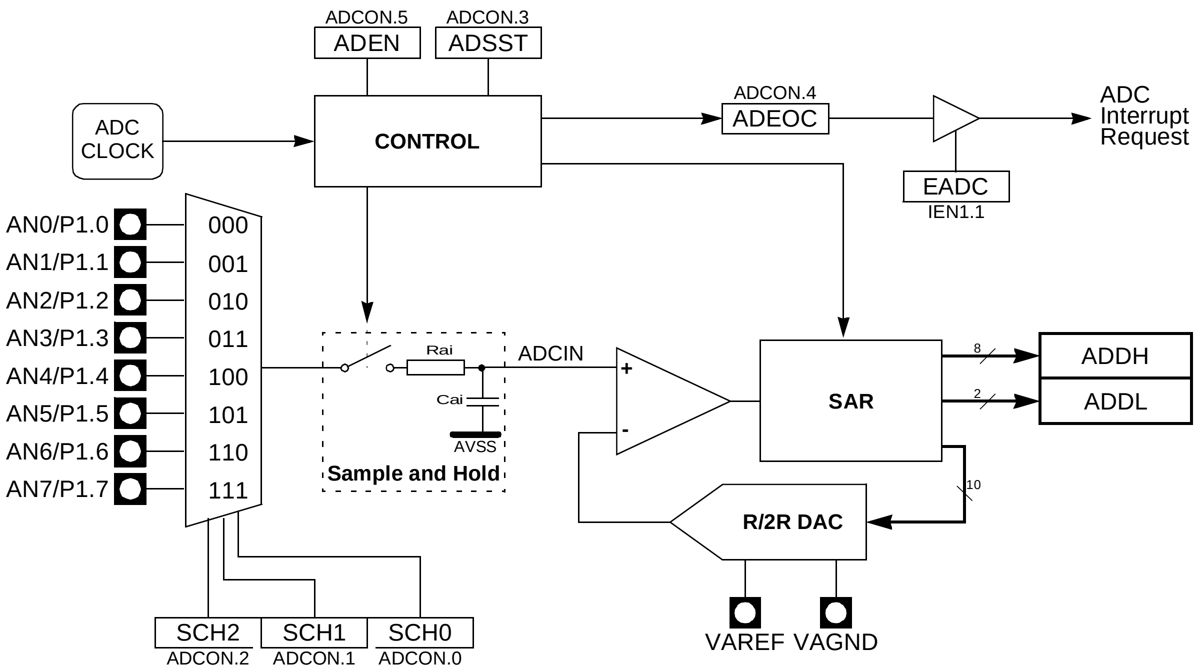
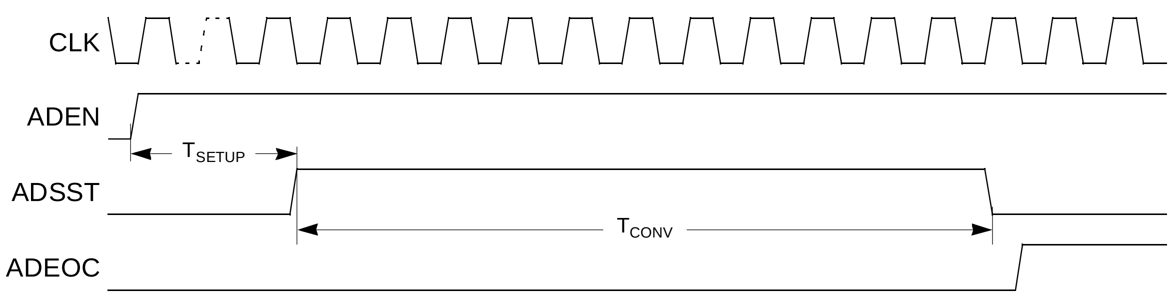


Figure 49 shows the timing diagram of a complete conversion. For simplicity, the figure depicts the waveforms in idealized form and do not provide precise timing information. For ADC characteristics and timing parameters refer to the section “AC Characteristics” of this datasheet.

Figure 49. Timing Diagram



Note: Tsetup min, see the AC Parameter for A/D conversion.
Tconv = 11 clock ADC = 1sample and hold + 10-bit conversion
The user must ensure that Tsetup time between setting ADEN and the start of the first conversion.

ADC Converter Operation

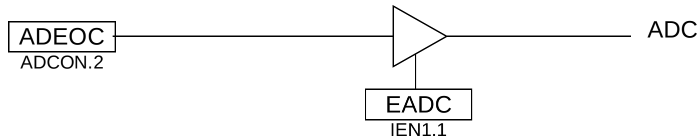
A start of single A/D conversion is triggered by setting bit ADSST (ADCON.3).

After completion of the A/D conversion, the ADSST bit is cleared by hardware.

The end-of-conversion flag ADEOC (ADCON.4) is set when the value of conversion is available in ADDH and ADDL, it must be cleared by software. If the bit EADC (IEN1.1) is set, an interrupt occur when flag ADEOC is set (See Figure 51). Clear this flag for re-arming the interrupt.

Note: Always leave Tsetup time before starting a conversion unless ADEN is permanently high. In this case one should wait Tsetup only before the first conversion

Figure 51. ADC interrupt structure



Routine Examples

```
1. Configure P1.2 and P1.3 in ADC channels
// configure channel P1.2 and P1.3 for ADC
 ADCF = 0Ch

// Enable the ADC
 ADCON = 20h
2. Start a standard conversion
// The variable 'channel' contains the channel to convert
// The variable 'value_converted' is an unsigned int
// Clear the field SCH[2:0]
 ADCON &= F8h
// Select channel
 ADCON |= channel
// Start conversion in standard mode
 ADCON |= 08h
// Wait flag End of conversion
 while((ADCON & 01h)!= 01h)
// Clear the End of conversion flag
 ADCON &= EFh
// read the value
 value_converted = (ADDH << 2)+(ADDL)

3. Start a precision conversion (need interrupt ADC)
// The variable 'channel' contains the channel to convert
// Enable ADC
 EADC = 1
// clear the field SCH[2:0]
 ADCON &= F8h
// Select the channel
 ADCON |= channel
// Start conversion in precision mode
 ADCON |= 48h
```

Note: To enable the ADC interrupt: EA = 1

Registers

Figure 53. IEN0 Register
IEN0 (S:A8h)
Interrupt Enable Register

7	6	5	4	3	2	1	0
EA	EC	ET2	ES	ET1	EX1	ET0	EX0

Bit Number	Bit Mnemonic	Description
7	EA	**Enable All Interrupt bit** Clear to disable all interrupts. Set to enable all interrupts. If EA=1, each interrupt source is individually enabled or disabled by setting or clearing its interrupt enable bit.
6	EC	**PCA Interrupt Enable** Clear to disable the PCA interrupt. Set to enable the PCA interrupt.
5	ET2	**Timer 2 Overflow Interrupt Enable bit** Clear to disable Timer 2 overflow interrupt. Set to enable Timer 2 overflow interrupt.
4	ES	**Serial port Enable bit** Clear to disable serial port interrupt. Set to enable serial port interrupt.
3	ET1	**Timer 1 Overflow Interrupt Enable bit** Clear to disable timer 1 overflow interrupt. Set to enable timer 1 overflow interrupt.
2	EX1	**External Interrupt 1 Enable bit** Clear to disable external interrupt 1. Set to enable external interrupt 1.
1	ET0	**Timer 0 Overflow Interrupt Enable bit** Clear to disable timer 0 overflow interrupt. Set to enable timer 0 overflow interrupt.
0	EX0	**External Interrupt 0 Enable bit** Clear to disable external interrupt 0. Set to enable external interrupt 0.

Reset Value = 0000 0000b
bit addressable

AC Parameters

Serial Port Timing - Shift Register Mode

Table 115. Symbol Description (F = 40 MHz)

Symbol	Parameter
T_{XLXL}	Serial port clock cycle time
T_{QVHX}	Output data set-up to clock rising edge
T_{XHQX}	Output data hold after clock rising edge
T_{XHDX}	Input data hold after clock rising edge
T_{XHDV}	Clock rising edge to input data valid

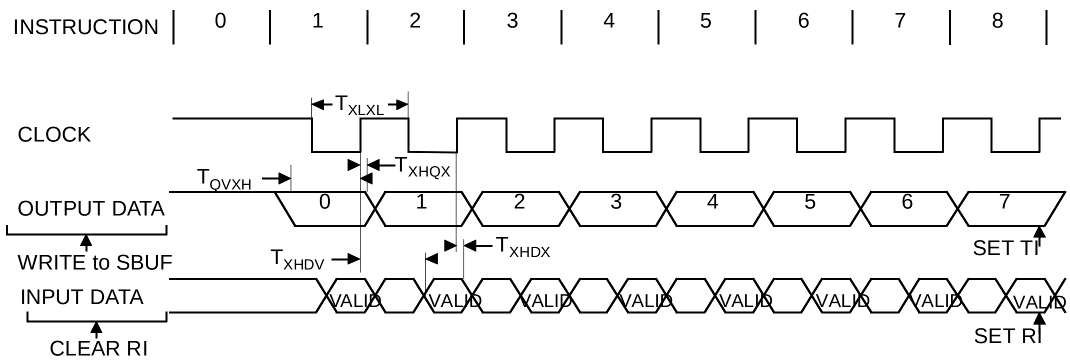
Table 116. AC Parameters for a Fix Clock (F = 40 MHz)

Symbol	Min	Max	Units
T_{XLXL}	300		ns
T_{QVHX}	200		ns
T_{XHQX}	30		ns
T_{XHDX}	0		ns
T_{XHDV}		117	ns

Table 117. AC Parameters for a Variable Clock

Symbol	Type	Standard Clock	X2 Clock	x parameter for -M range	Units
T_{XLXL}	Min	12 T	6 T		ns
T_{QVHX}	Min	10 T - x	5 T - x	50	ns
T_{XHQX}	Min	2 T - x	T - x	20	ns
T_{XHDX}	Min	x	x	0	ns
T_{XHDV}	Max	10 T - x	5 T- x	133	ns

Shift Register Timing Waveforms

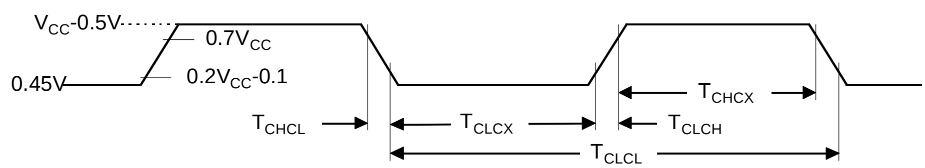


External Clock Drive Characteristics (XTAL1)

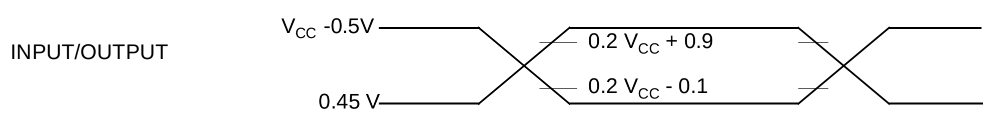
Table 118. AC Parameters

Symbol	Parameter	Min	Max	Units
T_{CLCL}	Oscillator Period	25		ns
T_{CHCX}	High Time	5		ns
T_{CLCX}	Low Time	5		ns
T_{CLCH}	Rise Time		5	ns
T_{CHCL}	Fall Time		5	ns
T_{CHCX}/T_{CLCX}	Cyclic ratio in X2 Mode	40	60	%

External Clock Drive Waveforms

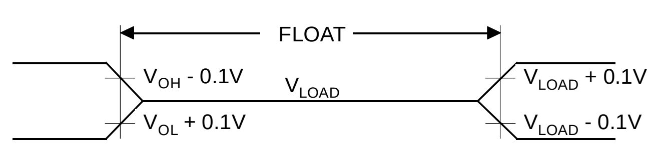


AC Testing Input/Output Waveforms

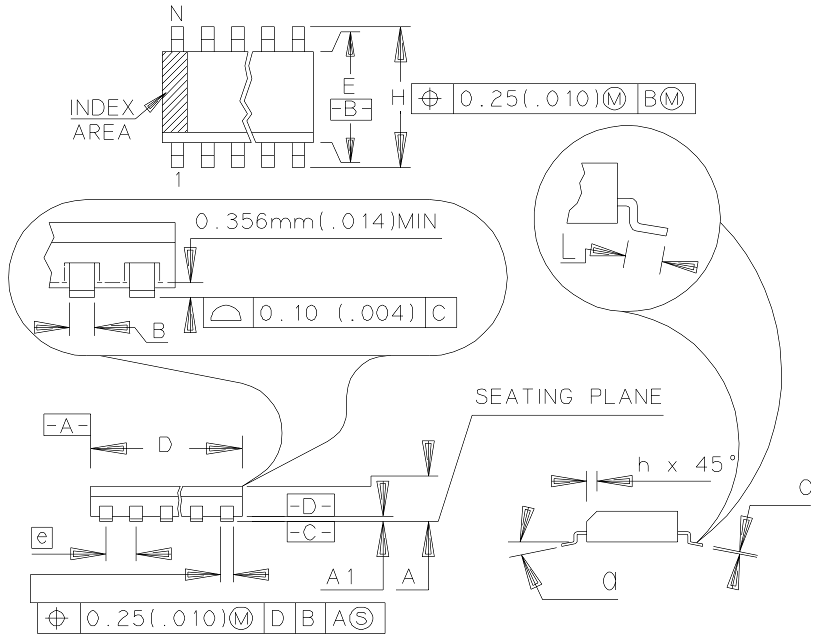


AC inputs during testing are driven at V_{CC} - 0.5 for a logic “1” and 0.45V for a logic “0”. Timing measurement are made at V_{IH} min for a logic “1” and V_{IL} max for a logic “0”.

Float Waveforms



SOIC28



	MM		INCH	
A	2.35	2.65	.093	.104
A1	0.10	0.30	.004	.012
B	0.35	0.49	.014	.019
C	0.23	0.32	.009	.013
D	17.70	18.10	.697	.713
E	7.40	7.60	.291	.299
e	1.27	BSC	.050	BSC
H	10.00	10.65	.394	.419
h	0.25	0.75	.010	.029
L	0.40	1.27	.016	.050
N	28		28	
α	0°		8°	