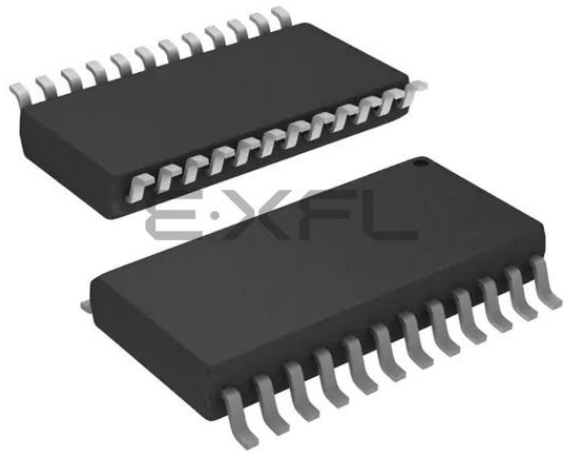

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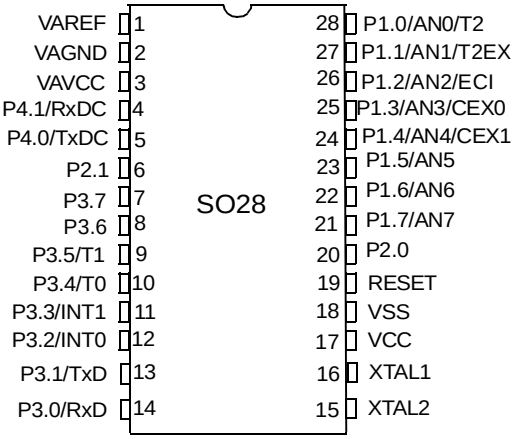
What is "Embedded - Microcontrollers"?

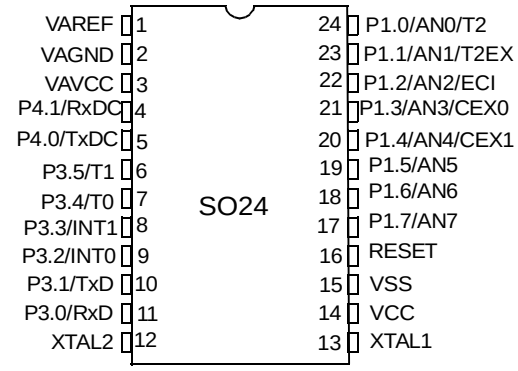
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

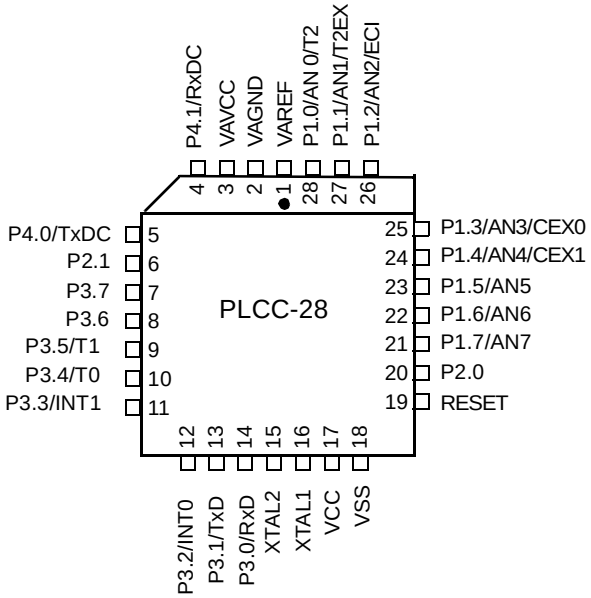
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	80C51
Core Size	8-Bit
Speed	40MHz
Connectivity	CANbus, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	20
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	24-SOIC (0.295", 7.50mm Width)
Supplier Device Package	24-SO
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/t89c51cc02ua-tdsim

Pin Configurations







Pin Name	Type	Description
P3.0:7	I/O	**Port 3:** Is an 8-bit bi-directional I/O port with internal pull-ups. Port 3 pins that have 1's written to them are pulled high by the internal pull-up transistors and can be used as inputs in this state. As inputs, Port 3 pins that are being pulled low externally will be a source of current (I_{IL}, See section 'Electrical Characteristic') because of the internal pull-ups. The output latch corresponding to a secondary function must be programmed to one for that function to operate (except for TxD and $\overline{WR}$). The secondary functions are assigned to the pins of port 3 as follows: P3.0/RxD: Receiver data input (asynchronous) or data input/output (synchronous) of the serial interface P3.1/TxD: Transmitter data output (asynchronous) or clock output (synchronous) of the serial interface P3.2/$\overline{INT0}$: External interrupt 0 input/timer 0 gate control input P3.3/$\overline{INT1}$: External interrupt 1 input/timer 1 gate control input P3.4/T0: Timer 0 counter input P3.5/T1: Timer 1 counter input P3.6: Regular I/O port pin P3.7: Regular I/O port pin
P4.0:1	I/O	**Port 4:** Is an 2-bit bi-directional I/O port with internal pull-ups. Port 4 pins that have 1's written to them are pulled high by the internal pull-ups and can be used as inputs in this state. As inputs, Port 4 pins that are being pulled low externally will be a source of current (IIL, on the datasheet) because of the internal pull-up transistor. The output latch corresponding to a secondary function RxDC must be programmed to one for that function to operate. The secondary functions are assigned to the two pins of port 4 as follows: P4.0/TxDC: Transmitter output of CAN controller P4.1/RxDC: Receiver input of CAN controller. It can drive CMOS inputs without external pull-ups.
RESET	I/O	**Reset:** A high level on this pin during two machine cycles while the oscillator is running resets the device. An internal pull-down resistor to VSS permits power-on reset using only an external capacitor to VCC.
XTAL1	I	**XTAL1:** Input of the inverting oscillator amplifier and input of the internal clock generator circuits. To drive the device from an external clock source, XTAL1 should be driven, while XTAL2 is left unconnected. To operate above a frequency of 16 MHz, a duty cycle of 50% should be maintained.
XTAL2	O	**XTAL2:** Output from the inverting oscillator amplifier.

I/O Configurations

Each Port SFR operates via type-D latches, as illustrated in Figure 1 for Ports 3 and 4. A CPU 'write to latch' signal initiates transfer of internal bus data into the type-D latch. A CPU 'read latch' signal transfers the latched Q output onto the internal bus. Similarly, a 'read pin' signal transfers the logical level of the Port pin. Some Port data instructions activate the 'read latch' signal while others activate the 'read pin' signal. Latch instructions are referred to as Read-Modify-Write instructions. Each I/O line may be independently programmed as input or output.

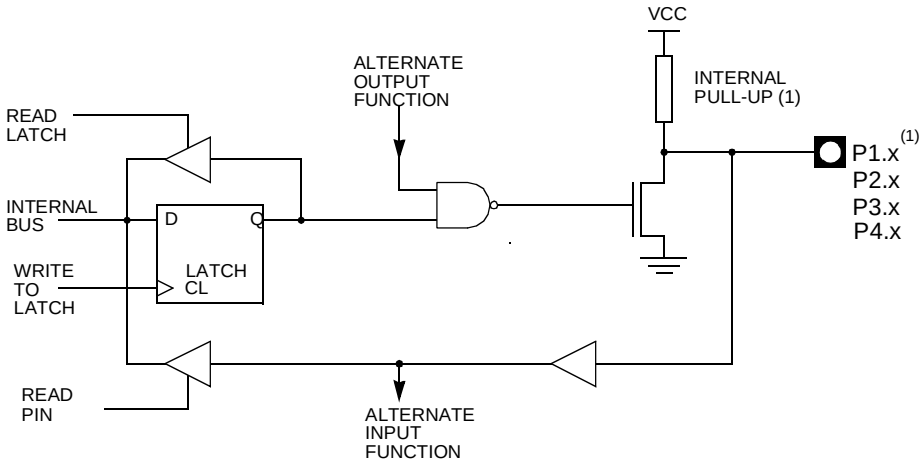
Port Structure

Figure 1 shows the structure of Ports, which have internal pull-ups. An external source can pull the pin low. Each Port pin can be configured either for general-purpose I/O or for its alternate input output function.

To use a pin for general-purpose output, set or clear the corresponding bit in the Px register (x = 1 to 4). To use a pin for general-purpose input, set the bit in the Px register. This turns off the output FET drive.

To configure a pin for its alternate function, set the bit in the Px register. When the latch is set, the 'alternate output function' signal controls the output level (See Figure 1). The operation of Ports is discussed further in 'Quasi-Bi-directional Port Operation' paragraph.

Figure 1. Ports Structure



Note: 1. The internal pull-up can be disabled on P1 when analog function is selected.

Register

Table 12. CKCON Register
CKCON (S:8Fh)
Clock Control Register

7	6	5	4	3	2	1	0
CANX2	**WDX2**	**PCAX2**	**SIX2**	**T2X2**	**T1X2**	**T0X2**	**X2**

Bit Number	Bit Mnemonic	Description
7	CANX2	**CAN Clock** (1) Clear to select 6 clock periods per peripheral clock cycle. Set to select 12 clock periods per peripheral clock cycle.
6	WDX2	**Watchdog Clock** (1) Clear to select 6 clock periods per peripheral clock cycle. Set to select 12 clock periods per peripheral clock cycle.
5	PCAX2	**Programmable Counter Array Clock** (1) Clear to select 6 clock periods per peripheral clock cycle. Set to select 12 clock periods per peripheral clock cycle.
4	SIX2	**Enhanced UART clock (MODE 0 and 2)** (1) Clear to select 6 clock periods per peripheral clock cycle. Set to select 12 clock periods per peripheral clock cycle.
3	T2X2	**Timer 2 Clock** (1) Clear to select 6 clock periods per peripheral clock cycle. Set to select 12 clock periods per peripheral clock cycle.
2	T1X2	**Timer 1 Clock** (1) Clear to select 6 clock periods per peripheral clock cycle. Set to select 12 clock periods per peripheral clock cycle.
1	T0X2	**Timer 0 Clock** (1) Clear to select 6 clock periods per peripheral clock cycle. Set to select 12 clock periods per peripheral clock cycle.
0	X2	**CPU Clock** Clear to select 12 clock periods per machine cycle (STD mode) for CPU and all the peripherals. Set to select 6 clock periods per machine cycle (X2 Mode) and to enable the individual peripherals 'X2' bits.

Note: 1. This control bit is validated when the CPU clock bit X2 is set; when X2 is low, this bit has no effect.

Reset Value = 0000 0000b

Power Management

Two power reduction modes are implemented in the T89C51CC02: the Idle mode and the Power-down mode. These modes are detailed in the following sections. In addition to these power reduction modes, the clocks of the core and peripherals can be dynamically divided by 2 using the X2 Mode detailed in Section “Clock”.

Reset Pin

In order to start-up (cold reset) or to restart (warm reset) properly the microcontroller, a high level has to be applied on the RST pin. A bad level leads to a wrong initialisation of the internal registers like SFRs, PC, etc. and to unpredictable behavior of the microcontroller. A warm reset can be applied either directly on the RST pin or indirectly by an internal reset source such as a watchdog, PCA, timer, etc.

At Power-up (cold reset)

Two conditions are required before enabling a CPU start-up:

- VDD must reach the specified VDD range,
- The level on xtal1 input must be outside the specification (VIH, VIL).

If one of these two conditions are not met, the microcontroller does not start correctly and can execute an instruction fetch from anywhere in the program space. An active level applied on the RST pin must be maintained until both of the above conditions are met. A reset is active when the level VIH1 is reached and when the pulse width covers the period of time where VDD and the oscillator are not stabilized. Two parameters have to be taken into account to determine the reset pulse width:

- VDD rise time (vddrst),
- Oscillator startup time (oscrst).

To determine the capacitor the highest value of these two parameters has to be chosen. The reset circuitry is shown in Figure 5.

Figure 5. Reset Circuitry

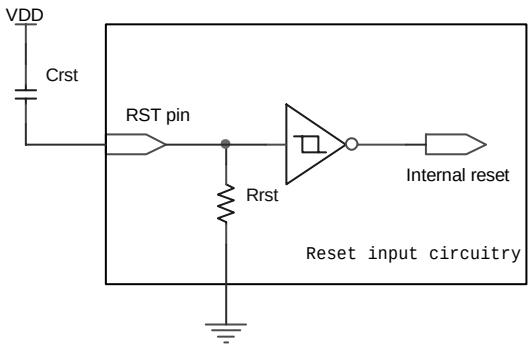


Table 13 and Table 14 give some typical examples for three values of VDD rise times, two values of oscillator start-up time and two pull-down resistor values.

Table 13. Minimum Reset Capacitor for a 50K Pull-down Resistor

oscrst/vddrst	1ms	10ms	100ms
5ms	820nF	1.2µF	12µF
20ms	2.7µF	3.9µF	12µF

Exiting Power-down Mode

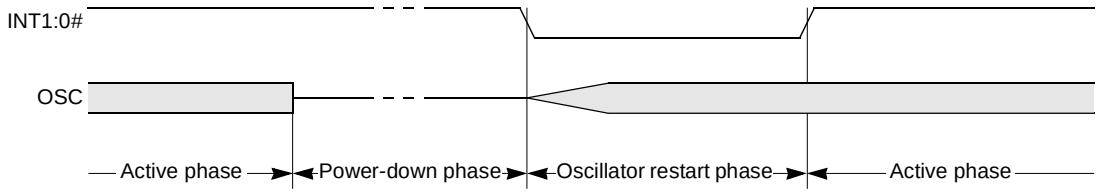
Note: If V_{DD} was reduced during the Power-down mode, do not exit Power-down mode until V_{DD} is restored to the normal operating level.

There are two ways to exit the Power-down mode:

1. Generate an enabled external interrupt.
   – The T89C51CC02 provides capability to exit from Power-down using INT0#, INT1#.
   Hardware clears PD bit in PCON register which starts the oscillator and restores the clocks to the CPU and peripherals. Using INTx# input, execution resumes when the input is released (See Figure 8). Execution resumes with the interrupt service routine. Upon completion of the interrupt service routine, program execution resumes with the instruction immediately following the instruction that activated Power-down mode.

Notes:
1. The external interrupt used to exit Power-down mode must be configured as level sensitive (INT0# and INT1#) and must be assigned the highest priority. In addition, the duration of the interrupt must be long enough to allow the oscillator to stabilize. The execution will only resume when the interrupt is deasserted.
2. Exit from power-down by external interrupt does not affect the SFRs nor the internal RAM content.

Figure 8. Power-down Exit Waveform Using INT1:0#



2. Generate a reset.
   – A logic high on the RST pin clears PD bit in PCON register directly and asynchronously. This starts the oscillator and restores the clock to the CPU and peripherals. Program execution momentarily resumes with the instruction immediately following the instruction that activated Power-down mode and may continue for a number of clock cycles before the internal reset algorithm takes control. Reset initializes the T89C51CC02 and vectors the CPU to address 0000h.

Notes:
1. During the time that execution resumes, the internal RAM cannot be accessed; however, it is possible for the Port pins to be accessed. To avoid unexpected outputs at the Port pins, the instruction immediately following the instruction that activated the Power-down mode should not write to a Port pin or to the external RAM.
2. Exit from power-down by reset redefines all the SFRs, but does not affect the internal RAM content.

Data Memory

The T89C51CC02 provides data memory access in two different spaces:

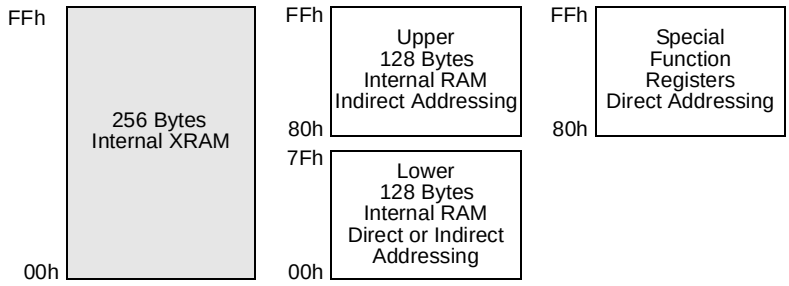
The internal space mapped in three separate segments:

- The lower 128 Bytes RAM segment.
- The upper 128 Bytes RAM segment.
- The expanded 256 Bytes RAM segment (XRAM).

A fourth internal segment is available but dedicated to Special Function Registers, SFRs, (addresses 80h to FFh) accessible by direct addressing mode.

Figure 9 shows the internal data memory spaces organization.

Figure 9. Internal memory - RAM



Internal Space

Lower 128 Bytes RAM

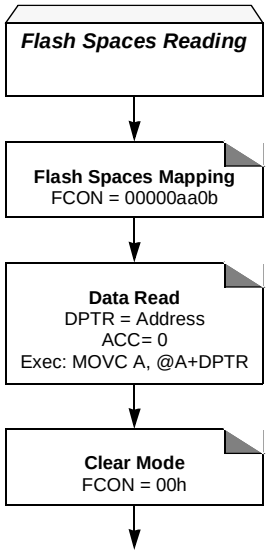
The lower 128 Bytes of RAM (See Figure 10) are accessible from address 00h to 7Fh using direct or indirect addressing modes. The lowest 32 Bytes are grouped into 4 banks of 8 registers (R0 to R7). Two bits RS0 and RS1 in PSW register (See Table 17) select which bank is in use according to Table 16. This allows more efficient use of code space, since register instructions are shorter than instructions that use direct addressing, and can be used for context switching in interrupt service routines.

Table 16. Register Bank Selection

RS1	RS0	Description
0	0	Register bank 0 from 00h to 07h
0	1	Register bank 0 from 08h to 0Fh
1	0	Register bank 0 from 10h to 17h
1	1	Register bank 0 from 18h to 1Fh

The next 16 Bytes above the register banks form a block of bit-addressable memory space. The C51 instruction set includes a wide selection of singlebit instructions, and the 128 bits in this area can be directly addressed by these instructions. The bit addresses in this area are 00h to 7Fh.

Figure 17. Reading Procedure



Note: aa = 10 for the Hardware Security Byte.

Flash Protection from Parallel Programming

The three lock bits in Hardware Security Byte (See 'In-System Programming' section) are programmed according to Table 23 provide different level of protection for the on-chip code and data located in FM0 and FM1.

The only way to write this bits are the parallel mode. They are set by default to level 3.

Table 23. Program Lock bit

Program Lock bits				
Security Level	LB0	LB1	LB2	**Protection Description**
1	U	U	U	No program lock features enabled. MOVC instruction executed from external program memory returns code data.
2	P	U	U	Parallel programming of the Flash is disabled.
3	U	P	U	Same as 2, also verify through parallel programming interface is disabled. This is the factory defaul programming.

Note: 1. Program Lock bits
U: unprogrammed
P: programmed

WARNING: Security level 2 and 3 should only be programmed after Flash and Core verification.

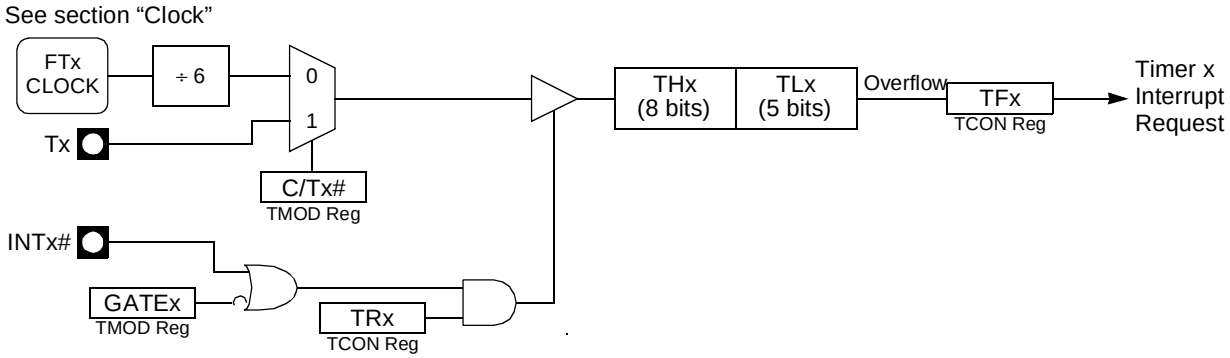
Preventing Flash Corruption

See Section "Power Management".

Mode 0 (13-bit Timer)

Mode 0 configures Timer 0 as an 13-bit Timer which is set up as an 8-bit Timer (TH0 register) with a modulo 32 prescaler implemented with the lower five bits of TL0 register (See Figure 24). The upper three bits of TL0 register are indeterminate and should be ignored. Prescaler overflow increments TH0 register.

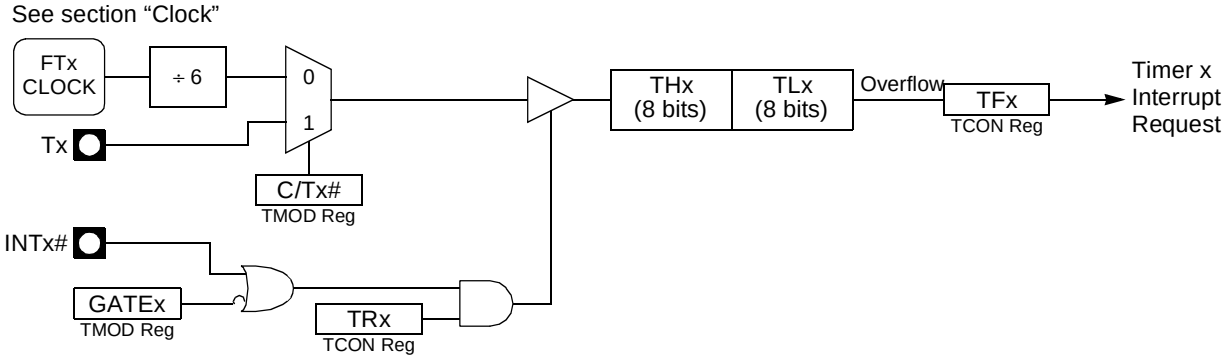
Figure 24. Timer/Counter x (x= 0 or 1) in Mode 0



Mode 1 (16-bit Timer)

Mode 1 configures Timer 0 as a 16-bit Timer with TH0 and TL0 registers connected in cascade (See Figure 25). The selected input increments TL0 register.

Figure 25. Timer/Counter x (x= 0 or 1) in Mode 1



Mode 2 (8-bit Timer with Auto-Reload)

Mode 2 configures Timer 0 as an 8-bit Timer (TL0 register) that automatically reloads from TH0 register (See Figure 26). TL0 overflow sets TF0 flag in TCON register and reloads TL0 with the contents of TH0, which is preset by software. When the interrupt request is serviced, hardware clears TF0. The reload leaves TH0 unchanged. The next reload value may be changed at any time by writing it to TH0 register.

Table 38. TMOD Register
TMOD (S:89h)
Timer/Counter Mode Control Register

7	6	5	4	3	2	1	0
GATE1	**C/T1#**	**M11**	**M01**	**GATE0**	**C/T0#**	**M10**	**M00**

Bit Number	Bit Mnemonic	Description
7	GATE1	**Timer 1 Gating Control bit** Clear to enable Timer 1 whenever TR1 bit is set. Set to enable Timer 1 only while INT1# pin is high and TR1 bit is set.
6	C/T1#	**Timer 1 Counter/Timer Select bit** Clear for Timer operation: Timer 1 counts the divided-down system clock. Set for Counter operation: Timer 1 counts negative transitions on external pin T1.
5	M11	**Timer 1 Mode Select bits** M11 M01 Operating mode 0 0 Mode 0: 8-bit Timer/Counter (TH1) with 5bit prescaler (TL1). 0 1 Mode 1: 16-bit Timer/Counter. 1 1 Mode 3: Timer 1 halted. Retains count. 1 0 Mode 2: 8-bit auto-reload Timer/Counter (TL1).(1)
4	M01	
3	GATE0	**Timer 0 Gating Control bit** Clear to enable Timer 0 whenever TR0 bit is set. Set to enable Timer/Counter 0 only while INT0# pin is high and TR0 bit is set.
2	C/T0#	**Timer 0 Counter/Timer Select bit** Clear for Timer operation: Timer 0 counts the divided-down system clock. Set for Counter operation: Timer 0 counts negative transitions on external pin T0.
1	M10	**Timer 0 Mode Select bit** M10 M00 Operating mode 0 0 Mode 0: 8-bit Timer/Counter (TH0) with 5bit prescaler (TL0). 0 1 Mode 1: 16-bit Timer/Counter. 1 0 Mode 2: 8-bit auto-reload Timer/Counter (TL0).(2) 1 1 Mode 3: TL0 is an 8-bit Timer/Counter. TH0 is an 8-bit Timer using Timer 1's TR0 and TF0 bits.
0	M00	

Reset Value = 0000 0000b
Notes: 1. Reloaded from TH1 at overflow.
2. Reloaded from TH0 at overflow.

Table 39. TH0 Register
TH0 (S:8Ch)
Timer 0 High Byte Register

7	6	5	4	3	2	1	0

Bit Number	Bit Mnemonic	Description
7:0		**High Byte of Timer 0**

Reset Value = 0000 0000b

Watchdog Programming

The three lower bits (S0, S1, S2) located into WDTPRG register permit to program the WDT duration.

Table 49. Machine Cycle Count

S2	S1	S0	Machine Cycle Count
0	0	0	$2^{14} - 1$
0	0	1	$2^{15} - 1$
0	1	0	$2^{16} - 1$
0	1	1	$2^{17} - 1$
1	0	0	$2^{18} - 1$
1	0	1	$2^{19} - 1$
1	1	0	$2^{20} - 1$
1	1	1	$2^{21} - 1$

To compute WD Timeout, the following formula is applied:

$$FTime-Out = \frac{F_{wd}}{12 \times ((2^{14} \times 2^{Svalue}) - 1)}$$

Note: Svalue represents the decimal value of (S2 S1 S0)

Find Hereafter computed Timeout values for f_{OSC}XTAL = 12 MHz in X1 mode

Table 50. Timeout Computation

S2	S1	S0	f_{osc}=12 MHz	f_{osc}=16MHz	f_{osc}=20 MHz
0	0	0	16.38 ms	12.28 ms	9.82 ms
0	0	1	32.77 ms	24.57 ms	19.66 ms
0	1	0	65.54 ms	49.14 ms	39.32 ms
0	1	1	131.07 ms	98.28 ms	78.64 ms
1	0	0	262.14 ms	196.56 ms	157.28 ms
1	0	1	524.29 ms	393.12 ms	314.56 ms
1	1	0	1.05 s	786.24 ms	629.12 ms
1	1	1	2.10 s	1.57 s	1.25 ms

CAN Controller Mailbox and Registers Organization

The pagination allows management of the 91 registers including 80(4 x 20) Bytes of mailbox via 32 SFRs.
All actions on the message object window SFRs apply to the corresponding message object registers pointed by the message object number find in the Page message object register (CANPAGE) as illustrate in Figure 33.

Figure 33. CAN Controller Memory Organization

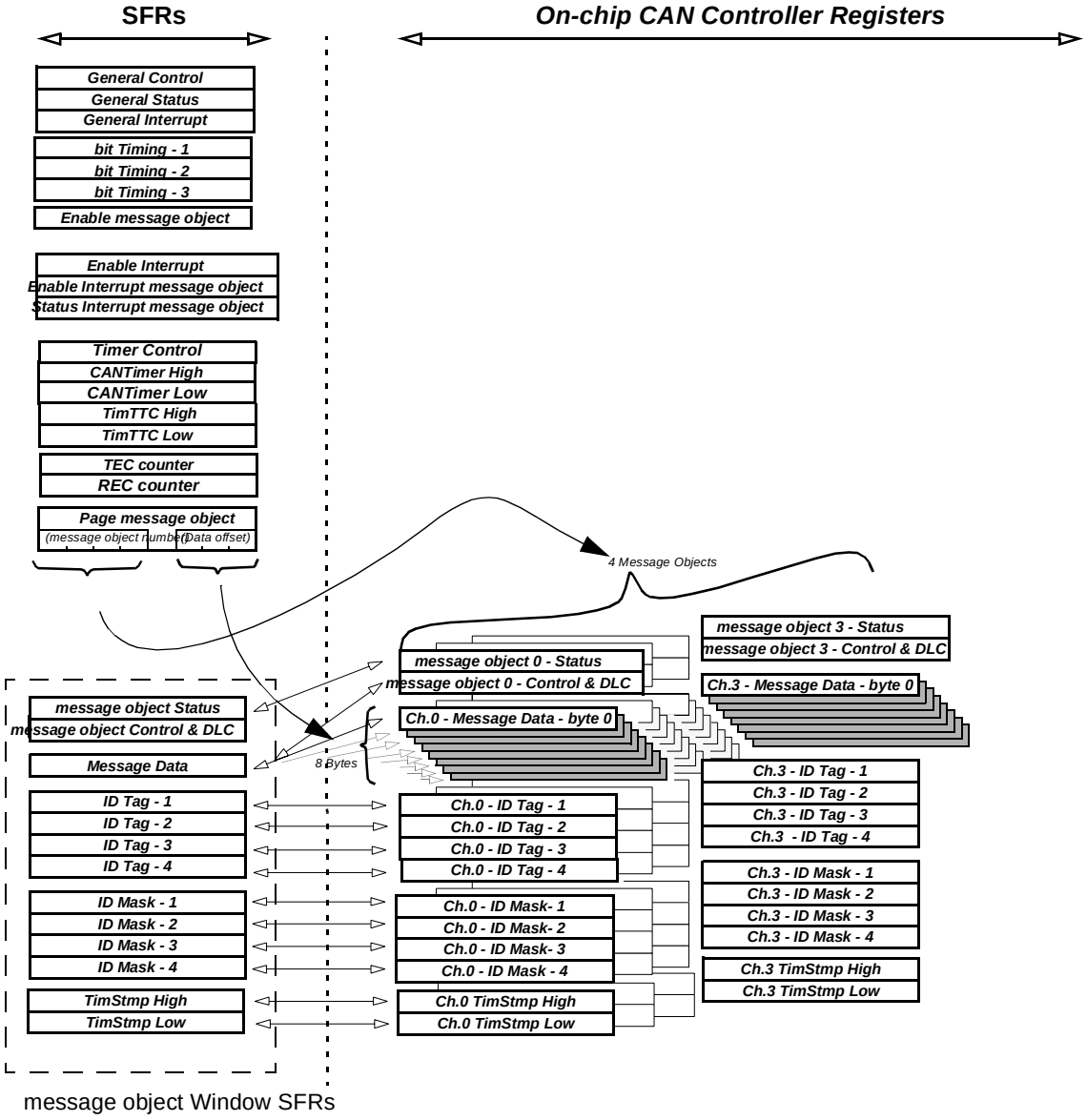
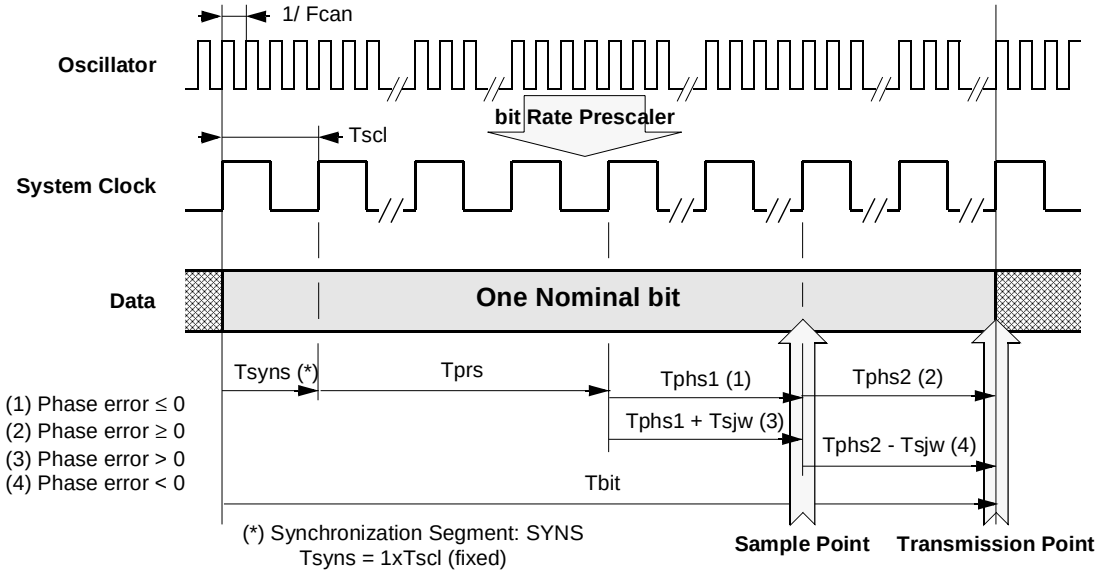


Figure 37. General Structure of a bit Period



Tbit calculation: $Tbit = Tsyns + Tprs + Tphs1 + Tphs2$

example of bit timing determination for CAN baudrate of 500 kbit/s:
F_{OSC} = 12 MHz in X1 mode => FCAN = 6MHz

Verify that the CAN baud rate you want is an integer division of FCAN clock.
FCAN/CANbaudrate = 6 MHz/500 kHz = 12
The time quanta TQ must be comprised between 8 and 25: TQ = 12 and **BRP = 0**

Define the various timing parameters: Tbit = Tsyns + Tprs + Tphs1 + Tphs2 = 12TQ
Tsyns = 1TQ and Tsjw =1TQ => **SJW = 0**
If we chose a sample point at 66.6% => Tphs2 = 4TQ => **PHS2 = 3**
Tbit = 12 = 4 + 1 + Tphs1 + Tprs, let us choose Tprs = 3 Tphs1 = 4
PHS1 = 3 and **PRS = 2**

BRP = 0 so CANBT1 = 00h
SJW = 0 and PRS = 2 so CANBT2 = 04h
PHS2 = 3 and PHS1 = 3 so CANBT3 = 36h

Table 57. CANGIT Register

CANGIT (S:9Bh)
CAN General Interrupt

7	6	5	4	3	2	1	0
CANIT	**-**	**OVRTIM**	**OVRBUF**	**SERG**	**CERG**	**FERG**	**AERG**

Bit Number	Bit Mnemonic	Description
7	CANIT	**General interrupt flag**[1] This status bit is the image of all the CAN controller interrupts sent to the interrupt controller. It can be used in the case of the polling method.
6	-	**Reserved** The values read from this bit is indeterminate. Do not set this bit.
5	OVRTIM	**Overrun CAN Timer** This status bit is set when the CAN timer switches 0xFFFF to 0x0000. If the bit ETIM in the IE1 register is set, an interrupt is generated. Clear this bit in order to reset the interrupt.
4	OVRBUF	**Overrun BUFFER** 0 - no interrupt. 1 - IT turned on This bit is set when the buffer is full. bit resetable by user. See Figure 35.
3	SERG	**Stuff Error General** Detection of more than five consecutive bits with the same polarity. This flag can generate an interrupt. resetable by user.
2	CERG	**CRC Error General** The receiver performs a CRC check on each destuffed received message from the start of frame up to the data field. If this checking does not match with the destuffed CRC field, a CRC error is set. This flag can generate an interrupt. resetable by user.
1	FERG	**Form Error General** The form error results from one or more violations of the fixed form in the following bit fields: CRC delimiter acknowledgment delimiter end_of_frame This flag can generate an interrupt. resetable by user.
0	AERG	**Acknowledgment Error General** No detection of the dominant bit in the acknowledge slot. This flag can generate an interrupt. resetable by user.

Note: 1. These fields are Read Only.

Reset Value = 0x00 0000b

Table 67. CANPAGE Register

CANPAGE (S:B1h) – CAN Message Object Page Register

7	6	5	4	3	2	1	0
-	-	CHNB 1	CHNB 0	AINC	INDX2	INDX1	INDX0

Bit Number	Bit Mnemonic	Description
7 - 6	-	**Reserved** The values read from these bits are indeterminate. Do not set these bits.
5 - 4	CHNB3:0	**Selection of Message Object Number** The available numbers are: 0 to 3(See Figure 33).
3	AINC	**Auto Increment of the Index (Active Low)** 0 - auto-increment of the index (default value). 1 - non-auto-increment of the index.
2 - 0	INDX2:0	**Index** Byte location of the data field for the defined message object (See Figure 33).

Reset Value = xx00 0000b

Table 68. CANCONCH Register

CANCONCH (S:B3h) – CAN Message Object Control and DLC Register

7	6	5	4	3	2	1	0
CONCH 1	CONCH 0	RPLV	IDE	DLC 3	DLC 2	DLC 1	DLC 0

Bit Number	Bit Mnemonic	Description
7 - 6	CONCH1:0	**Configuration of Message Object** **CONCH1 CONCH0** 0 0: disable 0 1: Launch transmission 1 0: Enable Reception 1 1: Enable Reception Buffer NOTE: The user must re-write the configuration to enable the corresponding bit in the CANEN1:2 registers.
5	RPLV	**Reply valid** Used in the automatic reply mode after receiving a remote frame 0 - reply not ready. 1 - reply ready & valid.
4	IDE	**Identifier Extension** 0 - CAN standard rev 2.0 A (ident = 11 bits). 1 - CAN standard rev 2.0 B (ident = 29 bits).
3 - 0	DLC3:0	**Data Length Code** Number of Bytes in the data field of the message. The range of DLC is from 0 up to 8. This value is updated when a frame is received (data or remote frame). If the expected DLC differs from the incoming DLC, a warning appears in the CANSTCH register.

No default value after reset

Table 73. CANIDT1 for V2.0 part A

CANIDT4 for V2.0 part A (S:BFh)
CAN Identifier Tag Registers 4

7	6	5	4	3	2	1	0
-	-	-	-	-	RTRTAG	-	RB0TAG

Bit Number	Bit Mnemonic	Description
7 - 3	-	**Reserved** The values read from these bits are indeterminate. Do not set these bits.
2	RTRTAG	Remote transmission request tag value.
1	-	**Reserved** The values read from this bit are indeterminate. Do not set these bit.
0	RB0TAG	Reserved bit 0 tag value.

No default value after reset.

Table 74. CANIDT2Register for V2.0 part A
CANIDT1 for V2.0 Part B (S:BCh)
CAN Identifier Tag Registers 1

7	6	5	4	3	2	1	0
IDT 28	IDT 27	IDT 26	IDT 25	IDT 24	IDT 23	IDT 22	IDT 21

Bit Number	Bit Mnemonic	Description
7 - 0	IDT28:21	**IDentifier Tag Value** See Figure 39.

No default value after reset.

Table 75. CANIDT2 Register for V2.0 Part B
CANIDT2 for V2.0 Part B (S:BDh)
CAN Identifier Tag Registers 2

7	6	5	4	3	2	1	0
IDT 20	IDT 19	IDT 18	IDT 17	IDT 16	IDT 15	IDT 14	IDT 13

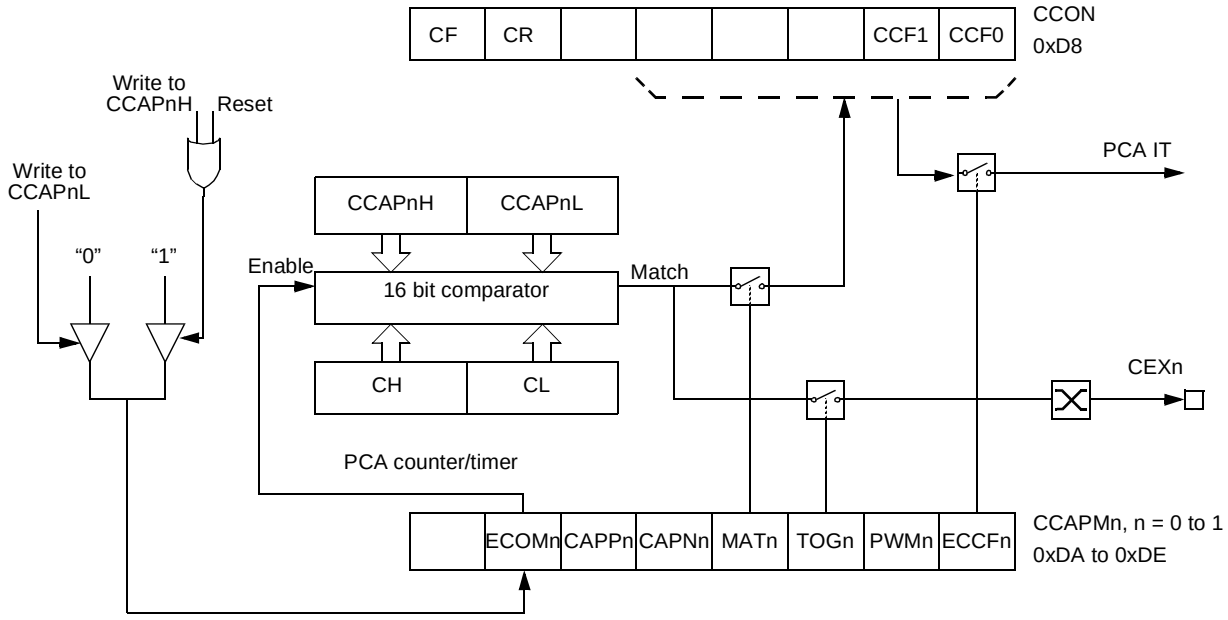
Bit Number	Bit Mnemonic	Description
7 - 0	IDT20:13	**IDentifier Tag Value** See Figure 39.

No default value after reset.

High Speed Output Mode

In this mode the CEX output (on port 1) associated with the PCA module will toggle each time a match occurs between the PCA counter and the module's capture registers. To activate this mode the TOG, MAT, and ECOM bits in the module's CCAPMn SFR must be set.

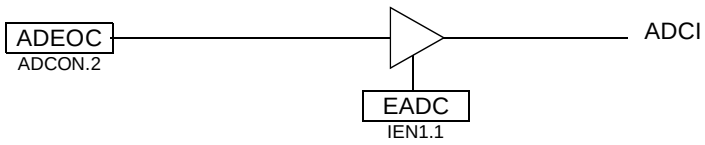
Figure 46. PCA High Speed Output Mode



Pulse Width Modulator Mode

All the PCA modules can be used as PWM outputs. The output frequency depends on the source for the PCA timer. All the modules will have the same output frequency because they all share the PCA timer. The duty cycle of each module is independently variable using the module's capture register CCAPLn. When the value of the PCA CL SFR is less than the value in the module's CCAPLn SFR the output will be low, when it is equal to or greater than it, the output will be high. When CL overflows from FF to 00, CCAPLn is reloaded with the value in CCAPHn. the allows the PWM to be updated without glitches. The PWM and ECOM bits in the module's CCAPMn register must be set to enable the PWM mode.

Figure 51. ADC interrupt structure



Routine Examples

```
1. Configure P1.2 and P1.3 in ADC channels
// configure channel P1.2 and P1.3 for ADC
 ADCF = 0Ch

// Enable the ADC
 ADCON = 20h
2. Start a standard conversion
// The variable 'channel' contains the channel to convert
// The variable 'value_converted' is an unsigned int
// Clear the field SCH[2:0]
 ADCON &= F8h
// Select channel
 ADCON |= channel
// Start conversion in standard mode
 ADCON |= 08h
// Wait flag End of conversion
 while((ADCON & 01h)!= 01h)
// Clear the End of conversion flag
 ADCON &= EFh
// read the value
 value_converted = (ADDH << 2)+(ADDL)

3. Start a precision conversion (need interrupt ADC)
// The variable 'channel' contains the channel to convert
// Enable ADC
 EADC = 1
// clear the field SCH[2:0]
 ADCON &= F8h
// Select the channel
 ADCON |= channel
// Start conversion in precision mode
 ADCON |= 48h
```

Note: To enable the ADC interrupt: EA = 1

AC Parameters

Serial Port Timing - Shift Register Mode

Table 115. Symbol Description (F = 40 MHz)

Symbol	Parameter
T_{XLXL}	Serial port clock cycle time
T_{QVHX}	Output data set-up to clock rising edge
T_{XHQX}	Output data hold after clock rising edge
T_{XHDX}	Input data hold after clock rising edge
T_{XHDV}	Clock rising edge to input data valid

Table 116. AC Parameters for a Fix Clock (F = 40 MHz)

Symbol	Min	Max	Units
T_{XLXL}	300		ns
T_{QVHX}	200		ns
T_{XHQX}	30		ns
T_{XHDX}	0		ns
T_{XHDV}		117	ns

Table 117. AC Parameters for a Variable Clock

Symbol	Type	Standard Clock	X2 Clock	x parameter for -M range	Units
T_{XLXL}	Min	12 T	6 T		ns
T_{QVHX}	Min	10 T - x	5 T - x	50	ns
T_{XHQX}	Min	2 T - x	T - x	20	ns
T_{XHDX}	Min	x	x	0	ns
T_{XHDV}	Max	10 T - x	5 T- x	133	ns

Datasheet Change Log for T89C51CC02

Changes from 4126C-10/02 to 4126D-04/03

1. Changed the endurance of Flash to 100, 000 Write/Erase cycles.
2. Added note on Flash retention formula for V_{IH1}, in Section "DC Parameters for Standard Voltage", page 141.Changes from 4129F-11/02 to 4129G-04/03
1. Changed the endurance of Flash to 100, 000 Write/Erase cycles.
2. Added note on Flash retention formula for V_{IH1}, in Section "DC Parameters for Standard Voltage", page 141.

Changes from 4126D-05/03 to 4126E - 10/03

1. Updated “Electrical Characteristics” on page 132.
2. Corrected Figure 35 on page 75.

Changes from 4126E - 10/03 to 4126F - 12/03

1. Changed value of IPDMAX to 400, Section "Absolute Maximum Ratings", page 132.
2. PCA , CPS0, register correction, Section "PCA Registers", page 113.
3. Cross Memory section added. Section "Operation Cross Memory Access", page 42.