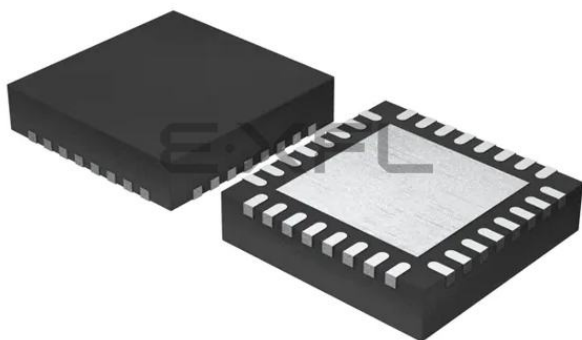




Welcome to [E-XFL.COM](https://www.e-xfl.com)

What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Discontinued at Digi-Key
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	25MHz
Connectivity	I ² C, IrDA, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I ² S, POR, PWM, WDT
Number of I/O	24
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.98V ~ 3.8V
Data Converters	A/D 4x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-VQFN Exposed Pad
Supplier Device Package	32-QFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32hg210f32g-a-qfn32

1 Ordering Information

Table 1.1 (p. 2) shows the available EFM32HG210 devices.

Table 1.1. Ordering Information

Ordering Code	Flash (kB)	RAM (kB)	Max Speed (MHz)	Supply Voltage (V)	Temperature (°C)	Package
EFM32HG210F32G-B-QFN32	32	4	25	1.98 - 3.8	-40 - 85	QFN32
EFM32HG210F64G-B-QFN32	64	8	25	1.98 - 3.8	-40 - 85	QFN32

Adding the suffix 'R' to the part number (e.g. EFM32HG210F32G-B-QFN32R) denotes tape and reel.

Visit **www.silabs.com** for information on global distributors and representatives.

There is also a read-only page in the information block containing system and device calibration data. Read and write operations are supported in the energy modes EM0 and EM1.

2.1.4 Direct Memory Access Controller (DMA)

The Direct Memory Access (DMA) controller performs memory operations independently of the CPU. This has the benefit of reducing the energy consumption and the workload of the CPU, and enables the system to stay in low energy modes when moving for instance data from the USART to RAM or from the External Bus Interface to a PWM-generating timer. The DMA controller uses the PL230 μ DMA controller licensed from ARM.

2.1.5 Reset Management Unit (RMU)

The RMU is responsible for handling the reset functionality of the EFM32HG.

2.1.6 Energy Management Unit (EMU)

The Energy Management Unit (EMU) manage all the low energy modes (EM) in EFM32HG microcontrollers. Each energy mode manages if the CPU and the various peripherals are available. The EMU can also be used to turn off the power to unused SRAM blocks.

2.1.7 Clock Management Unit (CMU)

The Clock Management Unit (CMU) is responsible for controlling the oscillators and clocks on-board the EFM32HG. The CMU provides the capability to turn on and off the clock on an individual basis to all peripheral modules in addition to enable/disable and configure the available oscillators. The high degree of flexibility enables software to minimize energy consumption in any specific application by not wasting power on peripherals and oscillators that are inactive.

2.1.8 Watchdog (WDOG)

The purpose of the watchdog timer is to generate a reset in case of a system failure, to increase application reliability. The failure may e.g. be caused by an external event, such as an ESD pulse, or by a software failure.

2.1.9 Peripheral Reflex System (PRS)

The Peripheral Reflex System (PRS) system is a network which lets the different peripheral module communicate directly with each other without involving the CPU. Peripheral modules which send out Reflex signals are called producers. The PRS routes these reflex signals to consumer peripherals which apply actions depending on the data received. The format for the Reflex signals is not given, but edge triggers and other functionality can be applied by the PRS.

2.1.10 Inter-Integrated Circuit Interface (I2C)

The I²C module provides an interface between the MCU and a serial I²C-bus. It is capable of acting as both a master and a slave, and supports multi-master buses. Both standard-mode, fast-mode and fast-mode plus speeds are supported, allowing transmission rates all the way from 10 kbit/s up to 1 Mbit/s. Slave arbitration and timeouts are also provided to allow implementation of an SMBus compliant system. The interface provided to software by the I²C module, allows both fine-grained control of the transmission process and close to automatic transfers. Automatic recognition of slave addresses is provided in all energy modes.

2.1.11 Universal Synchronous/Asynchronous Receiver/Transmitter (USART)

The Universal Synchronous Asynchronous serial Receiver and Transmitter (USART) is a very flexible serial I/O module. It supports full duplex asynchronous UART communication as well as RS-485, SPI, MicroWire and 3-wire. It can also interface with ISO7816 SmartCards, IrDA and I2S devices.

3.4 Current Consumption

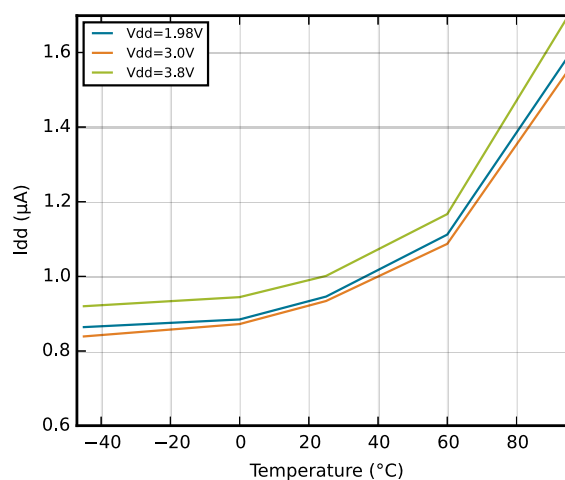
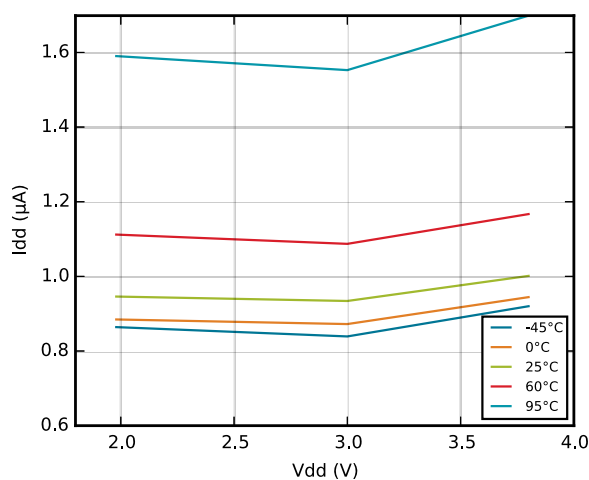
Table 3.3. Current Consumption

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I _{EM0}	EM0 current. No prescaling. Running prime number calculation code from Flash.	24 MHz HFXO, all peripheral clocks disabled, V _{DD} = 3.0 V, T _{AMB} =25°C		148	158	μA/ MHz
		24 MHz HFXO, all peripheral clocks disabled, V _{DD} = 3.0 V, T _{AMB} =85°C		153	163	μA/ MHz
		24 MHz USHFRCO, all peripheral clocks disabled, V _{DD} = 3.0 V, T _{AMB} =25°C		161	172	μA/ MHz
		24 MHz USHFRCO, all peripheral clocks disabled, V _{DD} = 3.0 V, T _{AMB} =85°C		163	174	μA/ MHz
		24 MHz HFRCO, all peripheral clocks disabled, V _{DD} = 3.0 V, T _{AMB} =25°C		127	137	μA/ MHz
		24 MHz HFRCO, all peripheral clocks disabled, V _{DD} = 3.0 V, T _{AMB} =85°C		129	139	μA/ MHz
		21 MHz HFRCO, all peripheral clocks disabled, V _{DD} = 3.0 V, T _{AMB} =25°C		131	140	μA/ MHz
		21 MHz HFRCO, all peripheral clocks disabled, V _{DD} = 3.0 V, T _{AMB} =85°C		134	143	μA/ MHz
		14 MHz HFRCO, all peripheral clocks disabled, V _{DD} = 3.0 V, T _{AMB} =25°C		134	143	μA/ MHz
		14 MHz HFRCO, all peripheral clocks disabled, V _{DD} = 3.0 V, T _{AMB} =85°C		137	145	μA/ MHz
		11 MHz HFRCO, all peripheral clocks disabled, V _{DD} = 3.0 V, T _{AMB} =25°C		136	144	μA/ MHz
		11 MHz HFRCO, all peripheral clocks disabled, V _{DD} = 3.0 V, T _{AMB} =85°C		139	148	μA/ MHz
		6.6 MHz HFRCO, all peripheral clocks disabled, V _{DD} = 3.0 V, T _{AMB} =25°C		142	150	μA/ MHz
		6.6 MHz HFRCO, all peripheral clocks disabled, V _{DD} = 3.0 V, T _{AMB} =85°C		146	154	μA/ MHz
		1.2 MHz HFRCO, all peripheral clocks disabled, V _{DD} = 3.0 V, T _{AMB} =25°C		184	196	μA/ MHz
		1.2 MHz HFRCO, all peripheral clocks disabled, V _{DD} = 3.0 V, T _{AMB} =85°C		194	208	μA/ MHz

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I _{EM1}	EM1 current	24 MHz HFXO, all peripheral clocks disabled, V _{DD} = 3.0 V, T _{AMB} =25°C		64	68	μA/ MHz
		24 MHz HFXO, all peripheral clocks disabled, V _{DD} = 3.0 V, T _{AMB} =85°C		67	71	μA/ MHz
		24 MHz USHFRCO, all peripheral clocks disabled, V _{DD} = 3.0 V, T _{AMB} =25°C		85	91	μA/ MHz
		24 MHz USHFRCO, all peripheral clocks disabled, V _{DD} = 3.0 V, T _{AMB} =85°C		86	92	μA/ MHz
		24 MHz HFRCO, all peripheral clocks disabled, V _{DD} = 3.0 V, T _{AMB} =25°C		51	55	μA/ MHz
		24 MHz HFRCO, all peripheral clocks disabled, V _{DD} = 3.0 V, T _{AMB} =85°C		52	56	μA/ MHz
		21 MHz HFRCO, all peripheral clocks disabled, V _{DD} = 3.0 V, T _{AMB} =25°C		53	57	μA/ MHz
		21 MHz HFRCO, all peripheral clocks disabled, V _{DD} = 3.0 V, T _{AMB} =85°C		54	58	μA/ MHz
		14 MHz HFRCO, all peripheral clocks disabled, V _{DD} = 3.0 V, T _{AMB} =25°C		56	59	μA/ MHz
		14 MHz HFRCO, all peripheral clocks disabled, V _{DD} = 3.0 V, T _{AMB} =85°C		57	61	μA/ MHz
		11 MHz HFRCO, all peripheral clocks disabled, V _{DD} = 3.0 V, T _{AMB} =25°C		58	61	μA/ MHz
		11 MHz HFRCO, all peripheral clocks disabled, V _{DD} = 3.0 V, T _{AMB} =85°C		59	63	μA/ MHz
		6.6 MHz HFRCO, all peripheral clocks disabled, V _{DD} = 3.0 V, T _{AMB} =25°C		64	68	μA/ MHz
		6.6 MHz HFRCO, all peripheral clocks disabled, V _{DD} = 3.0 V, T _{AMB} =85°C		67	71	μA/ MHz
		1.2 MHz HFRCO. all peripheral clocks disabled, V _{DD} = 3.0 V, T _{AMB} =25°C		106	114	μA/ MHz
		1.2 MHz HFRCO. all peripheral clocks disabled, V _{DD} = 3.0 V, T _{AMB} =85°C		114	126	μA/ MHz
I _{EM2}	EM2 current	EM2 current with RTC prescaled to 1 Hz, 32.768 kHz LFRCO, V _{DD} = 3.0 V, T _{AMB} =25°C		0.9	1.35	μA

3.4.3 EM2 Current Consumption

Figure 3.11. EM2 current consumption. RTC prescaled to 1kHz, 32.768 kHz LFRCO.



3.4.4 EM3 Current Consumption

Figure 3.12. EM3 current consumption.

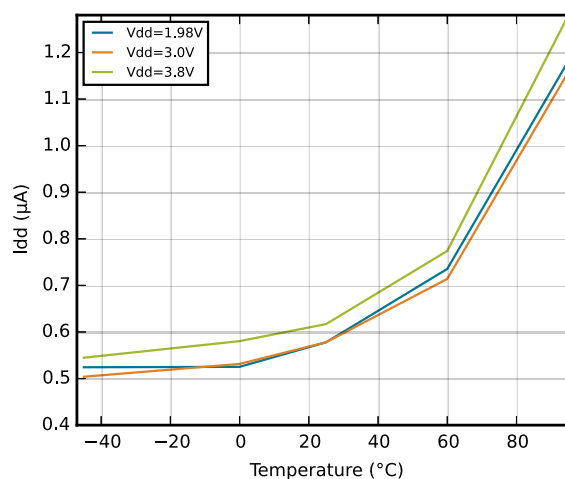
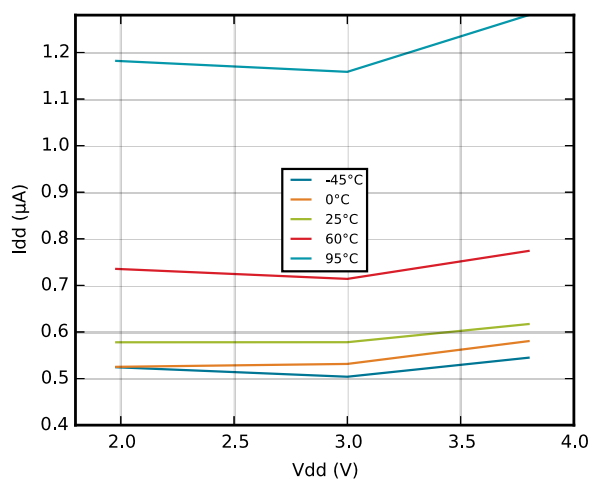
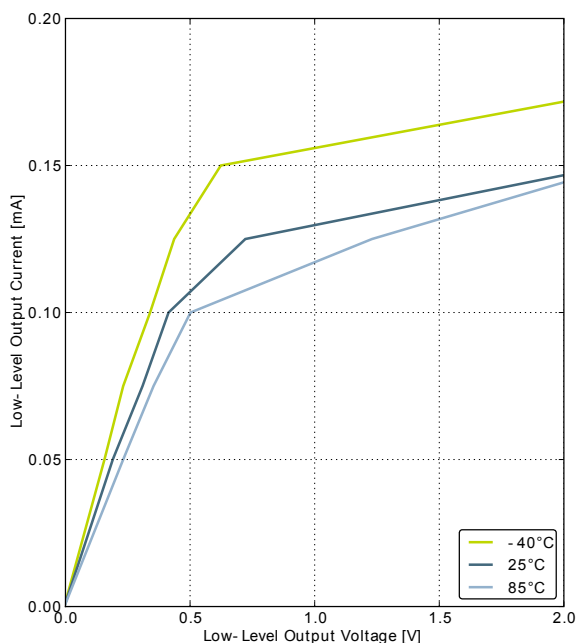
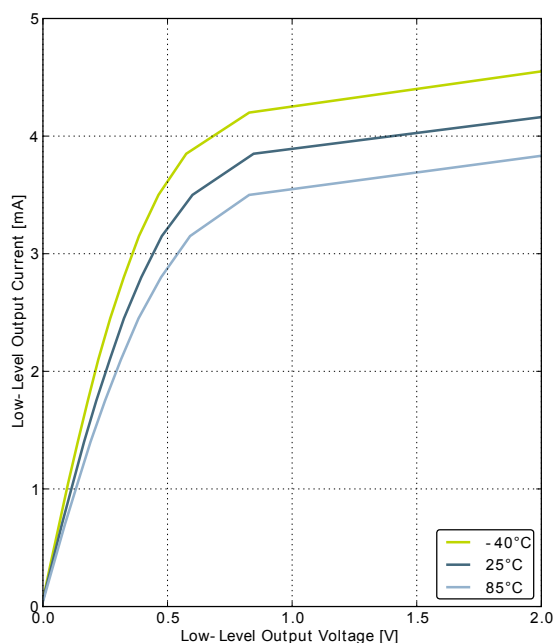


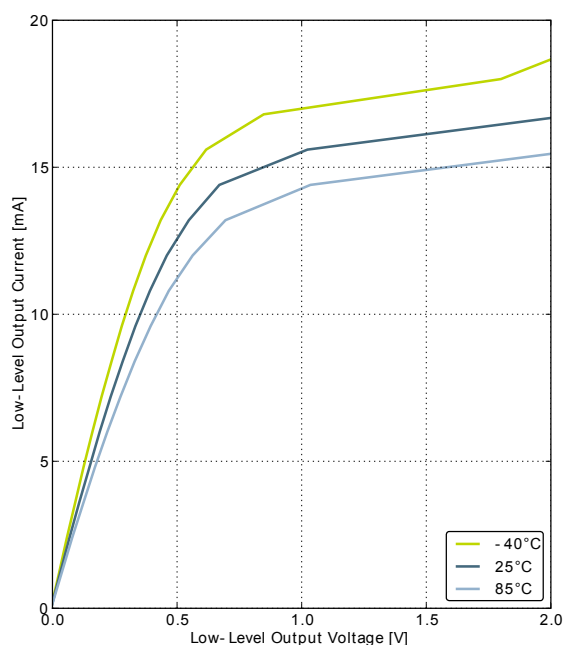
Figure 3.14. Typical Low-Level Output Current, 2V Supply Voltage



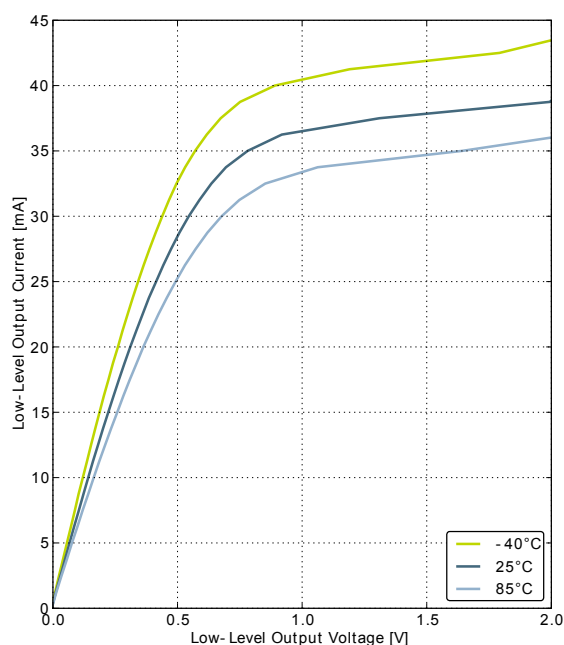
GPIO_Px_CTRL DRIVEMODE = LOWEST



GPIO_Px_CTRL DRIVEMODE = LOW

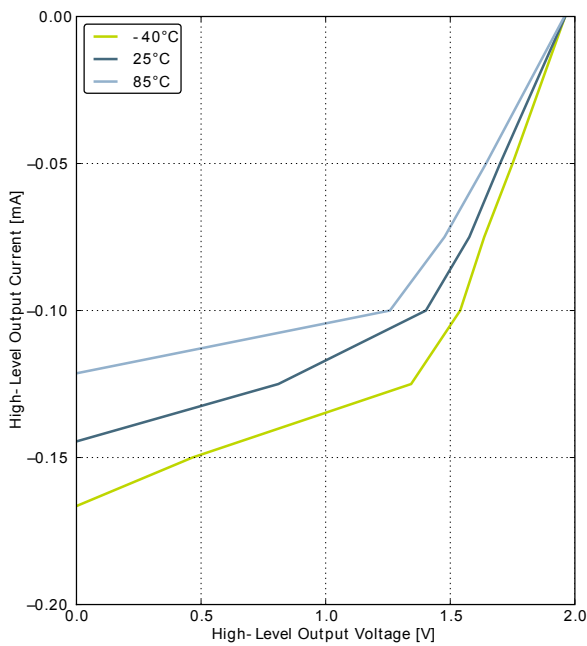


GPIO_Px_CTRL DRIVEMODE = STANDARD

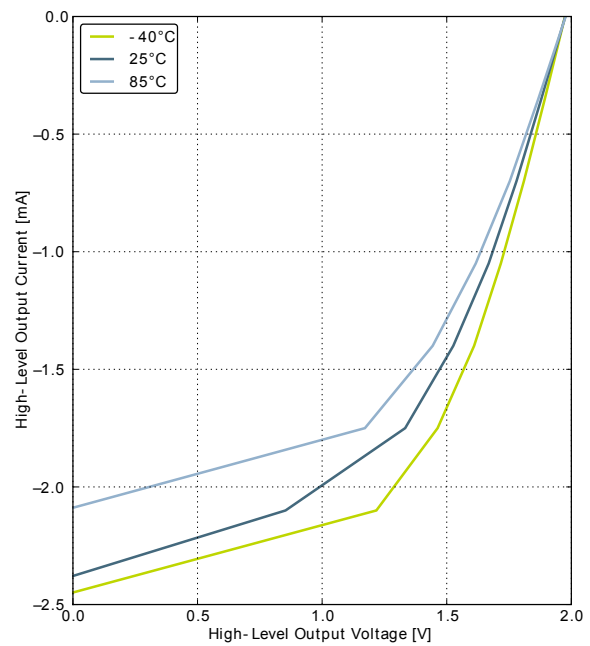


GPIO_Px_CTRL DRIVEMODE = HIGH

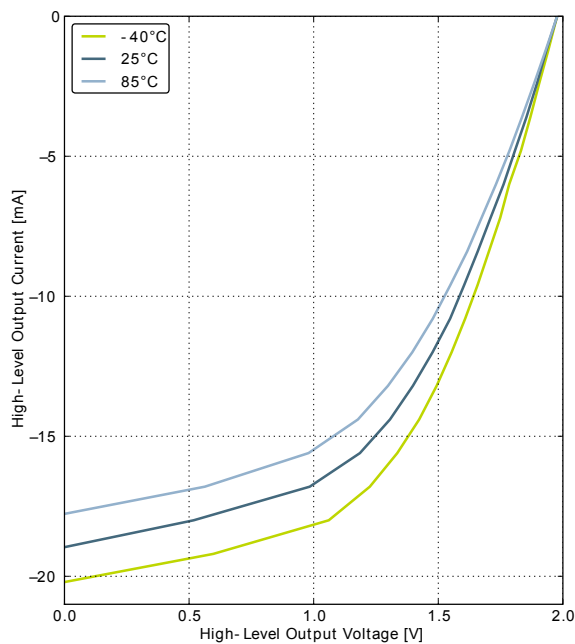
Figure 3.15. Typical High-Level Output Current, 2V Supply Voltage



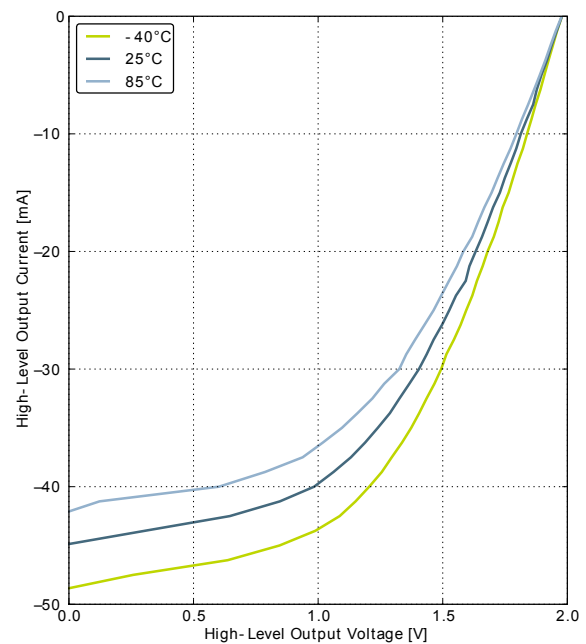
GPIO_Px_CTRL DRIVEMODE = LOWEST



GPIO_Px_CTRL DRIVEMODE = LOW



GPIO_Px_CTRL DRIVEMODE = STANDARD



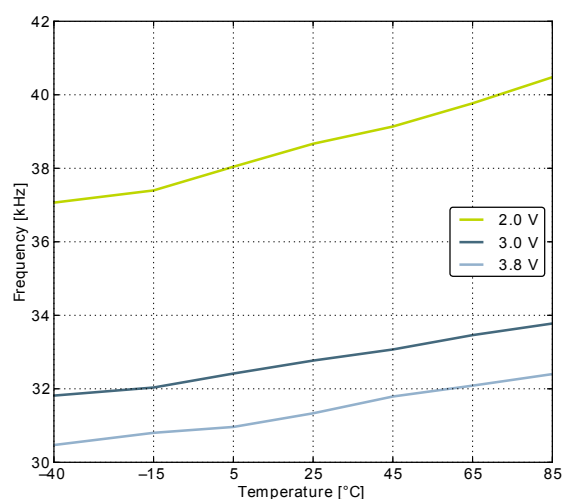
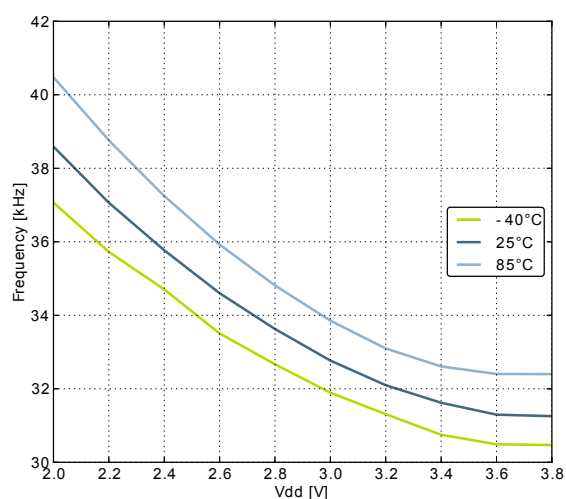
GPIO_Px_CTRL DRIVEMODE = HIGH

3.9.3 LFRCO

Table 3.10. LFRCO

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{LFRCO}	Oscillation frequency, $V_{\text{DD}} = 3.0 \text{ V}$, $T_{\text{AMB}} = 25^\circ\text{C}$		31.3	32.768	34.3	kHz
t_{LFRCO}	Startup time not including software calibration			150		μs
I_{LFRCO}	Current consumption			361	492	nA
TUNESTEP _{LFRCO}	Frequency step for LSB change in TUNING value			202		Hz

Figure 3.20. Calibrated LFRCO Frequency vs Temperature and Supply Voltage



Symbol	Parameter	Condition	Min	Typ	Max	Unit
$V_{ADCCMIN}$	Common mode input range		0		V_{DD}	V
I_{ADCIN}	Input current	2pF sampling capacitors		<100		nA
$CMRR_{ADC}$	Analog input common mode rejection ratio			65		dB
I_{ADC}	Average active current	1 MSamples/s, 12 bit, external reference		392	510	μA
		10 kSamples/s 12 bit, internal 1.25 V reference, WARMUP-MODE in ADCn_CTRL set to 0b00		67		μA
		10 kSamples/s 12 bit, internal 1.25 V reference, WARMUP-MODE in ADCn_CTRL set to 0b01		63		μA
		10 kSamples/s 12 bit, internal 1.25 V reference, WARMUP-MODE in ADCn_CTRL set to 0b10		64		μA
		10 kSamples/s 12 bit, internal 1.25 V reference, WARMUP-MODE in ADCn_CTRL set to 0b11		244		μA
I_{ADCREf}	Current consumption of internal voltage reference	Internal voltage reference		65		μA
C_{ADCIN}	Input capacitance			2		pF
R_{ADCIN}	Input ON resistance		1			MOhm
$R_{ADCfilt}$	Input RC filter resistance			10		kOhm
$C_{ADCfilt}$	Input RC filter/de-coupling capacitance			250		fF
f_{ADCCLK}	ADC Clock Frequency				13	MHz
$t_{ADCCONV}$	Conversion time	6 bit	7			ADC-CLK Cycles
		8 bit	11			ADC-CLK Cycles
		12 bit	13			ADC-CLK Cycles
t_{ADCACQ}	Acquisition time	Programmable	1		256	ADC-CLK Cycles
$t_{ADCACQVDD3}$	Required acquisition time for VDD/3 reference		2			μs

Symbol	Parameter	Condition	Min	Typ	Max	Unit
		1 MSamples/s, 12 bit, differential, internal 1.25V reference		60		dB
		1 MSamples/s, 12 bit, differential, internal 2.5V reference		64		dB
		1 MSamples/s, 12 bit, differential, 5V reference		54		dB
		1 MSamples/s, 12 bit, differential, V_{DD} reference		66		dB
		1 MSamples/s, 12 bit, differential, $2xV_{DD}$ reference		68		dB
		200 kSamples/s, 12 bit, single ended, internal 1.25V reference		61		dB
		200 kSamples/s, 12 bit, single ended, internal 2.5V reference		65		dB
		200 kSamples/s, 12 bit, single ended, V_{DD} reference		66		dB
		200 kSamples/s, 12 bit, differential, internal 1.25V reference		63		dB
		200 kSamples/s, 12 bit, differential, internal 2.5V reference		66		dB
		200 kSamples/s, 12 bit, differential, 5V reference		66		dB
		200 kSamples/s, 12 bit, differential, V_{DD} reference	62	66		dB
		200 kSamples/s, 12 bit, differential, $2xV_{DD}$ reference		69		dB
SFDR _{ADC}	Spurious-Free Dynamic Range (SFDR)	1 MSamples/s, 12 bit, single ended, internal 1.25V reference		64		dBc
		1 MSamples/s, 12 bit, single ended, internal 2.5V reference		76		dBc
		1 MSamples/s, 12 bit, single ended, V_{DD} reference		73		dBc
		1 MSamples/s, 12 bit, differential, internal 1.25V reference		66		dBc
		1 MSamples/s, 12 bit, differential, internal 2.5V reference		77		dBc
		1 MSamples/s, 12 bit, differential, V_{DD} reference		76		dBc
		1 MSamples/s, 12 bit, differential, $2xV_{DD}$ reference		75		dBc
		1 MSamples/s, 12 bit, differential, 5V reference		69		dBc
		200 kSamples/s, 12 bit, single ended, internal 1.25V reference		75		dBc
		200 kSamples/s, 12 bit, single ended, internal 2.5V reference		75		dBc

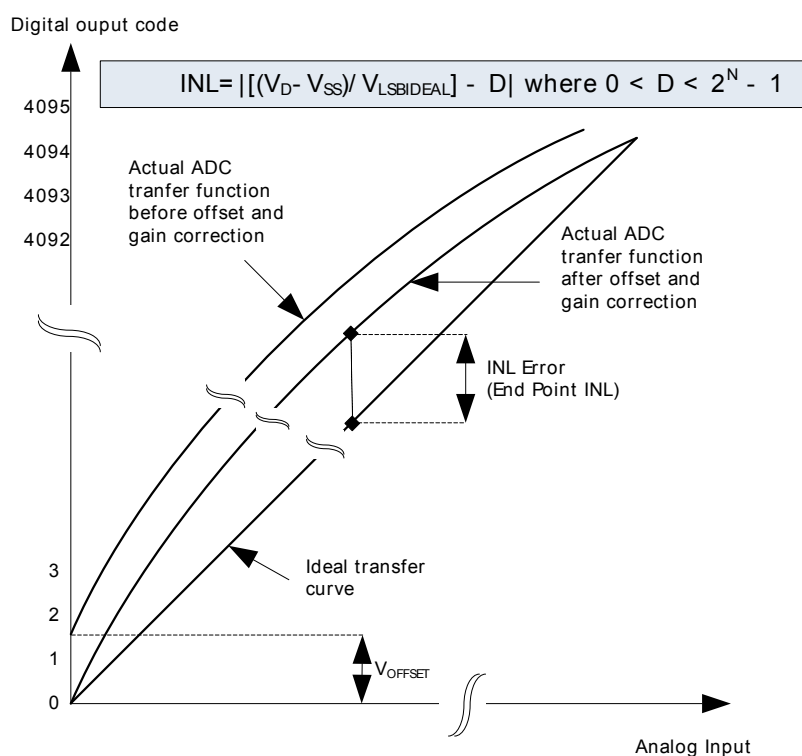
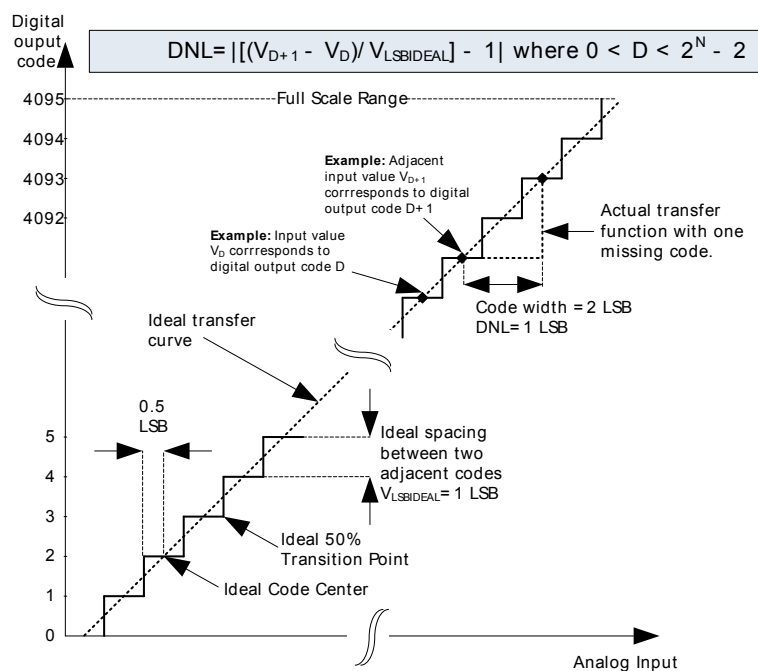
Figure 3.26. Integral Non-Linearity (INL)**Figure 3.27. Differential Non-Linearity (DNL)**

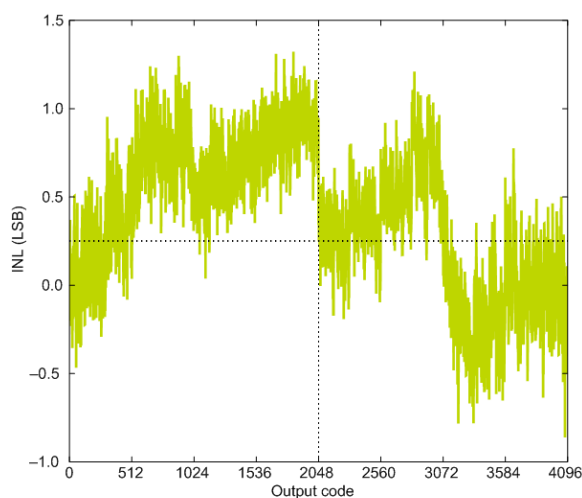
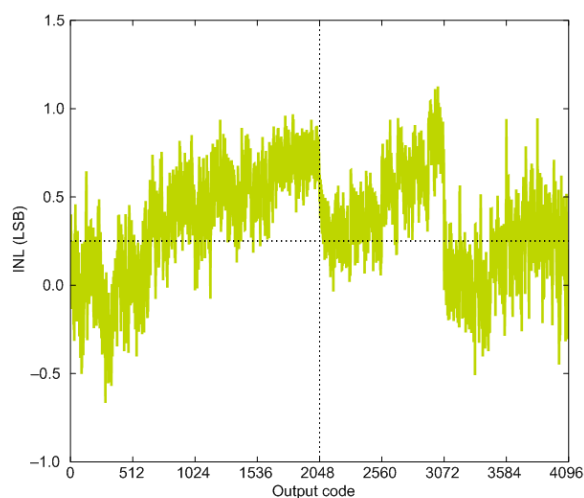
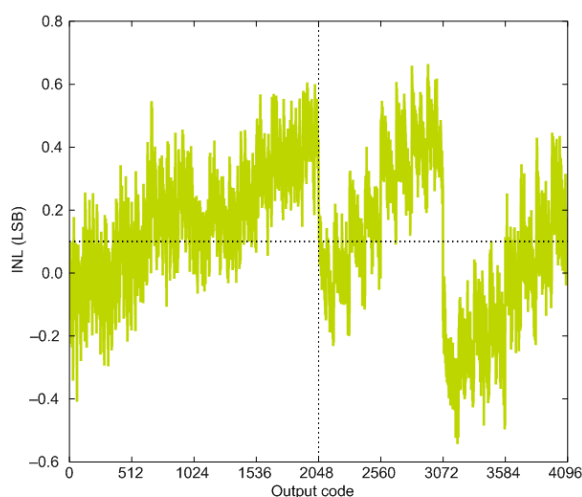
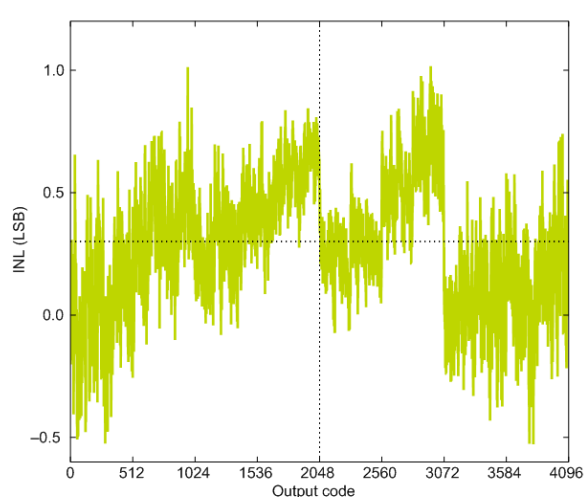
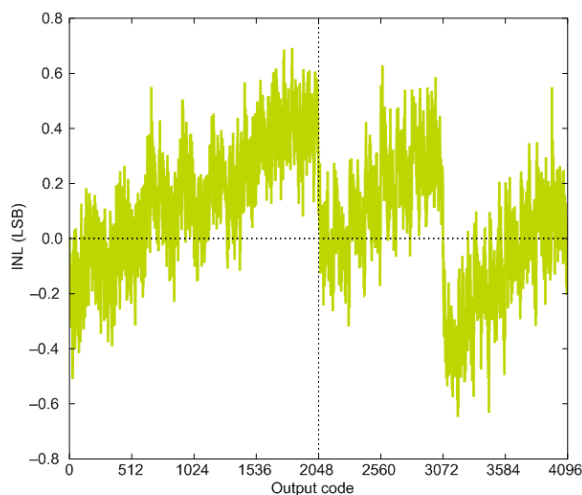
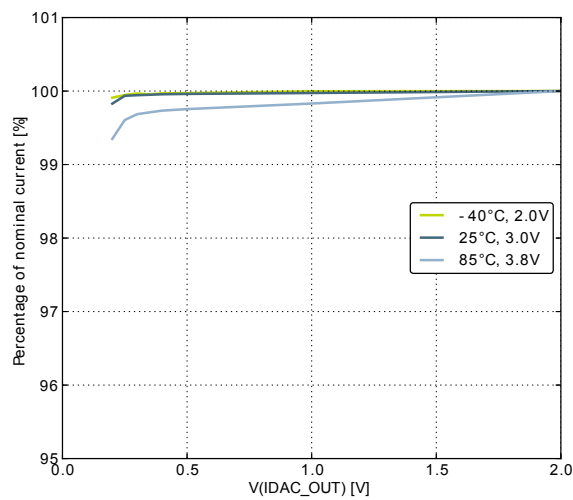
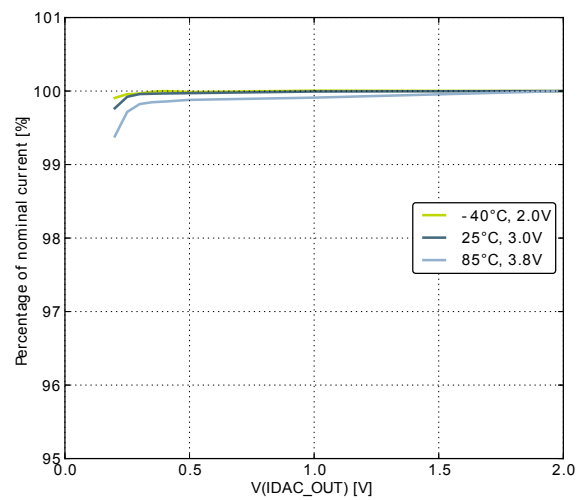
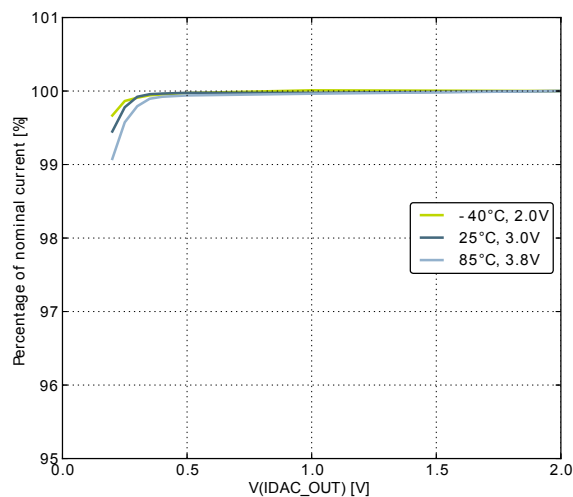
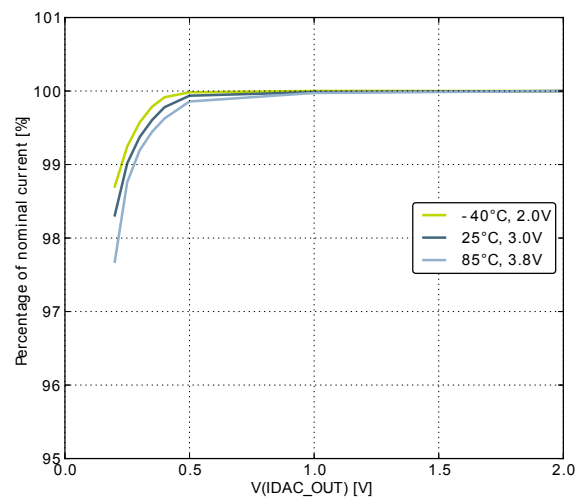
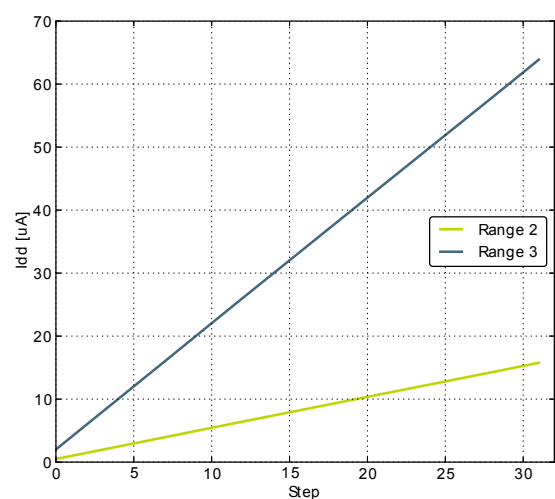
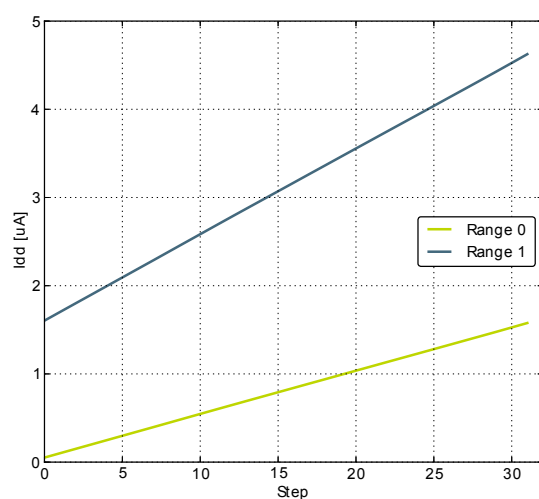
Figure 3.29. ADC Integral Linearity Error vs Code, Vdd = 3V, Temp = 25°C**1.25V Reference****2.5V Reference****2XVDDVSS Reference****5VDIFF Reference****VDD Reference**

Figure 3.35. IDAC Sink Current as a function of voltage from IDAC_OUT**Range 0****Range 1****Range 2****Range 3****Figure 3.36. IDAC linearity**

3.13 Voltage Comparator (VCMP)

Table 3.26. VCMP

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V _{VCMPIN}	Input voltage range			V _{DD}		V
V _{VCMP_{CM}}	VCMP Common Mode voltage range			V _{DD}		V
I _{VCMP}	Active current	BIASPROG=0b0000 and HALFBIAS=1 in VCMPn_CTRL register		0.2	0.8	μA
		BIASPROG=0b1111 and HALFBIAS=0 in VCMPn_CTRL register. LPREF=0.		22	35	μA
t _{VCMPREF}	Startup time reference generator	NORMAL		10		μs
V _{VCMP_{OFFSET}}	Offset voltage	Single ended		10		mV
		Differential		10		mV
V _{VCMPHYST}	VCMP hysteresis			17		mV
t _{VCMPSTART}	Startup time				10	μs

The V_{DD} trigger level can be configured by setting the TRIGLEVEL field of the VCMP_CTRL register in accordance with the following equation:

VCMP Trigger Level as a Function of Level Setting

$$V_{DD} \text{ Trigger Level} = 1.667V + 0.034 \times \text{TRIGLEVEL} \quad (3.2)$$

3.14 I2C

Table 3.27. I2C Standard-mode (Sm)

Symbol	Parameter	Min	Typ	Max	Unit
f _{SCL}	SCL clock frequency	0		100 ¹	kHz
t _{LOW}	SCL clock low time	4.7			μs
t _{HIGH}	SCL clock high time	4.0			μs
t _{SU,DAT}	SDA set-up time	250			ns
t _{HD,DAT}	SDA hold time	8		3450 ^{2,3}	ns
t _{SU,STA}	Repeated START condition set-up time	4.7			μs
t _{HD,STA}	(Repeated) START condition hold time	4.0			μs
t _{SU,STO}	STOP condition set-up time	4.0			μs
t _{BUF}	Bus free time between a STOP and START condition	4.7			μs

¹For the minimum HPPERCLK frequency required in Standard-mode, see the I2C chapter in the EFM32HG Reference Manual.

²The maximum SDA hold time (t_{HD,DAT}) needs to be met only when the device does not stretch the low time of SCL (t_{LOW}).

³When transmitting data, this number is guaranteed only when I2Cn_CLKDIV < ((3450*10⁻⁹ [s] * f_{HPPERCLK} [Hz]) - 5).

Table 3.28. I2C Fast-mode (Fm)

Symbol	Parameter	Min	Typ	Max	Unit
f _{SCL}	SCL clock frequency	0		400 ¹	kHz
t _{LOW}	SCL clock low time	1.3			μs
t _{HIGH}	SCL clock high time	0.6			μs
t _{SU,DAT}	SDA set-up time	100			ns
t _{HD,DAT}	SDA hold time	8		900 ^{2,3}	ns
t _{SU,STA}	Repeated START condition set-up time	0.6			μs
t _{HD,STA}	(Repeated) START condition hold time	0.6			μs
t _{SU,STO}	STOP condition set-up time	0.6			μs
t _{BUF}	Bus free time between a STOP and START condition	1.3			μs

¹For the minimum HFPERCLK frequency required in Fast-mode, see the I2C chapter in the EFM32HG Reference Manual.

²The maximum SDA hold time (t_{HD,DAT}) needs to be met only when the device does not stretch the low time of SCL (t_{LOW}).

³When transmitting data, this number is guaranteed only when I2Cn_CLKDIV < ((900*10⁻⁹ [s] * f_{HFPERCLK} [Hz]) - 5).

Table 3.29. I2C Fast-mode Plus (Fm+)

Symbol	Parameter	Min	Typ	Max	Unit
f _{SCL}	SCL clock frequency	0		1000 ¹	kHz
t _{LOW}	SCL clock low time	0.5			μs
t _{HIGH}	SCL clock high time	0.26			μs
t _{SU,DAT}	SDA set-up time	50			ns
t _{HD,DAT}	SDA hold time	8			ns
t _{SU,STA}	Repeated START condition set-up time	0.26			μs
t _{HD,STA}	(Repeated) START condition hold time	0.26			μs
t _{SU,STO}	STOP condition set-up time	0.26			μs
t _{BUF}	Bus free time between a STOP and START condition	0.5			μs

¹For the minimum HFPERCLK frequency required in Fast-mode Plus, see the I2C chapter in the EFM32HG Reference Manual.

3.15 Digital Peripherals

Table 3.30. Digital Peripherals

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I _{USART}	USART current	USART idle current, clock enabled		7.5		μA/ MHz
I _{I2C}	I2C current	I2C idle current, clock enabled		6.25		μA/ MHz
I _{TIMER}	TIMER current	TIMER_0 idle current, clock enabled		8.75		μA/ MHz
I _{PCNT}	PCNT current	PCNT idle current, clock enabled		100		nA
I _{RTC}	RTC current	RTC idle current, clock enabled		100		nA
I _{AES}	AES current	AES idle current, clock enabled		2.5		μA/ MHz

7 Revision History

7.1 Revision 1.00

December 4th, 2015

Updated all specs with results of full characterization.

Updated part number to revision B.

7.2 Revision 0.91

May 6th, 2015

Updated current consumption table for energy modes.

Updated GPIO max leakage current.

Updated startup time for HFXO and LFXO.

Updated current consumption for HFRCO and LFRCO.

Updated ADC current consumption.

Updated IDAC characteristics tables.

Updated ACMP internal resistance.

Updated VCMP current consumption.

7.3 Revision 0.90

March 16th, 2015

Note

This datasheet revision applies to a product under development. It's characteristics and specifications are subject to change without notice.

Corrected EM2 current consumption condition in Electrical Characteristics section.

Updated GPIO electrical characteristics.

Updated Max ESR_{HFXO} value for Crystal Frequency of 25 MHz.

Updated LFRCO plots.

Updated HFRCO table and plots.

Updated ADC table and temp sensor plot.

Added DMA current in Digital Peripherals section.

Updated block diagram.

Updated Package dimensions table.

Corrected leadframe type to matte-Sn.

A Disclaimer and Trademarks

A.1 Disclaimer

Silicon Laboratories intends to provide customers with the latest, accurate, and in-depth documentation of all peripherals and modules available for system and software implementers using or intending to use the Silicon Laboratories products. Characterization data, available modules and peripherals, memory sizes and memory addresses refer to each specific device, and "Typical" parameters provided can and do vary in different applications. Application examples described herein are for illustrative purposes only. Silicon Laboratories reserves the right to make changes without further notice and limitation to product information, specifications, and descriptions herein, and does not give warranties as to the accuracy or completeness of the included information. Silicon Laboratories shall have no liability for the consequences of use of the information supplied herein. This document does not imply or express copyright licenses granted hereunder to design or fabricate any integrated circuits. The products must not be used within any Life Support System without the specific written consent of Silicon Laboratories. A "Life Support System" is any product or system intended to support or sustain life and/or health, which, if it fails, can be reasonably expected to result in significant personal injury or death. Silicon Laboratories products are generally not intended for military applications. Silicon Laboratories products shall under no circumstances be used in weapons of mass destruction including (but not limited to) nuclear, biological or chemical weapons, or missiles capable of delivering such weapons.

A.2 Trademark Information

Silicon Laboratories Inc., Silicon Laboratories, Silicon Labs, SiLabs and the Silicon Labs logo, CMEMS[®], EFM, EFM32, EFR, Energy Micro, Energy Micro logo and combinations thereof, "the world's most energy friendly microcontrollers", Ember[®], EZLink[®], EZMac[®], EZRadio[®], EZRadioPRO[®], DSPLL[®], ISO-modem[®], Precision32[®], ProSLIC[®], SiPHY[®], USBXpress[®] and others are trademarks or registered trademarks of Silicon Laboratories Inc. ARM, CORTEX, Cortex-M3 and THUMB are trademarks or registered trademarks of ARM Holdings. Keil is a registered trademark of ARM Limited. All other products or brand names mentioned herein are trademarks of their respective holders.

Table of Contents

1. Ordering Information	2
2. System Summary	3
2.1. System Introduction	3
2.2. Configuration Summary	6
2.3. Memory Map	7
3. Electrical Characteristics	8
3.1. Test Conditions	8
3.2. Absolute Maximum Ratings	8
3.3. General Operating Conditions	8
3.4. Current Consumption	9
3.5. Transition between Energy Modes	17
3.6. Power Management	17
3.7. Flash	18
3.8. General Purpose Input Output	18
3.9. Oscillators	27
3.10. Analog Digital Converter (ADC)	32
3.11. Current Digital Analog Converter (IDAC)	42
3.12. Analog Comparator (ACMP)	47
3.13. Voltage Comparator (VCMP)	49
3.14. I2C	49
3.15. Digital Peripherals	50
4. Pinout and Package	52
4.1. Pinout	52
4.2. Alternate Functionality Pinout	54
4.3. GPIO Pinout Overview	56
4.4. QFN32 Package	56
5. PCB Layout and Soldering	58
5.1. Recommended PCB Layout	58
5.2. Soldering Information	60
6. Chip Marking, Revision and Errata	61
6.1. Chip Marking	61
6.2. Revision	61
6.3. Errata	61
7. Revision History	62
7.1. Revision 1.00	62
7.2. Revision 0.91	62
7.3. Revision 0.90	62
7.4. Revision 0.20	63
A. Disclaimer and Trademarks	64
A.1. Disclaimer	64
A.2. Trademark Information	64
B. Contact Information	65
B.1.	65

List of Figures

2.1. Block Diagram	3
2.2. EFM32HG210 Memory Map with largest RAM and Flash sizes	7
3.1. EM0 Current consumption while executing prime number calculation code from flash with HFRCO running at 24 MHz	11
3.2. EM0 Current consumption while executing prime number calculation code from flash with HFRCO running at 21 MHz	11
3.3. EM0 Current consumption while executing prime number calculation code from flash with HFRCO running at 14 MHz	12
3.4. EM0 Current consumption while executing prime number calculation code from flash with HFRCO running at 11 MHz	12
3.5. EM0 Current consumption while executing prime number calculation code from flash with HFRCO running at 6.6 MHz	13
3.6. EM1 Current consumption with all peripheral clocks disabled and HFRCO running at 24 MHz	13
3.7. EM1 Current consumption with all peripheral clocks disabled and HFRCO running at 21 MHz	14
3.8. EM1 Current consumption with all peripheral clocks disabled and HFRCO running at 14 MHz	14
3.9. EM1 Current consumption with all peripheral clocks disabled and HFRCO running at 11 MHz	15
3.10. EM1 Current consumption with all peripheral clocks disabled and HFRCO running at 6.6 MHz	15
3.11. EM2 current consumption. RTC prescaled to 1kHz, 32.768 kHz LFRCO.	16
3.12. EM3 current consumption.	16
3.13. EM4 current consumption.	17
3.14. Typical Low-Level Output Current, 2V Supply Voltage	21
3.15. Typical High-Level Output Current, 2V Supply Voltage	22
3.16. Typical Low-Level Output Current, 3V Supply Voltage	23
3.17. Typical High-Level Output Current, 3V Supply Voltage	24
3.18. Typical Low-Level Output Current, 3.8V Supply Voltage	25
3.19. Typical High-Level Output Current, 3.8V Supply Voltage	26
3.20. Calibrated LFRCO Frequency vs Temperature and Supply Voltage	28
3.21. Calibrated HFRCO 1 MHz Band Frequency vs Supply Voltage and Temperature	29
3.22. Calibrated HFRCO 7 MHz Band Frequency vs Supply Voltage and Temperature	30
3.23. Calibrated HFRCO 11 MHz Band Frequency vs Supply Voltage and Temperature	30
3.24. Calibrated HFRCO 14 MHz Band Frequency vs Supply Voltage and Temperature	30
3.25. Calibrated HFRCO 21 MHz Band Frequency vs Supply Voltage and Temperature	31
3.26. Integral Non-Linearity (INL)	37
3.27. Differential Non-Linearity (DNL)	37
3.28. ADC Frequency Spectrum, Vdd = 3V, Temp = 25°C	38
3.29. ADC Integral Linearity Error vs Code, Vdd = 3V, Temp = 25°C	39
3.30. ADC Differential Linearity Error vs Code, Vdd = 3V, Temp = 25°C	40
3.31. ADC Absolute Offset, Common Mode = Vdd /2	41
3.32. ADC Dynamic Performance vs Temperature for all ADC References, Vdd = 3V	41
3.33. ADC Temperature sensor readout	42
3.34. IDAC Source Current as a function of voltage on IDAC_OUT	45
3.35. IDAC Sink Current as a function of voltage from IDAC_OUT	46
3.36. IDAC linearity	46
3.37. ACMP Characteristics, Vdd = 3V, Temp = 25°C, FULLBIAS = 0, HALFBIAS = 1	48
4.1. EFM32HG210 Pinout (top view, not to scale)	52
4.2. QFN32	56
5.1. QFN32 PCB Land Pattern	58
5.2. QFN32 PCB Solder Mask	59
5.3. QFN32 PCB Stencil Design	60
6.1. Example Chip Marking (top view)	61

silabs.com

