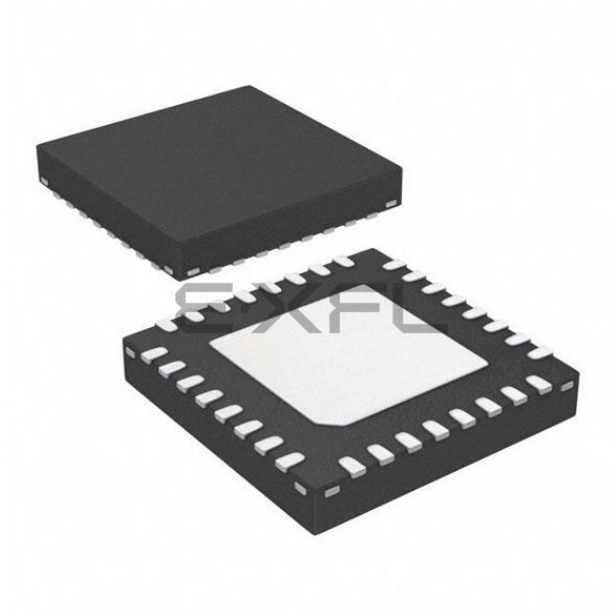

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	25MHz
Connectivity	I²C, IrDA, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	24
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.98V ~ 3.8V
Data Converters	A/D 4x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-VQFN Exposed Pad
Supplier Device Package	32-QFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32hg210f32g-b-qfn32

1 Ordering Information

Table 1.1 (p. 2) shows the available EFM32HG210 devices.

Table 1.1. Ordering Information

Ordering Code	Flash (kB)	RAM (kB)	Max Speed (MHz)	Supply Voltage (V)	Temperature (ºC)	Package
EFM32HG210F32G-B-QFN32	32	4	25	1.98 - 3.8	-40 - 85	QFN32
EFM32HG210F64G-B-QFN32	64	8	25	1.98 - 3.8	-40 - 85	QFN32

Adding the suffix 'R' to the part number (e.g. EFM32HG210F32G-B-QFN32R) denotes tape and reel.

Visit **www.silabs.com** for information on global distributors and representatives.

2.1.12 Pre-Programmed UART Bootloader

The bootloader presented in application note AN0003 is pre-programmed in the device at factory. Auto-baud and destructive write are supported. The autobaud feature, interface and commands are described further in the application note.

2.1.13 Low Energy Universal Asynchronous Receiver/Transmitter (LEUART)

The unique LEUART™, the Low Energy UART, is a UART that allows two-way UART communication on a strict power budget. Only a 32.768 kHz clock is needed to allow UART communication up to 9600 baud/s. The LEUART includes all necessary hardware support to make asynchronous serial communication possible with minimum of software intervention and energy consumption.

2.1.14 Timer/Counter (TIMER)

The 16-bit general purpose Timer has 3 compare/capture channels for input capture and compare/Pulse-Width Modulation (PWM) output. TIMER0 also includes a Dead-Time Insertion module suitable for motor control applications.

2.1.15 Real Time Counter (RTC)

The Real Time Counter (RTC) contains a 24-bit counter and is clocked either by a 32.768 kHz crystal oscillator, or a 32.768 kHz RC oscillator. In addition to energy modes EM0 and EM1, the RTC is also available in EM2. This makes it ideal for keeping track of time since the RTC is enabled in EM2 where most of the device is powered down.

2.1.16 Pulse Counter (PCNT)

The Pulse Counter (PCNT) can be used for counting pulses on a single input or to decode quadrature encoded inputs. It runs off either the internal LFACLK or the PCNTn_S0IN pin as external clock source. The module may operate in energy mode EM0 - EM3.

2.1.17 Analog Comparator (ACMP)

The Analog Comparator is used to compare the voltage of two analog inputs, with a digital output indicating which input voltage is higher. Inputs can either be one of the selectable internal references or from external pins. Response time and thereby also the current consumption can be configured by altering the current supply to the comparator.

2.1.18 Voltage Comparator (VCMP)

The Voltage Supply Comparator is used to monitor the supply voltage from software. An interrupt can be generated when the supply falls below or rises above a programmable threshold. Response time and thereby also the current consumption can be configured by altering the current supply to the comparator.

2.1.19 Analog to Digital Converter (ADC)

The ADC is a Successive Approximation Register (SAR) architecture, with a resolution of up to 12 bits at up to one million samples per second. The integrated input mux can select inputs from 4 external pins and 6 internal signals.

2.1.20 Current Digital to Analog Converter (IDAC)

The current digital to analog converter can source or sink a configurable constant current, which can be output on, or sinked from pin or ADC. The current is configurable with several ranges of various step sizes.

2.1.21 Advanced Encryption Standard Accelerator (AES)

The AES accelerator performs AES encryption and decryption with 128-bit. Encrypting or decrypting one 128-bit data block takes 52 HFCORECLK cycles with 128-bit keys. The AES module is an AHB slave which enables efficient access to the data and key registers. All write accesses to the AES module must be 32-bit operations, i.e. 8- or 16-bit operations are not supported.

2.1.22 General Purpose Input/Output (GPIO)

In the EFM32HG210, there are 24 General Purpose Input/Output (GPIO) pins, which are divided into ports with up to 16 pins each. These pins can individually be configured as either an output or input. More advanced configurations like open-drain, filtering and drive strength can also be configured individually for the pins. The GPIO pins can also be overridden by peripheral pin connections, like Timer PWM outputs or USART communication, which can be routed to several locations on the device. The GPIO supports up to 14 asynchronous external pin interrupts, which enables interrupts from any pin on the device. Also, the input value of a pin can be routed through the Peripheral Reflex System to other peripherals.

2.2 Configuration Summary

The features of the EFM32HG210 is a subset of the feature set described in the EFM32HG Reference Manual. Table 2.1 (p. 6) describes device specific implementation of the features.

Table 2.1. Configuration Summary

Module	Configuration	Pin Connections
Cortex-M0+	Full configuration	NA
DBG	Full configuration	DBG_SWCLK, DBG_SWDIO,
MSC	Full configuration	NA
DMA	Full configuration	NA
RMU	Full configuration	NA
EMU	Full configuration	NA
CMU	Full configuration	CMU_OUT0, CMU_OUT1
WDOG	Full configuration	NA
PRS	Full configuration	NA
I2C0	Full configuration	I2C0_SDA, I2C0_SCL
USART0	Full configuration with IrDA and I2S	US0_TX, US0_RX. US0_CLK, US0_CS
USART1	Full configuration with I2S and IrDA	US1_TX, US1_RX, US1_CLK, US1_CS
LEUART0	Full configuration	LEU0_TX, LEU0_RX
TIMER0	Full configuration with DTI	TIM0_CC[2:0], TIM0_CDTI[2:0]
TIMER1	Full configuration	TIM1_CC[2:0]
TIMER2	Full configuration	TIM2_CC[2:0]
RTC	Full configuration	NA
PCNT0	Full configuration, 16-bit count register	PCNT0_S[1:0]
ACMP0	Full configuration	ACMP0_CH[1:0], ACMP0_O
VCMP	Full configuration	NA
ADC0	Full configuration	ADC0_CH[7:4]

3 Electrical Characteristics

3.1 Test Conditions

3.1.1 Typical Values

The typical data are based on T_{AMB}=25°C and V_{DD}=3.0 V, as defined in Table 3.2 (p. 8), unless otherwise specified.

3.1.2 Minimum and Maximum Values

The minimum and maximum values represent the worst conditions of ambient temperature, supply voltage and frequencies, as defined in Table 3.2 (p. 8) , unless otherwise specified.

3.2 Absolute Maximum Ratings

The absolute maximum ratings are stress ratings, and functional operation under such conditions are not guaranteed. Stress beyond the limits specified in Table 3.1 (p. 8) may affect the device reliability or cause permanent damage to the device. Functional operating conditions are given in Table 3.2 (p. 8) .

Table 3.1. Absolute Maximum Ratings

Symbol	Parameter	Condition	Min	Typ	Max	Unit
T_{STG}	Storage temperature range		-40		150[1]	°C
T_S	Maximum soldering temperature	Latest IPC/JEDEC J-STD-020 Standard			260	°C
V_{DDMAX}	External main supply voltage		0		3.8	V
V_{IOPIN}	Voltage on any I/O pin		-0.3		V_{DD}+0.3	V

[1]Based on programmed devices tested for 10000 hours at 150ºC. Storage temperature affects retention of preprogrammed calibration values stored in flash. Please refer to the Flash section in the Electrical Characteristics for information on flash data retention for different temperatures.

3.3 General Operating Conditions

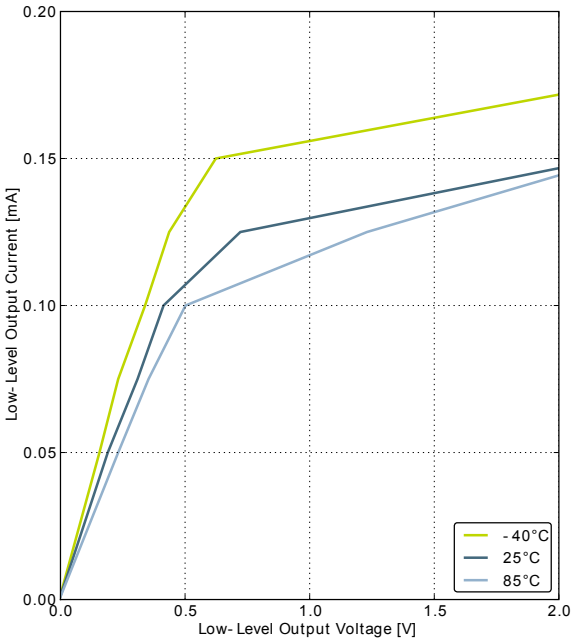
3.3.1 General Operating Conditions

Table 3.2. General Operating Conditions

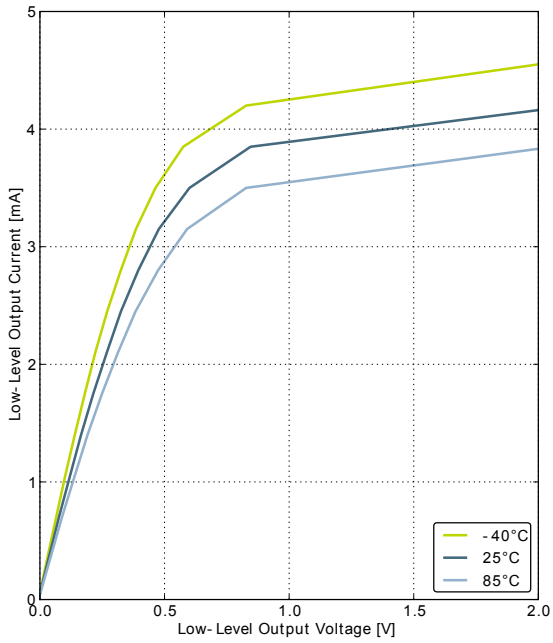
Symbol	Parameter	Min	Typ	Max	Unit
T_{AMB}	Ambient temperature range	-40		85	°C
V_{DDOP}	Operating supply voltage	1.98		3.8	V
f_{APB}	Internal APB clock frequency			25	MHz
f_{AHB}	Internal AHB clock frequency			25	MHz

Symbol	Parameter	Condition	Min	Typ	Max	Unit
	by the glitch suppression filter					
t_{IOOF}	Output fall time	GPIO_Px_CTRL DRIVEMODE = LOWEST and load capacitance C_L=12.5-25pF.	20+0.1C_L		250	ns
		GPIO_Px_CTRL DRIVEMODE = LOW and load capacitance C_L=350-600pF	20+0.1C_L		250	ns
V_{IOHYST}	I/O pin hysteresis (V_{IOTHR+} - V_{IOTHR-})	V_{DD} = 1.98 - 3.8 V	0.1V_{DD}			V

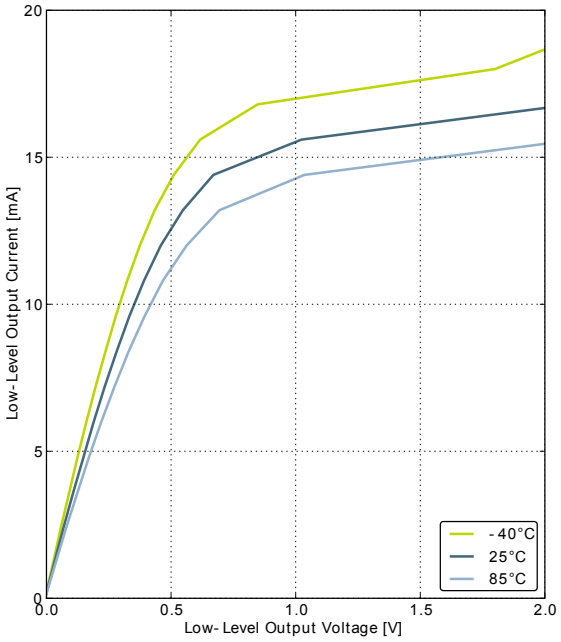
Figure 3.14. Typical Low-Level Output Current, 2V Supply Voltage



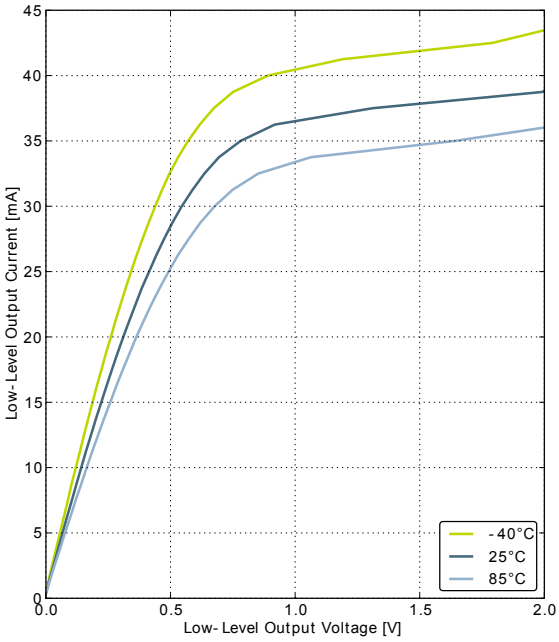
GPIO_Px_CTRL DRIVEMODE = LOWEST



GPIO_Px_CTRL DRIVEMODE = LOW

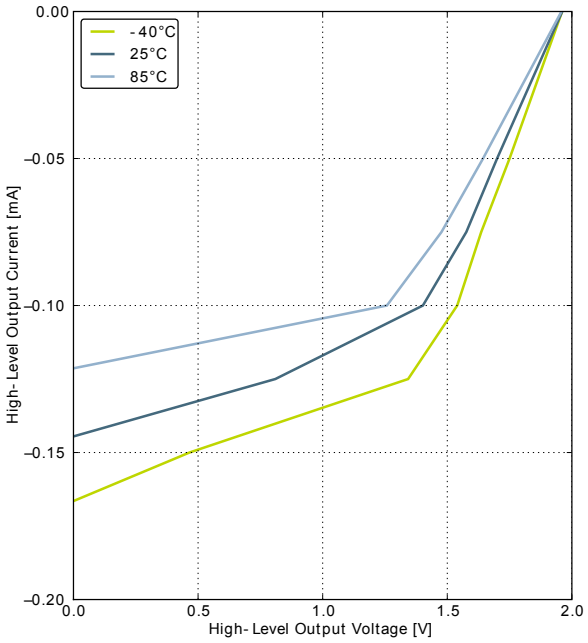


GPIO_Px_CTRL DRIVEMODE = STANDARD

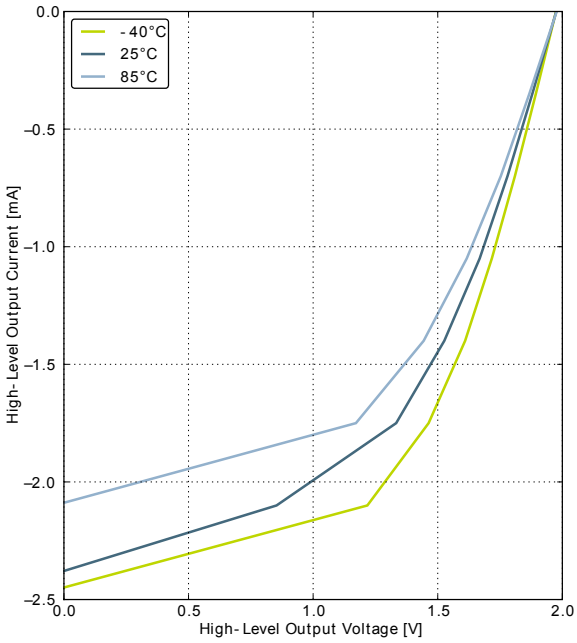


GPIO_Px_CTRL DRIVEMODE = HIGH

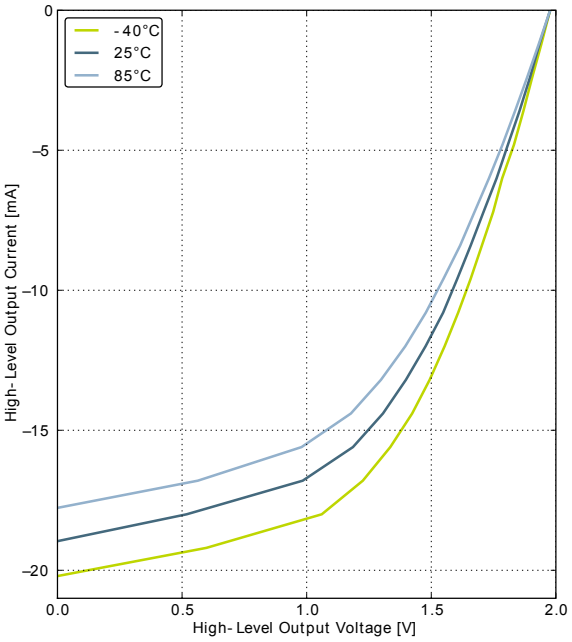
Figure 3.15. Typical High-Level Output Current, 2V Supply Voltage



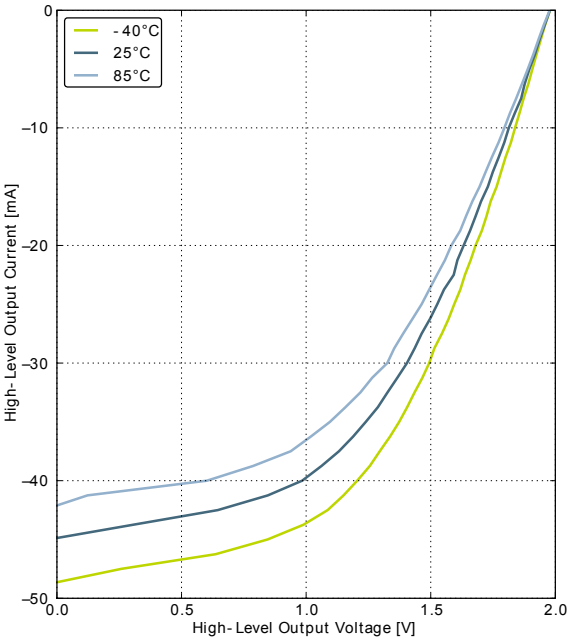
GPIO_Px_CTRL DRIVEMODE = LOWEST



GPIO_Px_CTRL DRIVEMODE = LOW

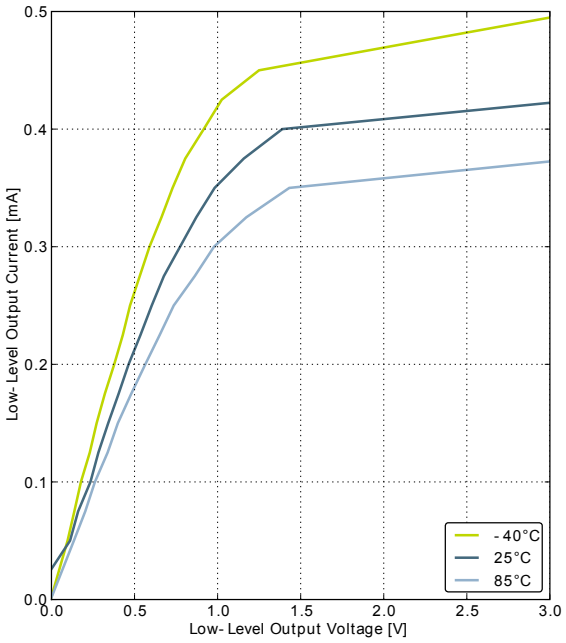


GPIO_Px_CTRL DRIVEMODE = STANDARD

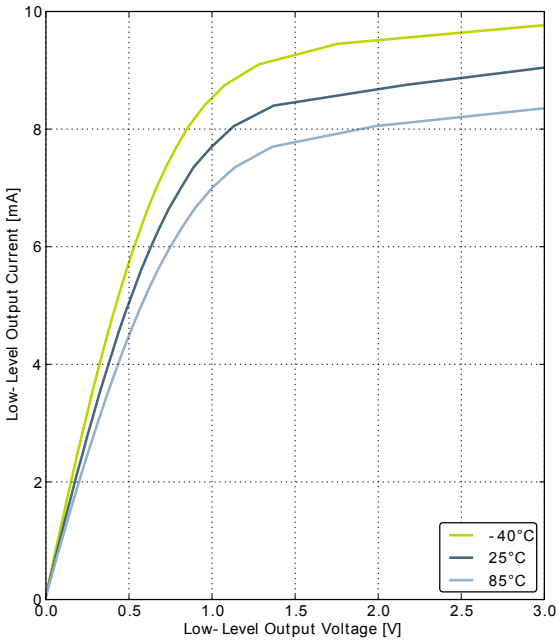


GPIO_Px_CTRL DRIVEMODE = HIGH

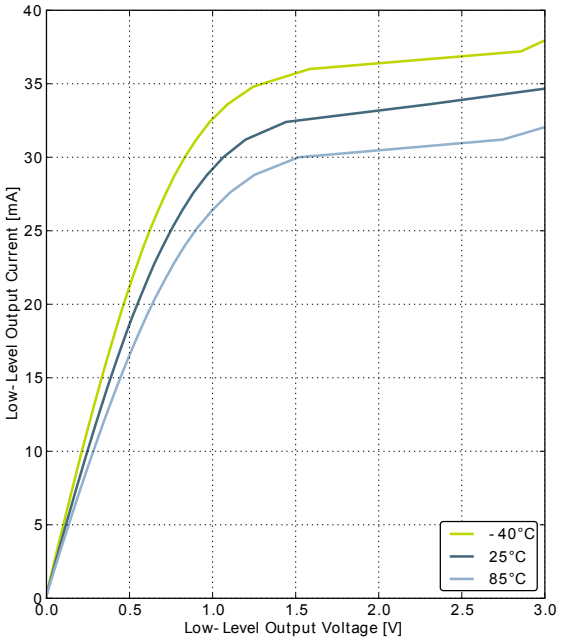
Figure 3.16. Typical Low-Level Output Current, 3V Supply Voltage



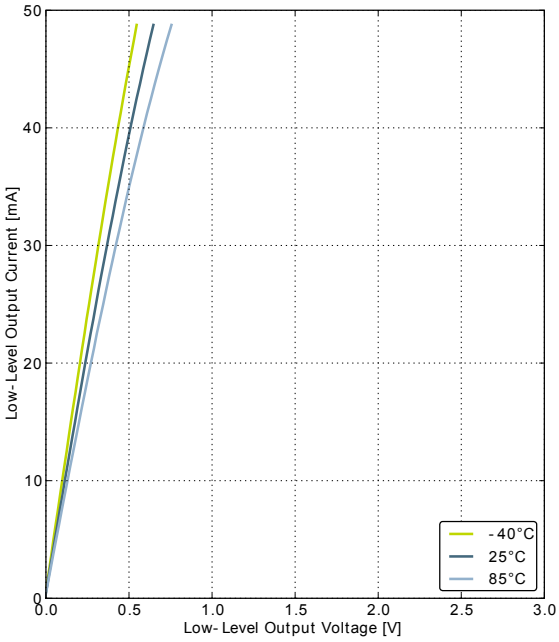
GPIO_Px_CTRL DRIVEMODE = LOWEST



GPIO_Px_CTRL DRIVEMODE = LOW



GPIO_Px_CTRL DRIVEMODE = STANDARD



GPIO_Px_CTRL DRIVEMODE = HIGH

3.9 Oscillators

3.9.1 LFXO

Table 3.8. LFXO

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{LFXO}	Supported nominal crystal frequency			32.768		kHz
ESR_{LFXO}	Supported crystal equivalent series resistance (ESR)			30	120	kOhm
C_{LFXOL}	Supported crystal external load range		5		25	pF
I_{LFXO}	Current consumption for core and buffer after startup.	ESR=30 kOhm, C_L=10 pF, LFXOBOOST in CMU_CTRL is 1		190		nA
t_{LFXO}	Start- up time.	ESR=30 kOhm, C_L=10 pF, 40% - 60% duty cycle has been reached, LFXOBOOST in CMU_CTRL is 1		1100		ms

For safe startup of a given crystal, the Configurator tool in Simplicity Studio contains a tool to help users configure both load capacitance and software settings for using the LFXO. For details regarding the crystal configuration, the reader is referred to application note "AN0016 EFM32 Oscillator Design Consideration".

3.9.2 HFXO

Table 3.9. HFXO

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{HFXO}	Supported frequency, any mode		4		25	MHz
ESR_{HFXO}	Supported crystal equivalent series resistance (ESR)	Crystal frequency 25 MHz		30	100	Ohm
		Crystal frequency 4 MHz		400	1500	Ohm
g_{mHFXO}	The transconductance of the HFXO input transistor at crystal startup	HFXOBOOST in CMU_CTRL equals 0b11	20			mS
C_{HFXOL}	Supported crystal external load range		5		25	pF
I_{HFXO}	Current consumption for HFXO after startup	4 MHz: ESR=400 Ohm, C_L=20 pF, HFXOBOOST in CMU_CTRL equals 0b11		85		µA
		25 MHz: ESR=30 Ohm, C_L=10 pF, HFXOBOOST in CMU_CTRL equals 0b11		165		µA
t_{HFXO}	Startup time	25 MHz: ESR=30 Ohm, C_L=10 pF, HFXOBOOST in CMU_CTRL equals 0b11		785		µs

Figure 3.22. Calibrated HFRCO 7 MHz Band Frequency vs Supply Voltage and Temperature

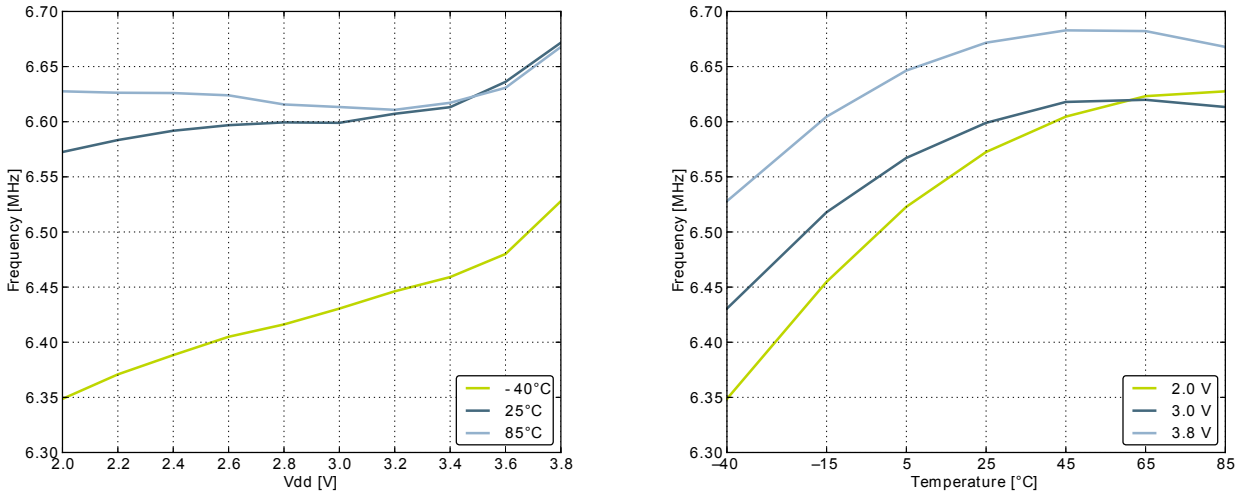


Figure 3.23. Calibrated HFRCO 11 MHz Band Frequency vs Supply Voltage and Temperature

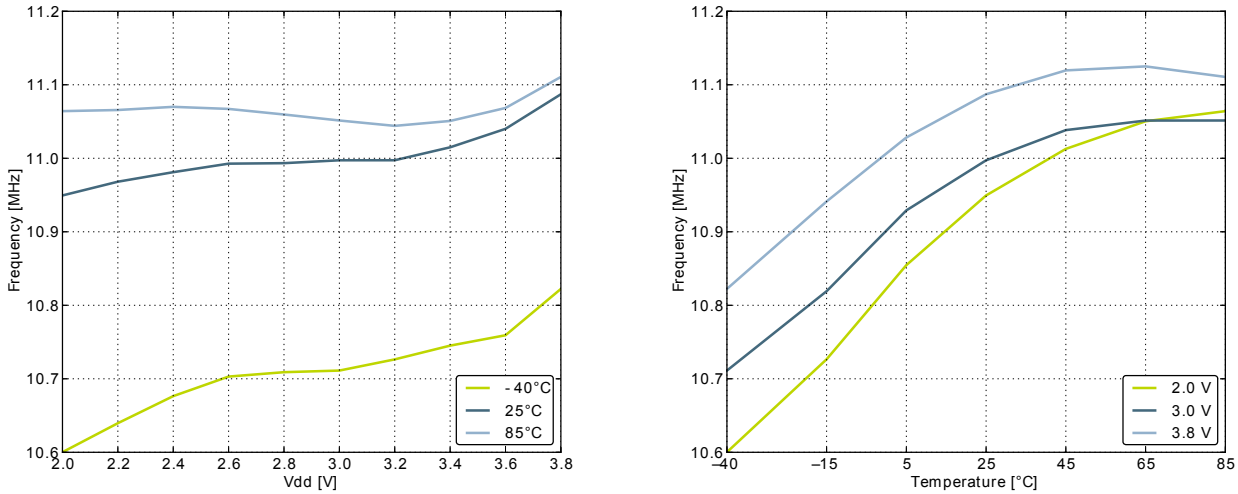
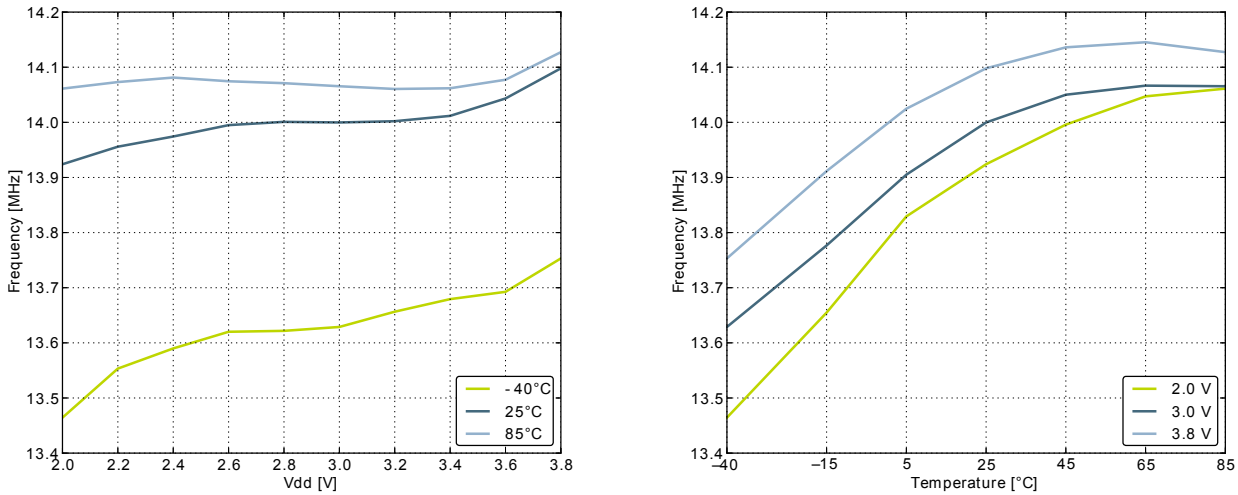


Figure 3.24. Calibrated HFRCO 14 MHz Band Frequency vs Supply Voltage and Temperature



Symbol	Parameter	Condition	Min	Typ	Max	Unit
$V_{ADCCMIN}$	Common mode input range		0		V_{DD}	V
I_{ADCIN}	Input current	2pF sampling capacitors		<100		nA
$CMRR_{ADC}$	Analog input common mode rejection ratio			65		dB
I_{ADC}	Average active current	1 MSamples/s, 12 bit, external reference		392	510	µA
		10 kSamples/s 12 bit, internal 1.25 V reference, WARMUPMODE in ADCn_CTRL set to 0b00		67		µA
		10 kSamples/s 12 bit, internal 1.25 V reference, WARMUPMODE in ADCn_CTRL set to 0b01		63		µA
		10 kSamples/s 12 bit, internal 1.25 V reference, WARMUPMODE in ADCn_CTRL set to 0b10		64		µA
		10 kSamples/s 12 bit, internal 1.25 V reference, WARMUPMODE in ADCn_CTRL set to 0b11		244		µA
I_{ADCREF}	Current consumption of internal voltage reference	Internal voltage reference		65		µA
C_{ADCIN}	Input capacitance			2		pF
R_{ADCIN}	Input ON resistance		1			MOhm
$R_{ADCFILT}$	Input RC filter resistance			10		kOhm
$C_{ADCFILT}$	Input RC filter/decoupling capacitance			250		fF
f_{ADCCLK}	ADC Clock Frequency				13	MHz
$t_{ADCCONV}$	Conversion time	6 bit	7			ADCCLK Cycles
		8 bit	11			ADCCLK Cycles
		12 bit	13			ADCCLK Cycles
t_{ADCACQ}	Acquisition time	Programmable	1		256	ADCCLK Cycles
$t_{ADCACQVDD3}$	Required acquisition time for VDD/3 reference		2			µs

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{0x10}	Nominal IDAC output current with STEPSEL=0x10			8.5		µA
I_{STEP}	Step size			0.5		µA
I_D	Current drop at high impedance load	V_{IDAC_OUT} = 200 mV		0.62		%
TC_{IDAC}	Temperature coefficient	V_{DD} = 3.0 V, STEPSEL=0x10		2.8		nA/°C
VC_{IDAC}	Voltage coefficient	T = 25 °C, STEPSEL=0x10		94.4		nA/V

Table 3.22. IDAC Range 3 Source

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{IDAC}	Active current with STEPSEL=0x10	EM0, default settings		18.7		µA
		Duty-cycled		10		nA
I_{0x10}	Nominal IDAC output current with STEPSEL=0x10			33.9		µA
I_{STEP}	Step size			2.0		µA
I_D	Current drop at high impedance load	V_{IDAC_OUT} = V_{DD} - 100 mV		3.54		%
TC_{IDAC}	Temperature coefficient	V_{DD} = 3.0 V, STEPSEL=0x10		10.9		nA/°C
VC_{IDAC}	Voltage coefficient	T = 25 °C, STEPSEL=0x10		159.5		nA/V

Table 3.23. IDAC Range 3 Sink

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{IDAC}	Active current with STEPSEL=0x10	EM0, default settings		62.5		µA
I_{0x10}	Nominal IDAC output current with STEPSEL=0x10			34.1		µA
I_{STEP}	Step size			2.0		µA
I_D	Current drop at high impedance load	V_{IDAC_OUT} = 200 mV		1.75		%
TC_{IDAC}	Temperature coefficient	V_{DD} = 3.0 V, STEPSEL=0x10		10.9		nA/°C
VC_{IDAC}	Voltage coefficient	T = 25 °C, STEPSEL=0x10		148.6		nA/V

Table 3.24. IDAC

Symbol	Parameter	Min	Typ	Max	Unit
$t_{IDACSTART}$	Start-up time, from enabled to output settled		40		µs

3.13 Voltage Comparator (VCMP)

Table 3.26. VCMP

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{VCMPIN}	Input voltage range			V_{DD}		V
V_{VCMPCM}	VCMP Common Mode voltage range			V_{DD}		V
I_{VCMP}	Active current	BIASPROG=0b0000 and HALFBIAS=1 in VCMPn_CTRL register		0.2	0.8	µA
		BIASPROG=0b1111 and HALFBIAS=0 in VCMPn_CTRL register. LPREF=0.		22	35	µA
$t_{VCMPREF}$	Startup time reference generator	NORMAL		10		µs
$V_{VCMPOFFSET}$	Offset voltage	Single ended		10		mV
		Differential		10		mV
$V_{VCMPHYST}$	VCMP hysteresis			17		mV
$t_{VCMPSTART}$	Startup time				10	µs

The V_{DD} trigger level can be configured by setting the TRIGLEVEL field of the VCMP_CTRL register in accordance with the following equation:

VCMP Trigger Level as a Function of Level Setting

$$V_{DD\ Trigger\ Level}=1.667V+0.034 \times TRIGLEVEL \quad (3.2)$$

3.14 I2C

Table 3.27. I2C Standard-mode (Sm)

Symbol	Parameter	Min	Typ	Max	Unit
f_{SCL}	SCL clock frequency	0		100[1]	kHz
t_{LOW}	SCL clock low time	4.7			µs
t_{HIGH}	SCL clock high time	4.0			µs
$t_{SU,DAT}$	SDA set-up time	250			ns
$t_{HD,DAT}$	SDA hold time	8		3450[2,3]	ns
$t_{SU,STA}$	Repeated START condition set-up time	4.7			µs
$t_{HD,STA}$	(Repeated) START condition hold time	4.0			µs
$t_{SU,STO}$	STOP condition set-up time	4.0			µs
t_{BUF}	Bus free time between a STOP and START condition	4.7			µs

[1]For the minimum HFPERCLK frequency required in Standard-mode, see the I2C chapter in the EFM32HG Reference Manual.
[2]The maximum SDA hold time ($t_{HD,DAT}$) needs to be met only when the device does not stretch the low time of SCL (t_{LOW}).
[3]When transmitting data, this number is guaranteed only when I2Cn_CLKDIV < ((3450*10^{-9} [s] * $f_{HFPERCLK}$ [Hz]) - 5).

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{GPIO}	GPIO current	GPIO idle current, clock enabled		5.31		µA/MHz
I_{PRS}	PRS current	PRS idle current		2.81		µA/MHz
I_{DMA}	DMA current	Clock enable		8.12		µA/MHz

4 Pinout and Package

Note

Please refer to the application note "AN0002 EFM32 Hardware Design Considerations" for guidelines on designing Printed Circuit Boards (PCB's) for the EFM32HG210.

4.1 Pinout

The *EFM32HG210* pinout is shown in Figure 4.1 (p. 52) and Table 4.1 (p. 52). Alternate locations are denoted by "#" followed by the location number (Multiple locations on the same pin are split with "/"). Alternate locations can be configured in the LOCATION bitfield in the *_ROUTE register in the module in question.

Figure 4.1. EFM32HG210 Pinout (top view, not to scale)

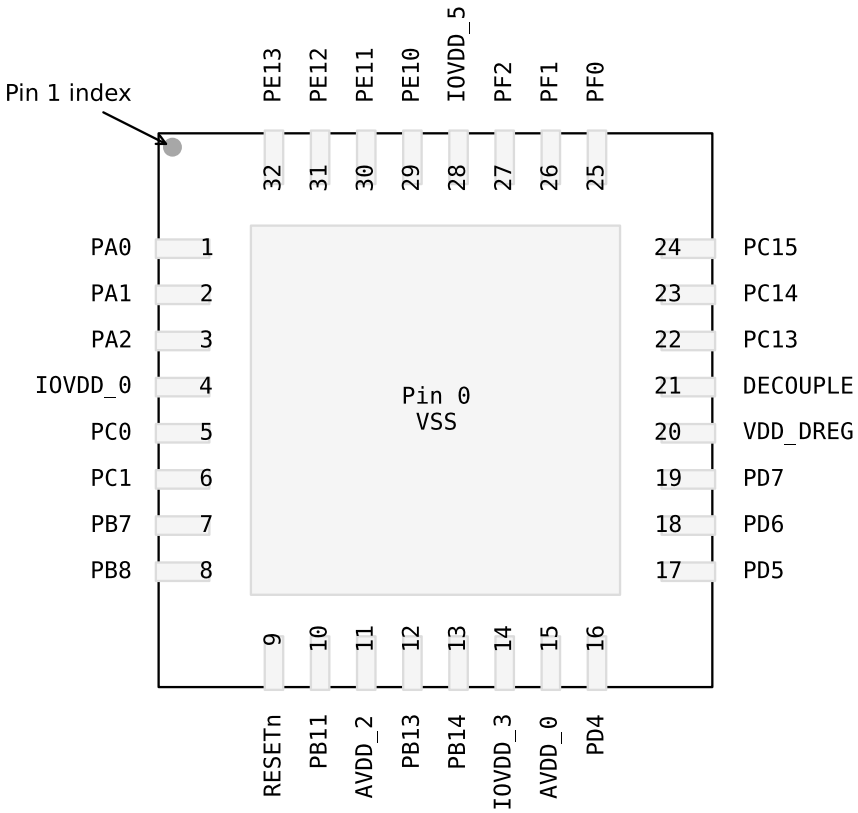


Table 4.1. Device Pinout

QFN32 Pin# and Name		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
0	VSS	Ground.			
1	PA0		TIM0_CC1 #6 TIM0_CC0 #0/1/4 PCNT0_S0IN #4	US1_RX #4 LEU0_RX #4 I2C0_SDA #0	PRS_CH0 #0 PRS_CH3 #3 GPIO_EM4WU0
2	PA1		TIM0_CC0 #6	I2C0_SCL #0	CMU_CLK1 #0

Alternate	LOCATION							
Functionality	0	1	2	3	4	5	6	Description
GPIO_EM4WU4	PF2							Pin can be used to wake the system up from EM4
GPIO_EM4WU5	PE13							Pin can be used to wake the system up from EM4
HFXTAL_N	PB14							High Frequency Crystal negative pin. Also used as external optional clock input pin.
HFXTAL_P	PB13							High Frequency Crystal positive pin.
I2C0_SCL	PA1	PD7			PC1	PF1	PE13	I2C0 Serial Clock Line input / output.
I2C0_SDA	PA0	PD6			PC0	PF0	PE12	I2C0 Serial Data input / output.
IDAC0_OUT	PB11							IDAC0 output.
LEU0_RX	PD5	PB14		PF1	PA0	PC15		LEUART0 Receive input.
LEU0_TX	PD4	PB13		PF0	PF2	PC14		LEUART0 Transmit output. Also used as receive input in half duplex communication.
LFXTAL_N	PB8							Low Frequency Crystal (typically 32.768 kHz) negative pin. Also used as an optional external clock input pin.
LFXTAL_P	PB7							Low Frequency Crystal (typically 32.768 kHz) positive pin.
PCNT0_S0IN	PC13		PC0	PD6	PA0			Pulse Counter PCNT0 input number 0.
PCNT0_S1IN	PC14		PC1	PD7	PB11			Pulse Counter PCNT0 input number 1.
PRS_CH0	PA0		PC14	PF2				Peripheral Reflex System PRS, channel 0.
PRS_CH1	PA1		PC15	PE12				Peripheral Reflex System PRS, channel 1.
PRS_CH2	PC0		PE10	PE13				Peripheral Reflex System PRS, channel 2.
PRS_CH3	PC1		PE11	PA0				Peripheral Reflex System PRS, channel 3.
TIM0_CC0	PA0	PA0			PA0	PF0	PA1	Timer 0 Capture Compare input / output channel 0.
TIM0_CC1	PA1	PA1			PC0	PF1	PA0	Timer 0 Capture Compare input / output channel 1.
TIM0_CC2	PA2	PA2			PC1	PF2	PF2	Timer 0 Capture Compare input / output channel 2.
TIM0_CDTI0		PC13					PC13	Timer 0 Complimentary Deat Time Insertion channel 0.
TIM0_CDTI1		PC14					PC14	Timer 0 Complimentary Deat Time Insertion channel 1.
TIM0_CDTI2		PC15					PC15	Timer 0 Complimentary Deat Time Insertion channel 2.
TIM1_CC0	PC13	PE10		PB7	PD6			Timer 1 Capture Compare input / output channel 0.
TIM1_CC1	PC14	PE11		PB8	PD7			Timer 1 Capture Compare input / output channel 1.
TIM1_CC2	PC15	PE12		PB11	PC13			Timer 1 Capture Compare input / output channel 2.
TIM2_CC0				PF2				Timer 2 Capture Compare input / output channel 0.
TIM2_CC1				PE12				Timer 2 Capture Compare input / output channel 1.
TIM2_CC2				PE13				Timer 2 Capture Compare input / output channel 2.
US0_CLK	PE12			PC15	PB13	PB13	PE12	USART0 clock input / output.
US0_CS	PE13			PC14	PB14	PB14	PE13	USART0 chip select input / output.
US0_RX	PE11			PE12	PB8	PC1	PC1	USART0 Asynchronous Receive. USART0 Synchronous mode Master Input / Slave Output (MISO).
US0_TX	PE10			PE13	PB7	PC0	PC0	USART0 Asynchronous Transmit.Also used as receive input in half duplex communication. USART0 Synchronous mode Master Output / Slave Input (MOSI).
US1_CLK	PB7		PF0	PC15	PB11			USART1 clock input / output.
US1_CS	PB8		PF1	PC14	PC14	PC0		USART1 chip select input / output.
US1_RX	PC1		PD6	PD6	PA0			USART1 Asynchronous Receive.

7.4 Revision 0.20

December 11th, 2014

Preliminary Release.

B Contact Information

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Please visit the Silicon Labs Technical Support web page:
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ARM Cortex-M3
GECKO
ARM Cortex-M3
LEOPARD
ARM Cortex-M3
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WONDER
ARM Cortex-M4