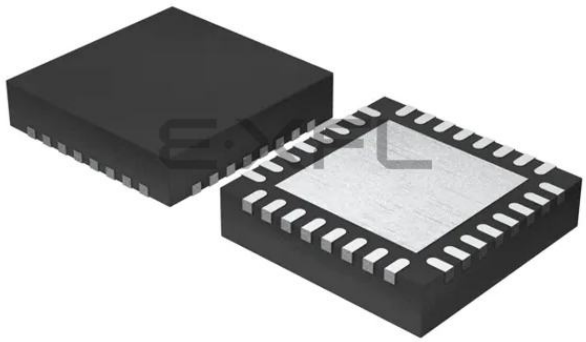

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Discontinued at Digi-Key |
| Core Processor | ARM® Cortex®-M0+ |
| Core Size | 32-Bit Single-Core |
| Speed | 25MHz |
| Connectivity | I²C, IrDA, SmartCard, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT |
| Number of I/O | 24 |
| Program Memory Size | 64KB (64K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 8K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.98V ~ 3.8V |
| Data Converters | A/D 4x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 32-VQFN Exposed Pad |
| Supplier Device Package | 32-QFN (6x6) |
| Purchase URL | https://www.e-xfl.com/product-detail/silicon-labs/efm32hg210f64g-a-qfn32r |

# 1 Ordering Information

Table 1.1 (p. 2) shows the available EFM32HG210 devices.

***Table 1.1. Ordering Information***

| Ordering Code | Flash (kB) | RAM (kB) | Max Speed (MHz) | Supply Voltage (V) | Temperature (ºC) | Package |
|---|---|---|---|---|---|---|
| EFM32HG210F32G-B-QFN32 | 32 | 4 | 25 | 1.98 - 3.8 | -40 - 85 | QFN32 |
| EFM32HG210F64G-B-QFN32 | 64 | 8 | 25 | 1.98 - 3.8 | -40 - 85 | QFN32 |

Adding the suffix 'R' to the part number (e.g. EFM32HG210F32G-B-QFN32R) denotes tape and reel.

Visit **www.silabs.com** for information on global distributors and representatives.

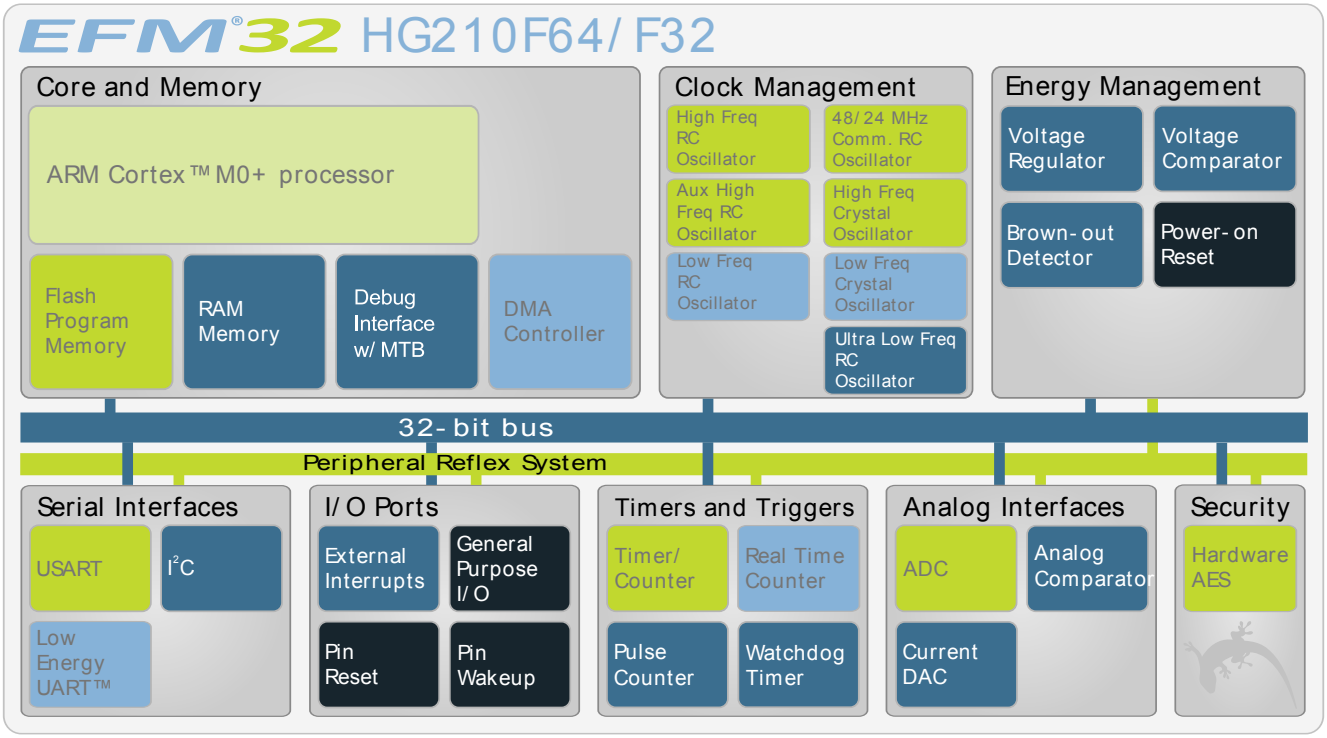
# 2 System Summary

## 2.1 System Introduction

The EFM32 MCUs are the world's most energy friendly microcontrollers. With a unique combination of the powerful 32-bit ARM Cortex-M0+, innovative low energy techniques, short wake-up time from energy saving modes, and a wide selection of peripherals, the EFM32HG microcontroller is well suited for any battery operated application as well as other systems requiring high performance and low-energy consumption. This section gives a short introduction to each of the modules in general terms and also shows a summary of the configuration for the EFM32HG210 devices. For a complete feature set and in-depth information on the modules, the reader is referred to the *EFM32HG Reference Manual*.

A block diagram of the EFM32HG210 is shown in Figure 2.1 (p. 3) .

***Figure 2.1. Block Diagram***




### 2.1.1 ARM Cortex-M0+ Core

The ARM Cortex-M0+ includes a 32-bit RISC processor which can achieve as much as 0.9 Dhrystone MIPS/MHz. A Wake-up Interrupt Controller handling interrupts triggered while the CPU is asleep is included as well. The EFM32 implementation of the Cortex-M0+ is described in detail in *ARM Cortex-M0+ Devices Generic User Guide*.

### 2.1.2 Debug Interface (DBG)

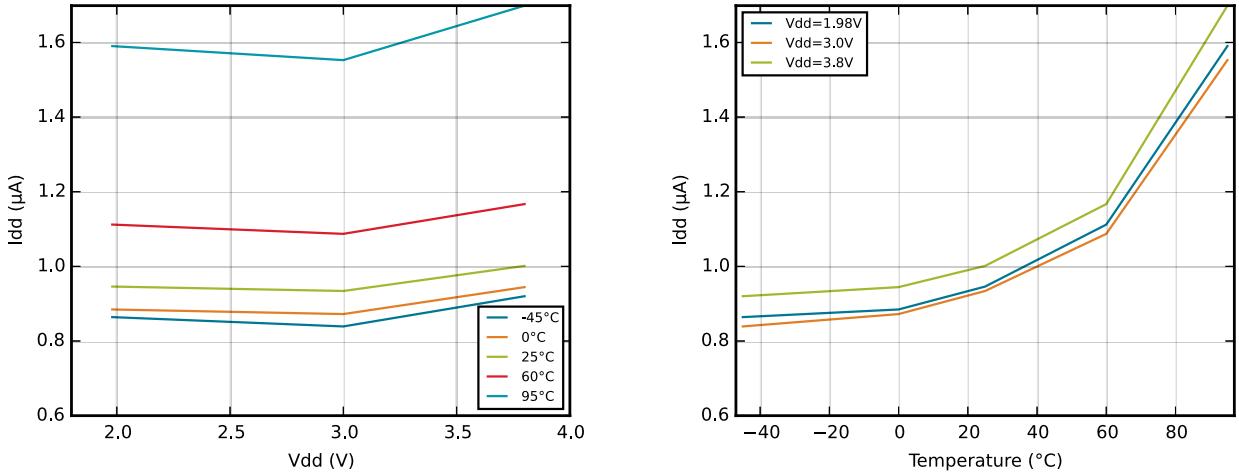
This device includes hardware debug support through a 2-pin serial-wire debug interface and a Micro Trace Buffer (MTB) for data/instruction tracing.

### 2.1.3 Memory System Controller (MSC)

The Memory System Controller (MSC) is the program memory unit of the EFM32HG microcontroller. The flash memory is readable and writable from both the Cortex-M0+ and DMA. The flash memory is divided into two blocks; the main block and the information block. Program code is normally written to the main block. Additionally, the information block is available for special user data and flash lock bits.

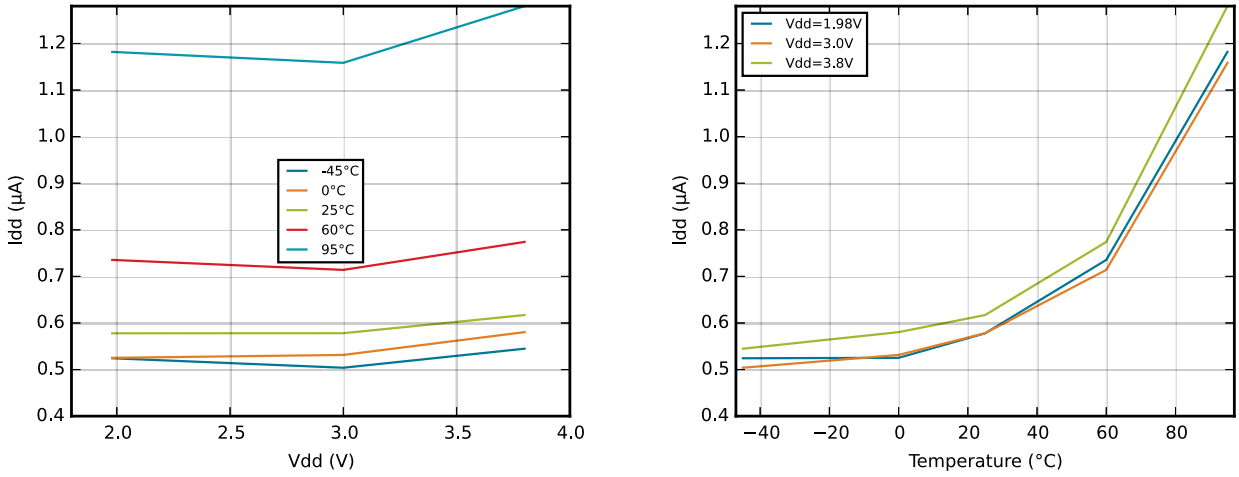
## 3.4.3 EM2 Current Consumption

***Figure 3.11. EM2 current consumption. RTC prescaled to 1kHz, 32.768 kHz LFRCO.***




## 3.4.4 EM3 Current Consumption

***Figure 3.12. EM3 current consumption.***



### Table 3.5. Power Management

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{BODextthr-}$ | BOD threshold on falling external supply voltage | EM0 | 1.74 | | 1.96 | V |
| | | EM2 | 1.71 | 1.86 | 1.98 | V |
| $V_{BODextthr+}$ | BOD threshold on rising external supply voltage | | | 1.85 | | V |
| $t_{RESET}$ | Delay from reset is released until program execution starts | Applies to Power-on Reset, Brown-out Reset and pin reset. | | 163 | | µs |
| $C_{DECOUPLE}$ | Voltage regulator decoupling capacitor. | X5R capacitor recommended. Apply between DECOUPLE pin and GROUND | | 1 | | µF |

## 3.7 Flash

### Table 3.6. Flash

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $EC_{FLASH}$ | Flash erase cycles before failure | | 20000 | | | cycles |
| $RET_{FLASH}$ | Flash data retention | $T_{AMB}$<150°C | 10000 | | | h |
| | | $T_{AMB}$<85°C | 10 | | | years |
| | | $T_{AMB}$<70°C | 20 | | | years |
| $t_{W\_PROG}$ | Word (32-bit) programming time | | 20 | | | µs |
| $t_{P\_ERASE}$ | Page erase time | | 20 | 20.4 | 20.8 | ms |
| $t_{D\_ERASE}$ | Device erase time | | 40 | 40.8 | 41.6 | ms |
| $I_{ERASE}$ | Erase current | | | | 7[1] | mA |
| $I_{WRITE}$ | Write current | | | | 7[1] | mA |
| $V_{FLASH}$ | Supply voltage during flash erase and write | | 1.98 | | 3.8 | V |

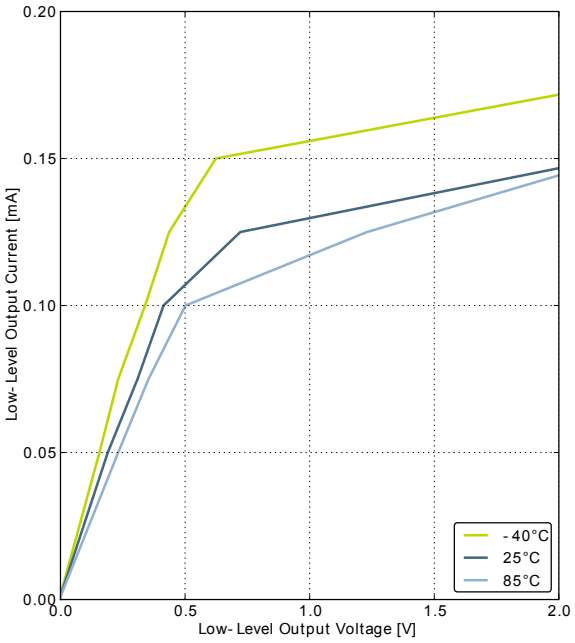
[1]Measured at 25°C

## 3.8 General Purpose Input Output

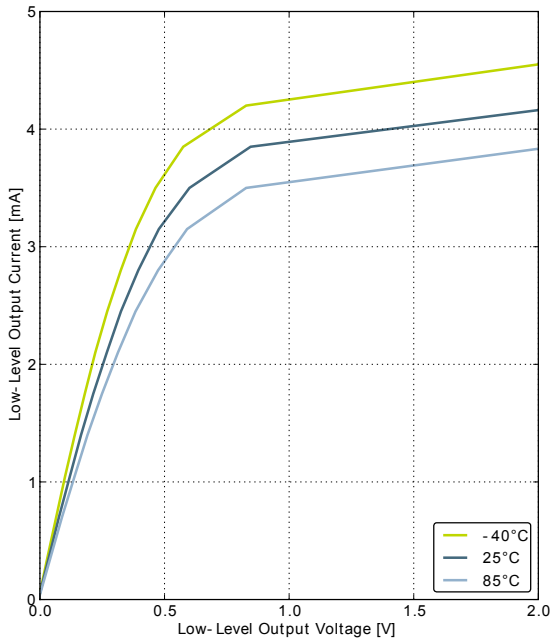
### Table 3.7. GPIO

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IOIL}$ | Input low voltage | | | | $0.30V_{DD}$ | V |
| $V_{IOIH}$ | Input high voltage | | $0.70V_{DD}$ | | | V |
| $V_{IOOH}$ | Output high voltage (Production test condition = 3.0V, DRIVEMODE = STANDARD) | Sourcing 0.1 mA, $V_{DD}$=1.98 V, GPIO_Px_CTRL DRIVEMODE = LOWEST | | $0.80V_{DD}$ | | V |
| | | Sourcing 0.1 mA, $V_{DD}$=3.0 V, GPIO_Px_CTRL DRIVEMODE = LOWEST | | $0.90V_{DD}$ | | V |

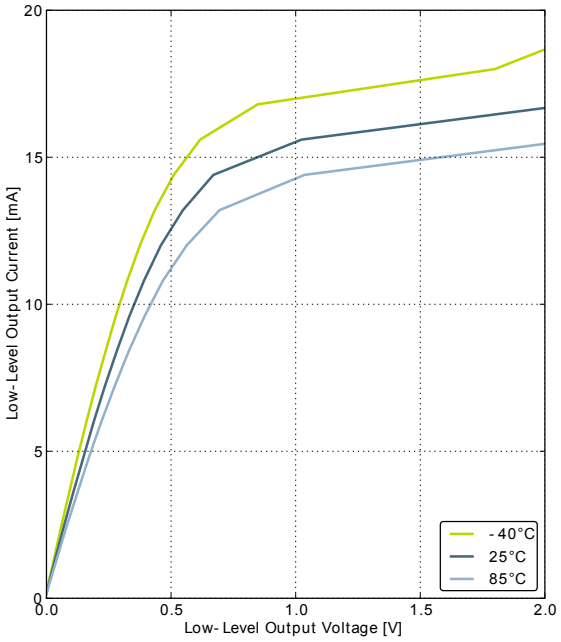
***Figure 3.14. Typical Low-Level Output Current, 2V Supply Voltage***



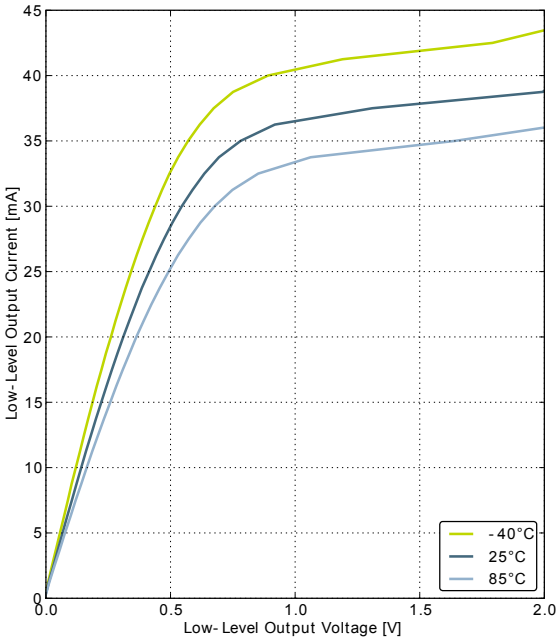

GPIO_Px_CTRL DRIVEMODE = LOWEST




GPIO_Px_CTRL DRIVEMODE = LOW

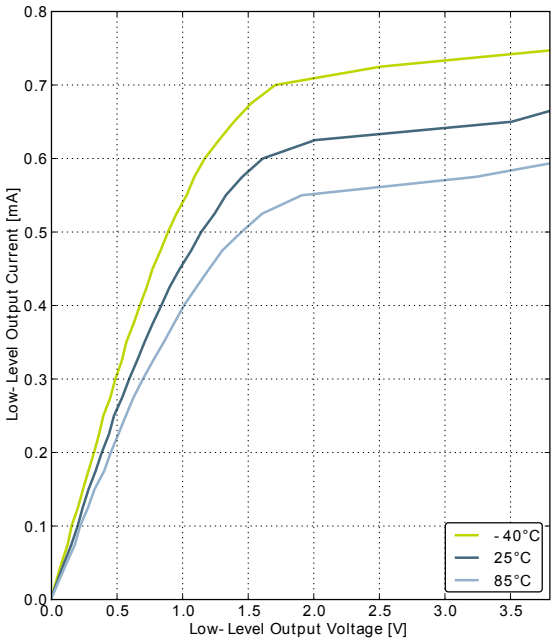



GPIO_Px_CTRL DRIVEMODE = STANDARD

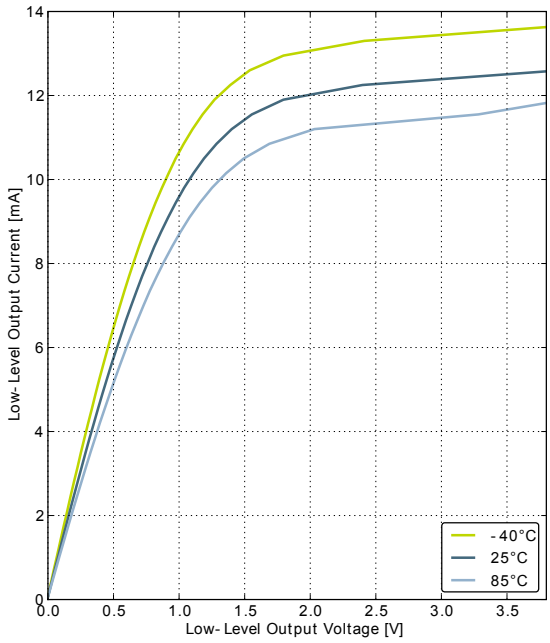



GPIO_Px_CTRL DRIVEMODE = HIGH

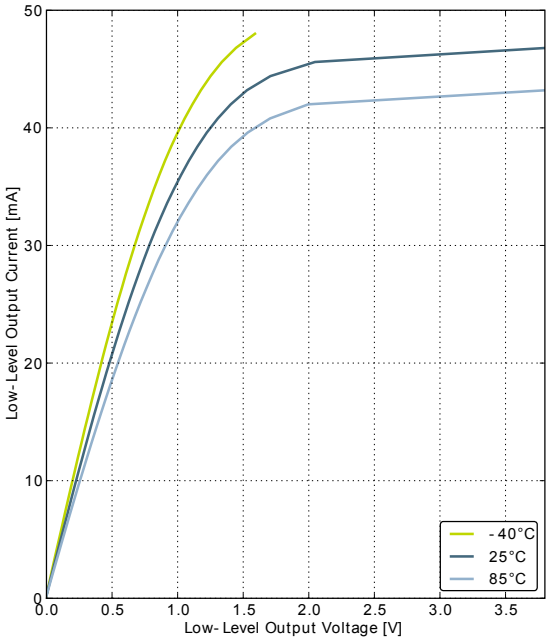
***Figure 3.18. Typical Low-Level Output Current, 3.8V Supply Voltage***



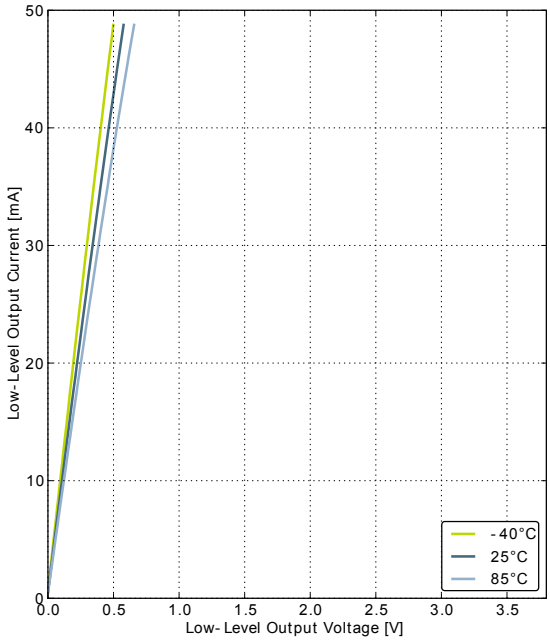

GPIO_Px_CTRL DRIVEMODE = LOWEST




GPIO_Px_CTRL DRIVEMODE = LOW

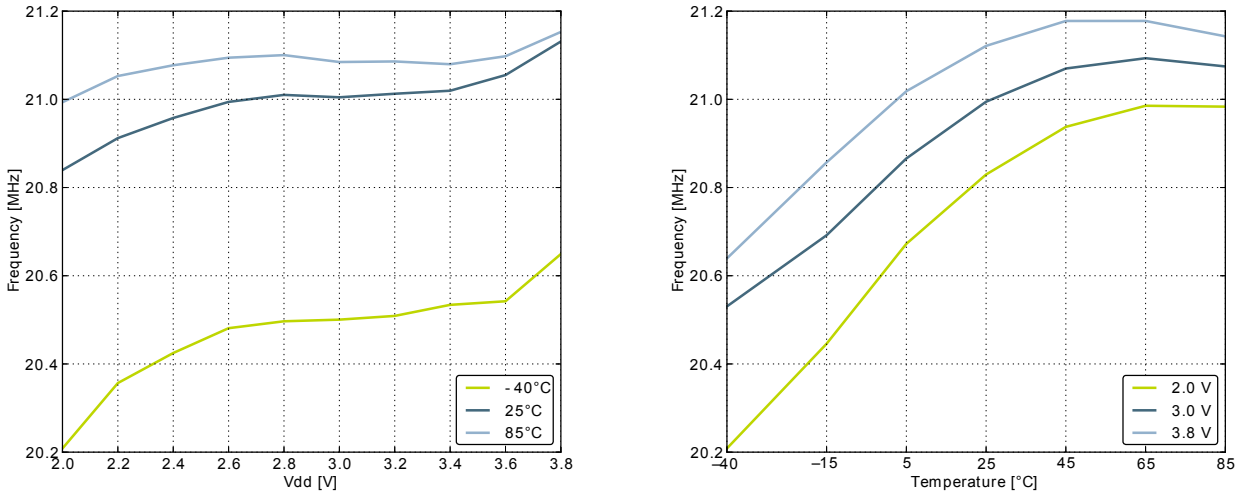



GPIO_Px_CTRL DRIVEMODE = STANDARD




GPIO_Px_CTRL DRIVEMODE = HIGH

*Figure 3.25. Calibrated HFRCO 21 MHz Band Frequency vs Supply Voltage and Temperature*




## 3.9.5 AUXHFRCO

*Table 3.12. AUXHFRCO*

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{AUXHFRCO}$ | Oscillation frequency, $V_{DD}$= 3.0 V, $T_{AMB}$=25°C | 21 MHz frequency band | 20.37 | 21.0 | 21.63 | MHz |
| | | 14 MHz frequency band | 13.58 | 14.0 | 14.42 | MHz |
| | | 11 MHz frequency band | 10.67 | 11.0 | 11.33 | MHz |
| | | 7 MHz frequency band | 6.40 | 6.60 | 6.80 | MHz |
| | | 1 MHz frequency band | 1.15 | 1.20 | 1.25 | MHz |
| $t_{AUXHFRCO\_settling}$ | Settling time after start-up | $f_{AUXHFRCO}$ = 14 MHz | | 0.6 | | Cycles |
| $TUNESTEP_{AUXHFRCO}$ | Frequency step for LSB change in TUNING value | 21 MHz frequency band | | 52.8 | | kHz |
| | | 14 MHz frequency band | | 36.9 | | kHz |
| | | 11 MHz frequency band | | 30.1 | | kHz |
| | | 7 MHz frequency band | | 18.0 | | kHz |
| | | 1 MHz frequency band | | 3.4 | | kHz |

### 3.9.6 USHFRCO

*Table 3.13. USHFRCO*

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{USHFRCO}$ | Oscillation frequency | No Clock Recovery, Full Temperature and Supply Range, 48 MHz band | 47.10 | 48.00 | 48.90 | MHz |
| | | No Clock Recovery, Full Temperature and Supply Range, 24 MHz band | 23.73 | 24.00 | 24.32 | MHz |
| | | No Clock Recovery, 25°C, 3.3V, 48 MHz band | 47.50 | 48.00 | 48.50 | MHz |
| | | No Clock Recovery, 25°C, 3.3V, 24 MHz band | 23.86 | 24.00 | 24.16 | MHz |
| $TC_{USHFRCO}$ | Temperature coefficient | 3.3V | | 0.0175 | | %/°C |
| $VC_{USHFRCO}$ | Supply voltage coefficient | 25°C | | 0.0045 | | %/V |
| $I_{USHFRCO}$ | Current consumption | $f_{USHFRCO}$ = 48 MHz | 1.21 | 1.36 | 1.48 | mA |
| | | $f_{USHFRCO}$ = 24 MHz | 0.81 | 0.92 | 1.02 | mA |

### 3.9.7 ULFRCO

*Table 3.14. ULFRCO*

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{ULFRCO}$ | Oscillation frequency | 25°C, 3V | 0.70 | | 1.75 | kHz |
| $TC_{ULFRCO}$ | Temperature coefficient | | | 0.05 | | %/°C |
| $VC_{ULFRCO}$ | Supply voltage coefficient | | | -18.2 | | %/V |

## 3.10 Analog Digital Converter (ADC)

*Table 3.15. ADC*

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{ADCIN}$ | Input voltage range | Single ended | 0 | | $V_{REF}$ | V |
| | | Differential | $-V_{REF}/2$ | | $V_{REF}/2$ | V |
| $V_{ADCREFIN}$ | Input range of external reference voltage, single ended and differential | | 1.25 | | $V_{DD}$ | V |
| $V_{ADCREFIN\_CH7}$ | Input range of external negative reference voltage on channel 7 | See $V_{ADCREFIN}$ | 0 | | $V_{DD}$ - 1.1 | V |
| $V_{ADCREFIN\_CH6}$ | Input range of external positive reference voltage on channel 6 | See $V_{ADCREFIN}$ | 0.625 | | $V_{DD}$ | V |

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{ADCCMIN}$ | Common mode input range | | 0 | | $V_{DD}$ | V |
| $I_{ADCIN}$ | Input current | 2pF sampling capacitors | | <100 | | nA |
| $CMRR_{ADC}$ | Analog input common mode rejection ratio | | | 65 | | dB |
| $I_{ADC}$ | Average active current | 1 MSamples/s, 12 bit, external reference | | 392 | 510 | µA |
| | | 10 kSamples/s 12 bit, internal 1.25 V reference, WARMUPMODE in ADCn_CTRL set to 0b00 | | 67 | | µA |
| | | 10 kSamples/s 12 bit, internal 1.25 V reference, WARMUPMODE in ADCn_CTRL set to 0b01 | | 63 | | µA |
| | | 10 kSamples/s 12 bit, internal 1.25 V reference, WARMUPMODE in ADCn_CTRL set to 0b10 | | 64 | | µA |
| | | 10 kSamples/s 12 bit, internal 1.25 V reference, WARMUPMODE in ADCn_CTRL set to 0b11 | | 244 | | µA |
| $I_{ADCREF}$ | Current consumption of internal voltage reference | Internal voltage reference | | 65 | | µA |
| $C_{ADCIN}$ | Input capacitance | | | 2 | | pF |
| $R_{ADCIN}$ | Input ON resistance | | 1 | | | MOhm |
| $R_{ADCFILT}$ | Input RC filter resistance | | | 10 | | kOhm |
| $C_{ADCFILT}$ | Input RC filter/decoupling capacitance | | | 250 | | fF |
| $f_{ADCCLK}$ | ADC Clock Frequency | | | | 13 | MHz |
| $t_{ADCCONV}$ | Conversion time | 6 bit | 7 | | | ADCCLK Cycles |
| | | 8 bit | 11 | | | ADCCLK Cycles |
| | | 12 bit | 13 | | | ADCCLK Cycles |
| $t_{ADCACQ}$ | Acquisition time | Programmable | 1 | | 256 | ADCCLK Cycles |
| $t_{ADCACQVDD3}$ | Required acquisition time for VDD/3 reference | | 2 | | | µs |

***Figure 3.26. Integral Non-Linearity (INL)***

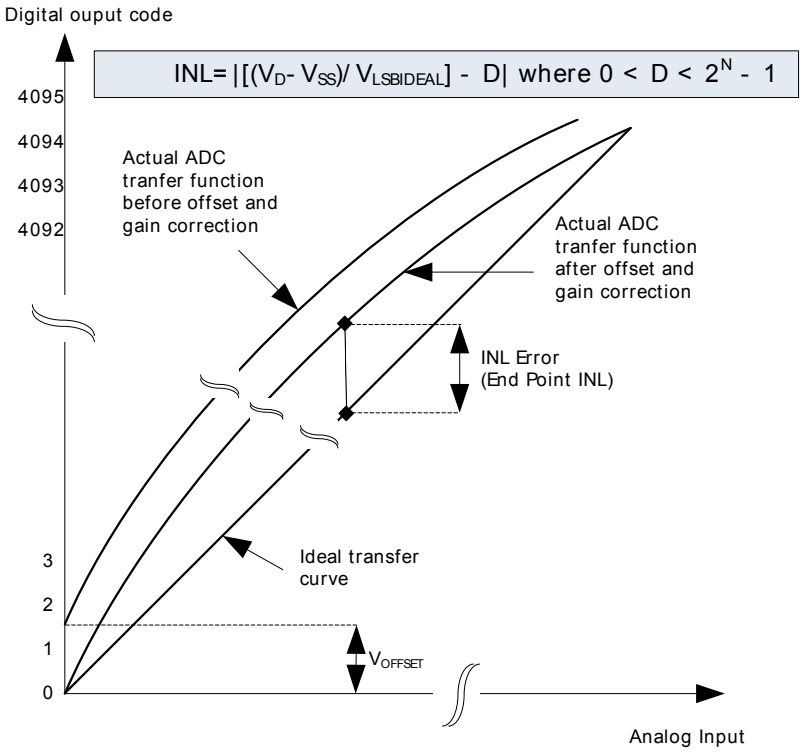



***Figure 3.27. Differential Non-Linearity (DNL)***

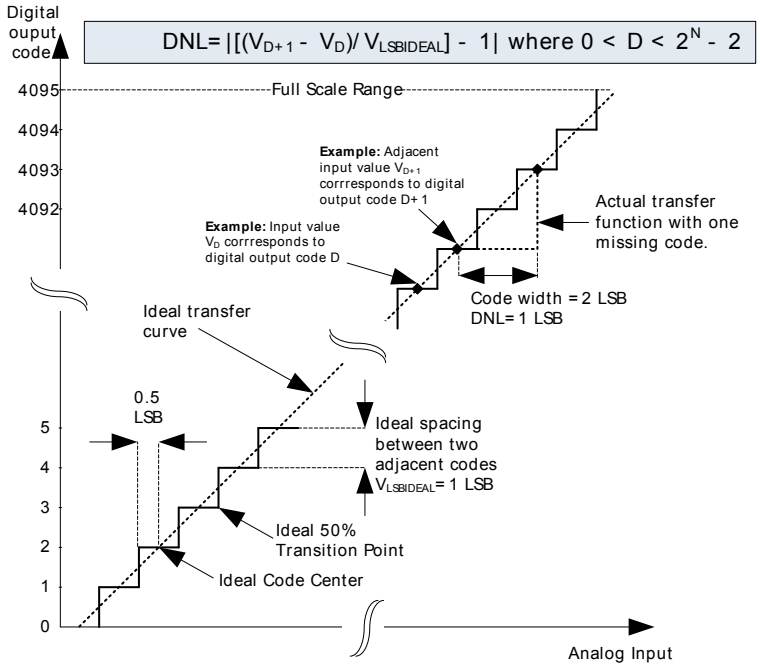
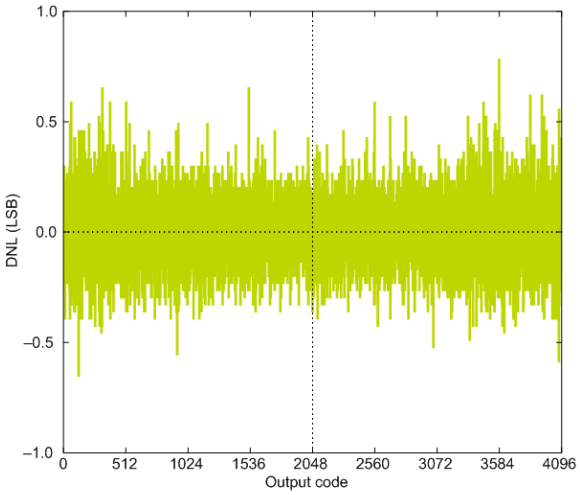
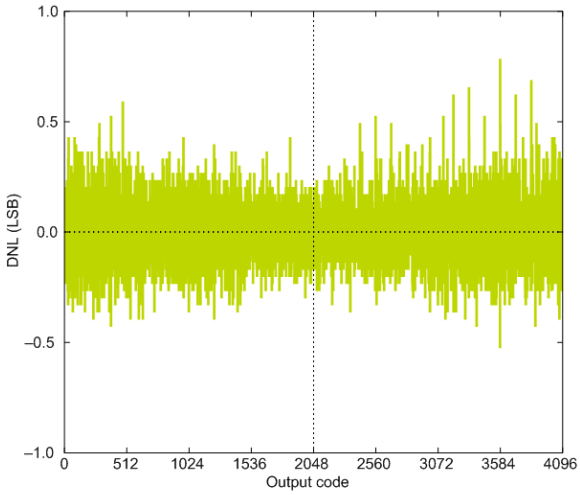


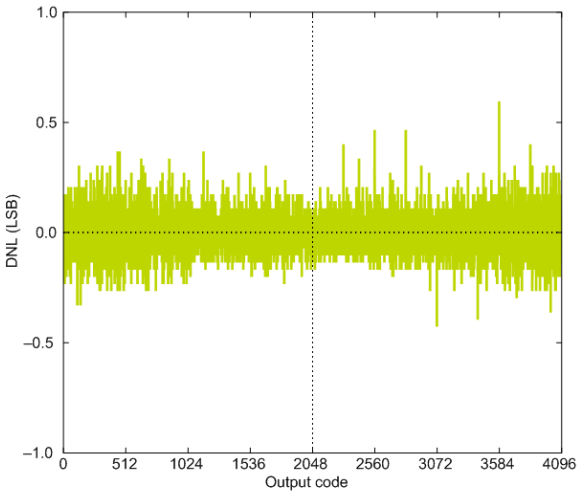
***Figure 3.30. ADC Differential Linearity Error vs Code, Vdd = 3V, Temp = 25°C***



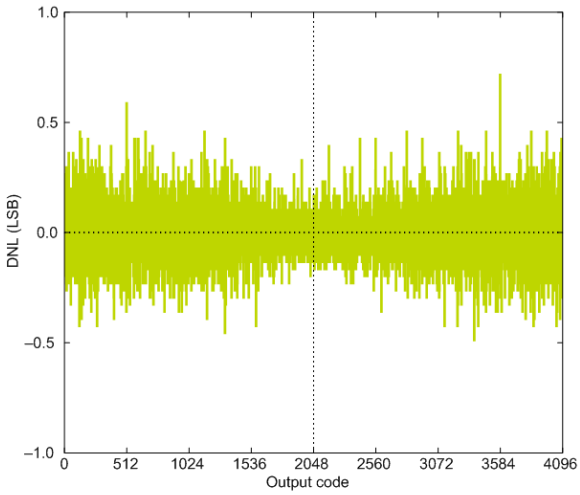

1.25V Reference



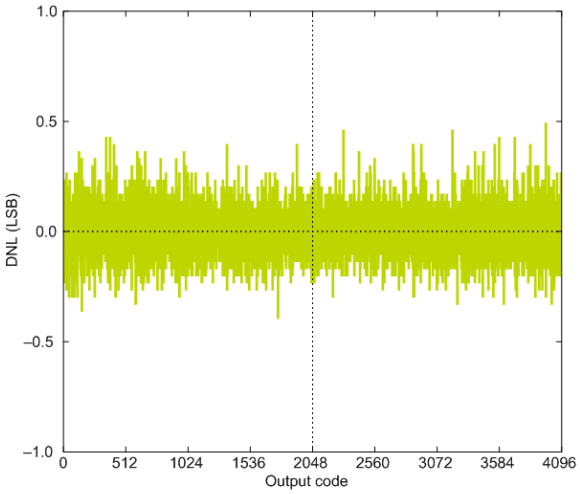

2.5V Reference




2XVDDVSS Reference




5VDIFF Reference




VDD Reference

### Table 3.18. IDAC Range 1 Source

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{IDAC}$ | Active current with STEPSEL=0x10 | EM0, default settings | | 14.4 | | µA |
| | | Duty-cycled | | 10 | | nA |
| $I_{0x10}$ | Nominal IDAC output current with STEPSEL=0x10 | | | 3.2 | | µA |
| $I_{STEP}$ | Step size | | | 0.1 | | µA |
| $I_D$ | Current drop at high impedance load | $V_{IDAC\_OUT}$ = $V_{DD}$ - 100mV | | 0.75 | | % |
| $TC_{IDAC}$ | Temperature coefficient | $V_{DD}$ = 3.0 V, STEPSEL=0x10 | | 0.7 | | nA/°C |
| $VC_{IDAC}$ | Voltage coefficient | T = 25 °C, STEPSEL=0x10 | | 38.4 | | nA/V |

### Table 3.19. IDAC Range 1 Sink

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{IDAC}$ | Active current with STEPSEL=0x10 | EM0, default settings | | 19.4 | | µA |
| $I_{0x10}$ | Nominal IDAC output current with STEPSEL=0x10 | | | 3.2 | | µA |
| $I_{STEP}$ | Step size | | | 0.1 | | µA |
| $I_D$ | Current drop at high impedance load | $V_{IDAC\_OUT}$ = 200 mV | | 0.32 | | % |
| $TC_{IDAC}$ | Temperature coefficient | $V_{DD}$ = 3.0 V, STEPSEL=0x10 | | 0.7 | | nA/°C |
| $VC_{IDAC}$ | Voltage coefficient | T = 25 °C, STEPSEL=0x10 | | 40.9 | | nA/V |

### Table 3.20. IDAC Range 2 Source

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{IDAC}$ | Active current with STEPSEL=0x10 | EM0, default settings | | 17.3 | | µA |
| | | Duty-cycled | | 10 | | nA |
| $I_{0x10}$ | Nominal IDAC output current with STEPSEL=0x10 | | | 8.5 | | µA |
| $I_{STEP}$ | Step size | | | 0.5 | | µA |
| $I_D$ | Current drop at high impedance load | $V_{IDAC\_OUT}$ = $V_{DD}$ - 100mV | | 1.22 | | % |
| $TC_{IDAC}$ | Temperature coefficient | $V_{DD}$ = 3.0 V, STEPSEL=0x10 | | 2.8 | | nA/°C |
| $VC_{IDAC}$ | Voltage coefficient | T = 25 °C, STEPSEL=0x10 | | 96.6 | | nA/V |

### Table 3.21. IDAC Range 2 Sink

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{IDAC}$ | Active current with STEPSEL=0x10 | EM0, default settings | | 29.3 | | µA |

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{0x10}$ | Nominal IDAC output current with STEPSEL=0x10 | | | 8.5 | | µA |
| $I_{STEP}$ | Step size | | | 0.5 | | µA |
| $I_D$ | Current drop at high impedance load | $V_{IDAC\_OUT}$ = 200 mV | | 0.62 | | % |
| $TC_{IDAC}$ | Temperature coefficient | $V_{DD}$ = 3.0 V, STEPSEL=0x10 | | 2.8 | | nA/°C |
| $VC_{IDAC}$ | Voltage coefficient | T = 25 °C, STEPSEL=0x10 | | 94.4 | | nA/V |

*Table 3.22. IDAC Range 3 Source*

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{IDAC}$ | Active current with STEPSEL=0x10 | EM0, default settings | | 18.7 | | µA |
| | | Duty-cycled | | 10 | | nA |
| $I_{0x10}$ | Nominal IDAC output current with STEPSEL=0x10 | | | 33.9 | | µA |
| $I_{STEP}$ | Step size | | | 2.0 | | µA |
| $I_D$ | Current drop at high impedance load | $V_{IDAC\_OUT}$ = $V_{DD}$ - 100 mV | | 3.54 | | % |
| $TC_{IDAC}$ | Temperature coefficient | $V_{DD}$ = 3.0 V, STEPSEL=0x10 | | 10.9 | | nA/°C |
| $VC_{IDAC}$ | Voltage coefficient | T = 25 °C, STEPSEL=0x10 | | 159.5 | | nA/V |

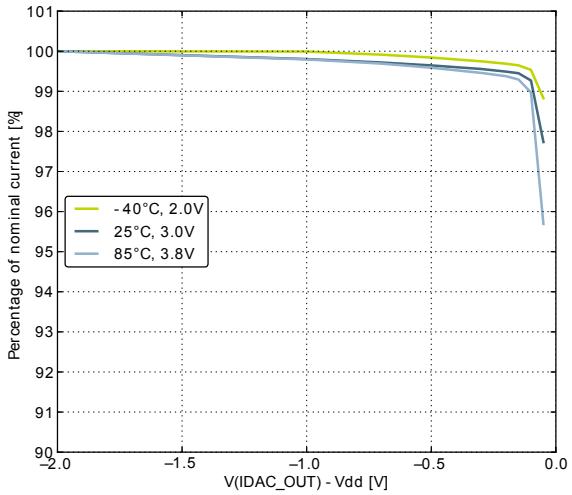
*Table 3.23. IDAC Range 3 Sink*

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{IDAC}$ | Active current with STEPSEL=0x10 | EM0, default settings | | 62.5 | | µA |
| $I_{0x10}$ | Nominal IDAC output current with STEPSEL=0x10 | | | 34.1 | | µA |
| $I_{STEP}$ | Step size | | | 2.0 | | µA |
| $I_D$ | Current drop at high impedance load | $V_{IDAC\_OUT}$ = 200 mV | | 1.75 | | % |
| $TC_{IDAC}$ | Temperature coefficient | $V_{DD}$ = 3.0 V, STEPSEL=0x10 | | 10.9 | | nA/°C |
| $VC_{IDAC}$ | Voltage coefficient | T = 25 °C, STEPSEL=0x10 | | 148.6 | | nA/V |

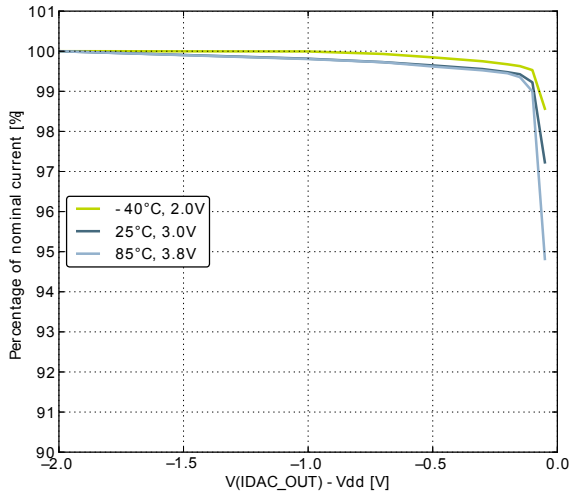
*Table 3.24. IDAC*

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $t_{IDACSTART}$ | Start-up time, from enabled to output settled | | 40 | | µs |

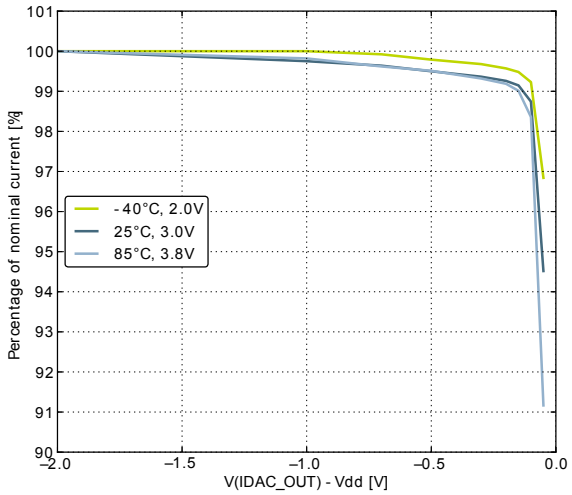
***Figure 3.34. IDAC Source Current as a function of voltage on IDAC_OUT***



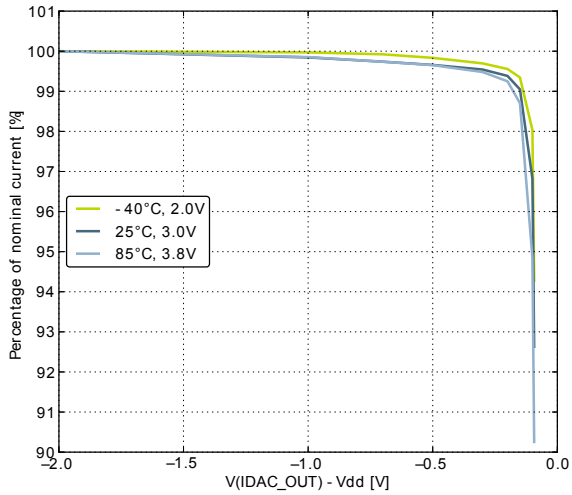

Range 0




Range 1

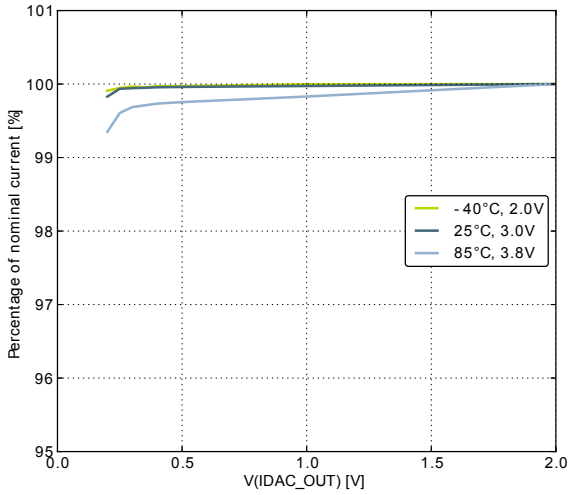



Range 2

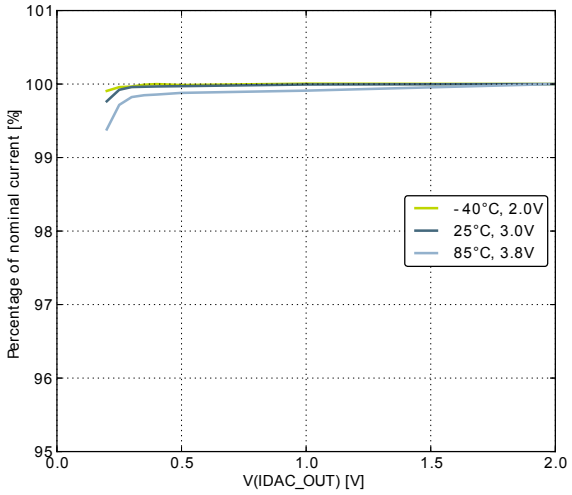



Range 3

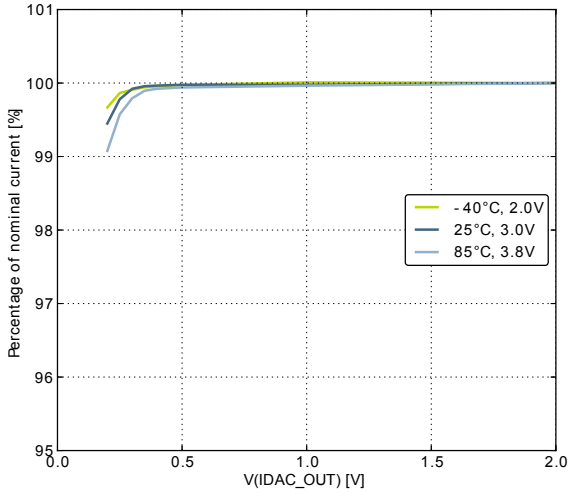
***Figure 3.35. IDAC Sink Current as a function of voltage from IDAC_OUT***



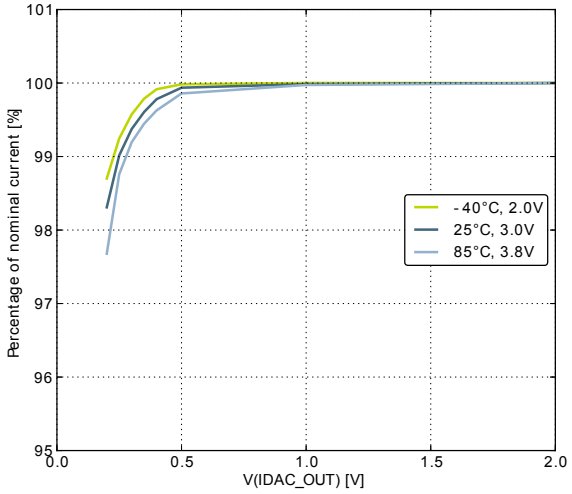

Range 0




Range 1

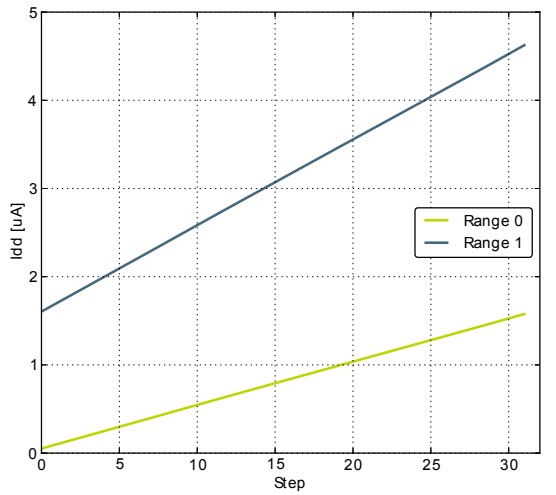


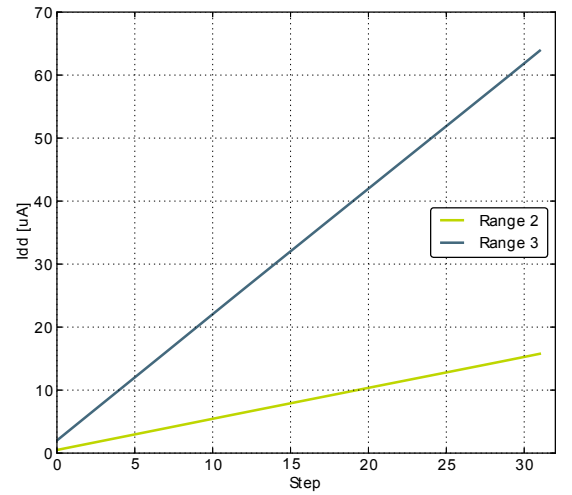

Range 2




Range 3

***Figure 3.36. IDAC linearity***



| QFN32 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| | | | TIM0_CC1 #0/1 | | PRS_CH1 #0 |
| 3 | PA2 | | TIM0_CC2 #0/1 | | CMU_CLK0 #0 |
| 4 | IOVDD_0 | Digital IO power supply 0. | | | |
| 5 | PC0 | ACMP0_CH0 | TIM0_CC1 #4<br>PCNT0_S0IN #2 | US0_TX #5/6<br>US1_TX #0<br>US1_CS #5<br>I2C0_SDA #4 | PRS_CH2 #0 |
| 6 | PC1 | ACMP0_CH1 | TIM0_CC2 #4<br>PCNT0_S1IN #2 | US0_RX #5/6<br>US1_TX #5<br>US1_RX #0<br>I2C0_SCL #4 | PRS_CH3 #0 |
| 7 | PB7 | LFXTAL_P | TIM1_CC0 #3 | US0_TX #4<br>US1_CLK #0 | |
| 8 | PB8 | LFXTAL_N | TIM1_CC1 #3 | US0_RX #4<br>US1_CS #0 | |
| 9 | RESETn | Reset input, active low.<br>To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released. | | | |
| 10 | PB11 | IDAC0_OUT | TIM1_CC2 #3<br>PCNT0_S1IN #4 | US1_CLK #4 | CMU_CLK1 #3<br>ACMP0_O #3 |
| 11 | AVDD_2 | Analog power supply 2. | | | |
| 12 | PB13 | HFXTAL_P | | US0_CLK #4/5<br>LEU0_TX #1 | |
| 13 | PB14 | HFXTAL_N | | US0_CS #4/5<br>LEU0_RX #1 | |
| 14 | IOVDD_3 | Digital IO power supply 3. | | | |
| 15 | AVDD_0 | Analog power supply 0. | | | |
| 16 | PD4 | ADC0_CH4 | | LEU0_TX #0 | |
| 17 | PD5 | ADC0_CH5 | | LEU0_RX #0 | |
| 18 | PD6 | ADC0_CH6 | TIM1_CC0 #4<br>PCNT0_S0IN #3 | US1_RX #2/3<br>I2C0_SDA #1 | ACMP0_O #2 |
| 19 | PD7 | ADC0_CH7 | TIM1_CC1 #4<br>PCNT0_S1IN #3 | US1_TX #2/3<br>I2C0_SCL #1 | CMU_CLK0 #2 |
| 20 | VDD_DREG | Power supply for on-chip voltage regulator. | | | |
| 21 | DECOUPLE | Decouple output for on-chip voltage regulator. An external capacitance of size $C_{DECOUPLE}$ is required at this pin. | | | |
| 22 | PC13 | | TIM0_CDTI0 #1/6<br>TIM1_CC0 #0<br>TIM1_CC2 #4<br>PCNT0_S0IN #0 | | |
| 23 | PC14 | | TIM0_CDTI1 #1/6<br>TIM1_CC1 #0<br>PCNT0_S1IN #0 | US0_CS #3<br>US1_CS #3/4<br>LEU0_TX #5 | PRS_CH0 #2 |
| 24 | PC15 | | TIM0_CDTI2 #1/6<br>TIM1_CC2 #0 | US0_CLK #3<br>US1_CLK #3<br>LEU0_RX #5 | PRS_CH1 #2 |
| 25 | PF0 | | TIM0_CC0 #5 | US1_CLK #2<br>LEU0_TX #3<br>I2C0_SDA #5 | DBG_SWCLK #0<br>BOOT_TX |
| 26 | PF1 | | TIM0_CC1 #5 | US1_CS #2<br>LEU0_RX #3<br>I2C0_SCL #5 | DBG_SWDIO #0<br>GPIO_EM4WU3<br>BOOT_RX |
| 27 | PF2 | | TIM0_CC2 #5/6<br>TIM2_CC0 #3 | US1_TX #4<br>LEU0_TX #4 | CMU_CLK0 #3<br>PRS_CH0 #3<br>GPIO_EM4WU4 |

*Figure 5.3. QFN32 PCB Stencil Design*

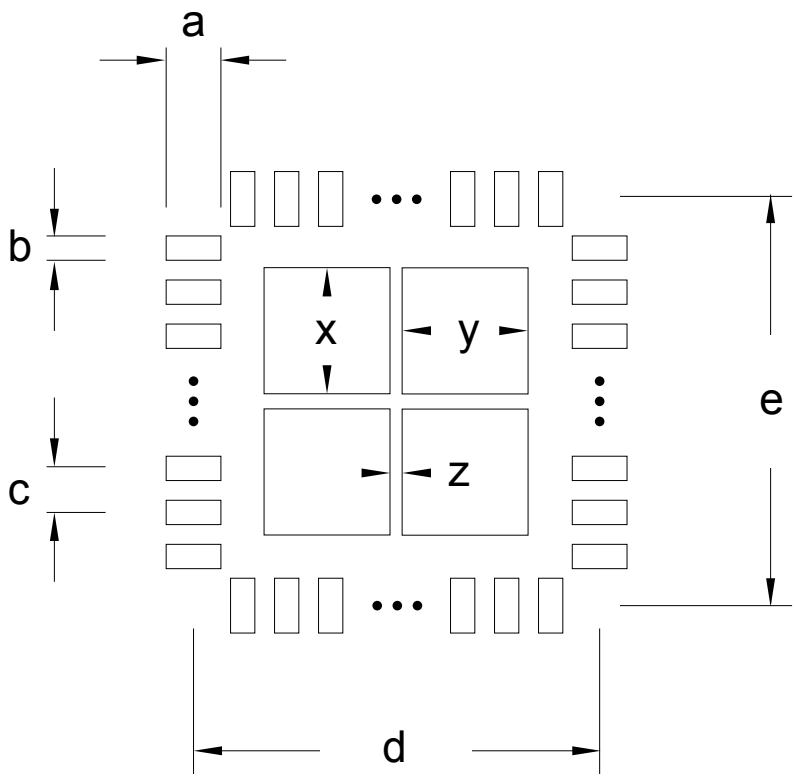



*Table 5.3. QFN32 PCB Stencil Design Dimensions (Dimensions in mm)*

| Symbol | Dim. (mm) |
|---|---|
| a | 0.70 |
| b | 0.25 |
| c | 0.65 |
| d | 6.00 |
| e | 6.00 |
| x | 1.30 |
| y | 1.30 |
| z | 0.50 |

1. The drawings are not to scale.
2. All dimensions are in millimeters.
3. All drawings are subject to change without notice.
4. The PCB Land Pattern drawing is in compliance with IPC-7351B.
5. Stencil thickness 0.125 mm.
6. For detailed pin-positioning, see Figure 4.2 (p. 56) .

## 5.2 Soldering Information

The latest IPC/JEDEC J-STD-020 recommendations for Pb-Free reflow soldering should be followed.

Place as many and as small as possible vias underneath each of the solder patches under the ground pad.

## 7.4 Revision 0.20

December 11th, 2014

Preliminary Release.

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