



Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Discontinued at Digi-Key
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	25MHz
Connectivity	I ² C, IrDA, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I ² S, POR, PWM, WDT
Number of I/O	24
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.98V ~ 3.8V
Data Converters	A/D 4x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-VQFN Exposed Pad
Supplier Device Package	32-QFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32hg210f64g-b-qfn32

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

3 Electrical Characteristics

3.1 Test Conditions

3.1.1 Typical Values

The typical data are based on T_{AMB} =25°C and V_{DD} =3.0 V, as defined in Table 3.2 (p. 8), unless otherwise specified.

3.1.2 Minimum and Maximum Values

The minimum and maximum values represent the worst conditions of ambient temperature, supply voltage and frequencies, as defined in Table 3.2 (p. 8), unless otherwise specified.

3.2 Absolute Maximum Ratings

The absolute maximum ratings are stress ratings, and functional operation under such conditions are not guaranteed. Stress beyond the limits specified in Table 3.1 (p. 8) may affect the device reliability or cause permanent damage to the device. Functional operating conditions are given in Table 3.2 (p. 8).

Table 3.1. Absolute Maximum Ratings

Symbol	Parameter	Condition	Min	Тур	Мах	Unit
T _{STG}	Storage tempera- ture range		-40		150 ¹	°C
Τ _S	Maximum soldering temperature	Latest IPC/JEDEC J-STD-020 Standard			260	°C
V _{DDMAX}	External main sup- ply voltage		0		3.8	V
VIOPIN	Voltage on any I/O pin		-0.3		V _{DD} +0.3	V

¹Based on programmed devices tested for 10000 hours at 150°C. Storage temperature affects retention of preprogrammed calibration values stored in flash. Please refer to the Flash section in the Electrical Characteristics for information on flash data retention for different temperatures.

3.3 General Operating Conditions

3.3.1 General Operating Conditions

Table 3.2. General Operating Conditions

Symbol	Parameter	Min	Тур	Мах	Unit
T _{AMB}	Ambient temperature range	-40		85	°C
V _{DDOP}	Operating supply voltage	1.98		3.8	V
f _{APB}	Internal APB clock frequency			25	MHz
f _{AHB}	Internal AHB clock frequency			25	MHz

3.4 Current Consumption

Table 3.3. Current Consumption

Symbol	Parameter	Condition	Min	Тур	Мах	Unit
		24 MHz HFXO, all peripheral clocks disabled, V_{DD} = 3.0 V, T_{AMB} =25°C		148	158	μΑ/ MHz
		24 MHz HFXO, all peripheral clocks disabled, V_{DD} = 3.0 V, T_{AMB} =85°C		153	163	μΑ/ MHz
		24 MHz USHFRCO, all peripheral clocks disabled, V_{DD} = 3.0 V, T_{AMB} =25°C		161	172	μΑ/ MHz
		24 MHz USHFRCO, all peripheral clocks disabled, V_{DD} = 3.0 V, T_{AMB} =85°C		163	174	μΑ/ MHz
		24 MHz HFRCO, all peripheral clocks disabled, V_{DD} = 3.0 V, T_{AMB} =25°C		127	137	μΑ/ MHz
		24 MHz HFRCO, all peripheral clocks disabled, V_{DD} = 3.0 V, T_{AMB} =85°C		129	139	μΑ/ MHz
	EM0 current. No prescaling. Running prime number cal- culation code from Flash.	21 MHz HFRCO, all peripheral clocks disabled, V_{DD} = 3.0 V, T_{AMB} =25°C		131	140	μΑ/ MHz
		21 MHz HFRCO, all peripheral clocks disabled, V_{DD} = 3.0 V, T_{AMB} =85°C		134	143	μΑ/ MHz
EMU		14 MHz HFRCO, all peripheral clocks disabled, V_{DD} = 3.0 V, T_{AMB} =25°C		134	143	μΑ/ MHz
		14 MHz HFRCO, all peripheral clocks disabled, V_{DD} = 3.0 V, T_{AMB} =85°C		137	145	μΑ/ MHz
		11 MHz HFRCO, all peripheral clocks disabled, V_{DD} = 3.0 V, T_{AMB} =25°C		136	144	μΑ/ MHz
		11 MHz HFRCO, all peripheral clocks disabled, V_{DD} = 3.0 V, T_{AMB} =85°C		139	148	μΑ/ MHz
		6.6 MHz HFRCO, all peripher- al clocks disabled, V_{DD} = 3.0 V, T_{AMB} =25°C		142	150	μΑ/ MHz
		6.6 MHz HFRCO, all peripheral clocks disabled, V_{DD} = 3.0 V, T_{AMB} =85°C		146	154	μΑ/ MHz
		1.2 MHz HFRCO, all peripheral clocks disabled, V_{DD} = 3.0 V, T_{AMB} =25°C		184	196	μΑ/ MHz
		1.2 MHz HFRCO, all peripheral clocks disabled, V_{DD} = 3.0 V, T_{AMB} =85°C		194	208	μΑ/ MHz

Figure 3.7. EM1 Current consumption with all peripheral clocks disabled and HFRCO running at 21 MHz



Figure 3.8. EM1 Current consumption with all peripheral clocks disabled and HFRCO running at 14 MHz



Figure 3.9. EM1 Current consumption with all peripheral clocks disabled and HFRCO running at 11 MHz



Figure 3.10. EM1 Current consumption with all peripheral clocks disabled and HFRCO running at 6.6 MHz



3.4.3 EM2 Current Consumption

Figure 3.11. EM2 current consumption. RTC prescaled to 1kHz, 32.768 kHz LFRCO.





3.4.4 EM3 Current Consumption

Figure 3.12. EM3 current consumption.



3.4.5 EM4 Current Consumption

Figure 3.13. EM4 current consumption.



3.5 Transition between Energy Modes

The transition times are measured from the trigger to the first clock edge in the CPU.

Table 3.4. Energy Modes Transitions

Symbol	Parameter	Min	Тур	Max	Unit
t _{EM10}	Transition time from EM1 to EM0		0		HF- CORE- CLK cycles
t _{EM20}	Transition time from EM2 to EM0		2		μs
t _{EM30}	Transition time from EM3 to EM0		2		μs
t _{EM40}	Transition time from EM4 to EM0		163		μs

3.6 Power Management

The EFM32HG requires the AVDD_x, VDD_DREG and IOVDD_x pins to be connected together (with optional filter) at the PCB level. For practical schematic recommendations, please see the application note, "AN0002 EFM32 Hardware Design Considerations".



...the world's most energy friendly microcontrollers

Symbol	Parameter	Condition	Min	Тур	Мах	Unit
	by the glitch sup- pression filter					
t _{IOOF}	Output fall time	GPIO_Px_CTRL DRIVEMODE = LOWEST and load capaci- tance C_L =12.5-25pF.	20+0.1C _L		250	ns
		GPIO_Px_CTRL DRIVEMODE = LOW and load capacitance C _L =350-600pF	20+0.1C _L		250	ns
V _{IOHYST}	I/O pin hysteresis (V _{IOTHR+} - V _{IOTHR-})	V _{DD} = 1.98 - 3.8 V	0.1V _{DD}			V



Figure 3.18. Typical Low-Level Output Current, 3.8V Supply Voltage



GPIO_Px_CTRL DRIVEMODE = LOWEST



GPIO_Px_CTRL DRIVEMODE = STANDARD



GPIO_Px_CTRL DRIVEMODE = LOW



GPIO_Px_CTRL DRIVEMODE = HIGH

3.9 Oscillators

3.9.1 LFXO

Table 3.8. LFXO

Symbol	Parameter	Condition	Min	Тур	Max	Unit
f _{LFXO}	Supported nominal crystal frequency			32.768		kHz
ESR _{LFXO}	Supported crystal equivalent series re- sistance (ESR)			30	120	kOhm
C _{LFXOL}	Supported crystal external load range		5		25	pF
I _{LFXO}	Current consump- tion for core and buffer after startup.	ESR=30 kOhm, C _L =10 pF, LFXOBOOST in CMU_CTRL is 1		190		nA
t _{LFXO}	Start- up time.	ESR=30 kOhm, C _L =10 pF, 40% - 60% duty cycle has been reached, LFXOBOOST in CMU_CTRL is 1		1100		ms

For safe startup of a given crystal, the Configurator tool in Simplicity Studio contains a tool to help users configure both load capacitance and software settings for using the LFXO. For details regarding the crystal configuration, the reader is referred to application note "AN0016 EFM32 Oscillator Design Consideration".

3.9.2 HFXO

Table 3.9. HFXO

Symbol	Parameter	Condition	Min	Тур	Мах	Unit
f _{HFXO}	Supported frequen- cy, any mode		4		25	MHz
	Supported crystal	Crystal frequency 25 MHz		30	100	Ohm
ESR _{HFXO}	sistance (ESR)	Crystal frequency 4 MHz		400	1500	Ohm
9mhfxo	The transconduc- tance of the HFXO input transistor at crystal startup	HFXOBOOST in CMU_CTRL equals 0b11	20			mS
C _{HFXOL}	Supported crystal external load range		5		25	pF
1	Current consump-	4 MHz: ESR=400 Ohm, C _L =20 pF, HFXOBOOST in CMU_CTRL equals 0b11		85		μA
IHFXO	startup	25 MHz: ESR=30 Ohm, C _L =10 pF, HFXOBOOST in CMU_CTRL equals 0b11		165		μA
t _{HFXO}	Startup time	25 MHz: ESR=30 Ohm, C _L =10 pF, HFXOBOOST in CMU_CTRL equals 0b11		785		μs

3.9.6 USHFRCO

Table 3.13. USHFRCO

Symbol	Parameter	Condition	Min	Тур	Max	Unit
fushfrco	Oscillation frequen- cy	No Clock Recovery, Full Tem- perature and Supply Range, 48 MHz band	47.10	48.00	48.90	MHz
		No Clock Recovery, Full Tem- perature and Supply Range, 24 MHz band	23.73	24.00	24.32	MHz
		No Clock Recovery, 25°C, 3.3V, 48 MHz band	47.50	48.00	48.50	MHz
		No Clock Recovery, 25°C, 3.3V, 24 MHz band	23.86	24.00	24.16	MHz
TC _{USHFRCO}	Temperature coeffi- cient	3.3V		0.0175		%/°C
VC _{USHFRCO}	Supply voltage co- efficient	25°C		0.0045		%/V
	Current consump-	f _{USHFRCO} = 48 MHz	1.21	1.36	1.48	mA
IUSHFRCO	tion	f _{USHFRCO} = 24 MHz	0.81	0.92	1.02	mA

3.9.7 ULFRCO

Table 3.14. ULFRCO

Symbol	Parameter	Condition	Min	Тур	Мах	Unit
fulfrco	Oscillation frequen- cy	25°C, 3V	0.70		1.75	kHz
TC _{ULFRCO}	Temperature coeffi- cient			0.05		%/°C
VC _{ULFRCO}	Supply voltage co- efficient			-18.2		%/V

3.10 Analog Digital Converter (ADC)

Table 3.15. ADC

Symbol	Parameter	Condition	Min	Тур	Мах	Unit
		Single ended	0		V _{REF}	V
V ADCIN	input voitage range	Differential	-V _{REF} /2		V _{REF} /2	V
VADCREFIN	Input range of exter- nal reference volt- age, single ended and differential		1.25		V _{DD}	V
V _{ADCREFIN_CH7}	Input range of ex- ternal negative ref- erence voltage on channel 7	See V _{ADCREFIN}	0		V _{DD} - 1.1	V
VADCREFIN_CH6	Input range of ex- ternal positive ref- erence voltage on channel 6	See V _{ADCREFIN}	0.625		V _{DD}	V



Symbol	Parameter	Condition	Min	Тур	Max	Unit
V _{ADCCMIN}	Common mode in- put range		0		V _{DD}	V
	Input current	2pF sampling capacitors		<100		nA
CMRR _{ADC}	Analog input com- mon mode rejection ratio			65		dB
		1 MSamples/s, 12 bit, external reference		392	510	μA
		10 kSamples/s 12 bit, internal 1.25 V reference, WARMUP- MODE in ADCn_CTRL set to 0b00		67		μA
I _{ADC}	Average active cur- rent	10 kSamples/s 12 bit, internal 1.25 V reference, WARMUP- MODE in ADCn_CTRL set to 0b01		63		μΑ
		10 kSamples/s 12 bit, internal 1.25 V reference, WARMUP- MODE in ADCn_CTRL set to 0b10		64		μA
		10 kSamples/s 12 bit, internal 1.25 V reference, WARMUP- MODE in ADCn_CTRL set to 0b11		244		μΑ
I _{ADCREF}	Current consump- tion of internal volt- age reference	Internal voltage reference		65		μA
C _{ADCIN}	Input capacitance			2		pF
R _{ADCIN}	Input ON resistance		1			MOhm
R _{ADCFILT}	Input RC filter resis- tance			10		kOhm
C _{ADCFILT}	Input RC filter/de- coupling capaci- tance			250		fF
f _{ADCCLK}	ADC Clock Fre- quency				13	MHz
		6 bit	7			ADC- CLK Cycles
tadcconv	Conversion time	8 bit	11			ADC- CLK Cycles
		12 bit	13			ADC- CLK Cycles
t _{ADCACQ}	Acquisition time	Programmable	1		256	ADC- CLK Cycles
t _{ADCACQVDD3}	Required acquisi- tion time for VDD/3 reference		2			μs



Symbol	Parameter	Condition	Min	Тур	Мах	Unit
		1 MSamples/s, 12 bit, differen- tial, internal 1.25V reference		60		dB
		1 MSamples/s, 12 bit, differen- tial, internal 2.5V reference		64		dB
		1 MSamples/s, 12 bit, differen- tial, 5V reference		54		dB
		1 MSamples/s, 12 bit, differen- tial, V _{DD} reference		66		dB
		1 MSamples/s, 12 bit, differen- tial, 2xV _{DD} reference		68		dB
		200 kSamples/s, 12 bit, sin- gle ended, internal 1.25V refer- ence		61		dB
		200 kSamples/s, 12 bit, single ended, internal 2.5V reference		65		dB
		200 kSamples/s, 12 bit, single ended, V _{DD} reference		66		dB
		200 kSamples/s, 12 bit, differ- ential, internal 1.25V reference		63		dB
		200 kSamples/s, 12 bit, differ- ential, internal 2.5V reference		66		dB
		200 kSamples/s, 12 bit, differ- ential, 5V reference		66		dB
		200 kSamples/s, 12 bit, differential, V_{DD} reference	62	66		dB
		200 kSamples/s, 12 bit, differ- ential, 2xV _{DD} reference		69		dB
	Spurious-Free Dy- namic Range (SF- DR)	1 MSamples/s, 12 bit, single ended, internal 1.25V refer- ence		64		dBc
		1 MSamples/s, 12 bit, single ended, internal 2.5V reference		76		dBc
		1 MSamples/s, 12 bit, single ended, V _{DD} reference		73		dBc
		1 MSamples/s, 12 bit, differen- tial, internal 1.25V reference		66		dBc
		1 MSamples/s, 12 bit, differen- tial, internal 2.5V reference		77		dBc
SFUKADC		1 MSamples/s, 12 bit, differential, V_{DD} reference		76		dBc
		1 MSamples/s, 12 bit, differen- tial, 2xV _{DD} reference		75		dBc
		1 MSamples/s, 12 bit, differen- tial, 5V reference		69		dBc
		200 kSamples/s, 12 bit, sin- gle ended, internal 1.25V refer- ence		75		dBc
		200 kSamples/s, 12 bit, single ended, internal 2.5V reference		75		dBc

Figure 3.29. ADC Integral Linearity Error vs Code, Vdd = 3V, Temp = 25°C





VDD Reference



2.5V Reference



5VDIFF Reference

Figure 3.34. IDAC Source Current as a function of voltage on IDAC_OUT





	QFN32 Pin# and Name		Pin Alternate Functio	onality / Description	
Pin#	Pin Name	Analog	Timers	Communication	Other
28	IOVDD_5	Digital IO power supply 5.			<u></u>
29	PE10		TIM1_CC0 #1	US0_TX #0	PRS_CH2 #2
30	PE11		TIM1_CC1 #1	US0_RX #0	PRS_CH3 #2
31	PE12	ADC0_CH0	TIM1_CC2 #1 TIM2_CC1 #3	US0_RX #3 US0_CLK #0/6 I2C0_SDA #6	CMU_CLK1 #2 PRS_CH1 #3
32	PE13	ADC0_CH1	TIM2_CC2 #3	US0_TX #3 US0_CS #0/6 I2C0_SCL #6	ACMP0_O #0 PRS_CH2 #3 GPIO_EM4WU5

4.2 Alternate Functionality Pinout

A wide selection of alternate functionality is available for multiplexing to various pins. This is shown in Table 4.2 (p. 54). The table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings.

Note

Some functionality, such as analog interfaces, do not have alternate settings or a LOCA-TION bitfield. In these cases, the pinout is shown in the column corresponding to LOCA-TION 0.

Table 4.2. Alternate functionality overview

Alternate			L	OCATIO	N			
Functionality	0	1	2	3	4	5	6	Description
ACMP0_CH0	PC0							Analog comparator ACMP0, channel 0.
ACMP0_CH1	PC1							Analog comparator ACMP0, channel 1.
ACMP0_O	PE13		PD6	PB11				Analog comparator ACMP0, digital output.
ADC0_CH0	PE12							Analog to digital converter ADC0, input channel number 0.
ADC0_CH1	PE13							Analog to digital converter ADC0, input channel number 1.
ADC0_CH4	PD4							Analog to digital converter ADC0, input channel number 4.
ADC0_CH5	PD5							Analog to digital converter ADC0, input channel number 5.
ADC0_CH6	PD6							Analog to digital converter ADC0, input channel number 6.
ADC0_CH7	PD7							Analog to digital converter ADC0, input channel number 7.
BOOT_RX	PF1							Bootloader RX.
BOOT_TX	PF0							Bootloader TX.
CMU_CLK0	PA2		PD7	PF2				Clock Management Unit, clock output number 0.
CMU_CLK1	PA1		PE12	PB11				Clock Management Unit, clock output number 1.
								Debug-interface Serial Wire clock input.
DBG_SWCLK	PF0							Note that this function is enabled to pin out of reset, and has a built-in pull down.
								Debug-interface Serial Wire data input / output.
DBG_SWDIO	PF1							Note that this function is enabled to pin out of reset, and has a built-in pull up.
GPIO_EM4WU0	PA0							Pin can be used to wake the system up from EM4
GPIO_EM4WU3	PF1							Pin can be used to wake the system up from EM4

Note:

- 1. Dimensioning & tolerancing confirm to ASME Y14.5M-1994.
- 2. All dimensions are in millimeters. Angles are in degrees.
- 3. Dimension 'b' applies to metallized terminal and is measured between 0.25 mm and 0.30 mm from the terminal tip. Dimension L1 represents terminal full back from package edge up to 0.1 mm is acceptable.
- 4. Coplanarity applies to the exposed heat slug as well as the terminal.
- 5. Radius on terminal is optional

Table 4.4. QFN32 (Dimensions in mm)

Symbol	Α	A1	A 3	b	D	E	D2	E2	е	L	L1	aaa	bbb	ссс	ddd	eee
Min	0.80	0.00		0.25			4.30	4.30		0.30	0.00					
Nom	0.85	-	0.203 REF	0.30	6.00 BSC	6.00 BSC	4.40	4.40	0.65 BSC	0.35		0.10	0.10	0.10	0.05	0.08
Max	0.90	0.05		0.35			4.50	4.50		0.40	0.10					

The QFN32 package uses matte-Sn post plated leadframe.

All EFM32 packages are RoHS compliant and free of Bromine (Br) and Antimony (Sb).

For additional Quality and Environmental information, please see: http://www.silabs.com/support/quality/pages/default.aspx

5 PCB Layout and Soldering

5.1 Recommended PCB Layout

Figure 5.1. QFN32 PCB Land Pattern



Table 5.1. QFN32 PCB Land Pattern Dimensions (Dimensions in mm)

Symbol	Dim. (mm)	Symbol	Pin number	Symbol	Pin number
а	0.80	P1	1	P6	24
b	0.35	P2	8	P7	25
с	0.65	P3	26	P8	32
d	6.00	P4	16	P9	33
e	6.00	P5	17	-	-
f	4.40	-	-	-	-
g	4.40	-	-	-	-



Figure 5.3. QFN32 PCB Stencil Design



Table 5.3. QFN32 PCB Stencil Design Dimensions (Dimensions in mm)

Symbol	Dim. (mm)
a	0.70
b	0.25
С	0.65
d	6.00
e	6.00
x	1.30
у	1.30
Z	0.50

- 1. The drawings are not to scale.
- 2. All dimensions are in millimeters.
- 3. All drawings are subject to change without notice.
- 4. The PCB Land Pattern drawing is in compliance with IPC-7351B.
- 5. Stencil thickness 0.125 mm.
- 6. For detailed pin-positioning, see Figure 4.2 (p. 56).

5.2 Soldering Information

The latest IPC/JEDEC J-STD-020 recommendations for Pb-Free reflow soldering should be followed.

Place as many and as small as possible vias underneath each of the solder patches under the ground pad.

7.4 Revision 0.20

December 11th, 2014

Preliminary Release.

A Disclaimer and Trademarks

A.1 Disclaimer

Silicon Laboratories intends to provide customers with the latest, accurate, and in-depth documentation of all peripherals and modules available for system and software implementers using or intending to use the Silicon Laboratories products. Characterization data, available modules and peripherals, memory sizes and memory addresses refer to each specific device, and "Typical" parameters provided can and do vary in different applications. Application examples described herein are for illustrative purposes only. Silicon Laboratories reserves the right to make changes without further notice and limitation to product information, specifications, and descriptions herein, and does not give warranties as to the accuracy or completeness of the included information. Silicon Laboratories shall have no liability for the consequences of use of the information supplied herein. This document does not imply or express copyright licenses granted hereunder to design or fabricate any integrated circuits. The products must not be used within any Life Support System without the specific written consent of Silicon Laboratories. A "Life Support System" is any product or system intended to support or sustain life and/or health, which, if it fails, can be reasonably expected to result in significant personal injury or death. Silicon Laboratories products are generally not intended for military applications. Silicon Laboratories products shall under no circumstances be used in weapons of mass destruction including (but not limited to) nuclear, biological or chemical weapons, or missiles capable of delivering such weapons.

A.2 Trademark Information

Silicon Laboratories Inc., Silicon Laboratories, Silicon Labs, SiLabs and the Silicon Labs logo, CMEMS®, EFM, EFM32, EFR, Energy Micro, Energy Micro logo and combinations thereof, "the world's most energy friendly microcontrollers", Ember®, EZLink®, EZMac®, EZRadio®, EZRadioPRO®, DSPLL®, ISO-modem®, Precision32®, ProSLIC®, SiPHY®, USBXpress® and others are trademarks or registered trademarks of Silicon Laboratories Inc. ARM, CORTEX, Cortex-M3 and THUMB are trademarks or registered trademarks of ARM Holdings. Keil is a registered trademark of ARM Limited. All other products or brand names mentioned herein are trademarks of their respective holders.