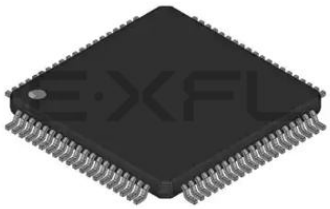
Infineon Technologies - XC2785X104F80LABKXUMA1 Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	C166SV2
Core Size	16/32-Bit
Speed	80MHz
Connectivity	CANbus, EBI/EMI, I²C, LINbus, SPI, SSC, UART/USART, USI
Peripherals	I²S, POR, PWM, WDT
Number of I/O	116
Program Memory Size	832KB (832K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	50K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 24x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP Exposed Pad
Supplier Device Package	PG-LQFP-144-4
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xc2785x104f80labkxuma1

16/32-Bit

Architecture

XC2785X

16/32-Bit Single-Chip Microcontroller with
32-Bit Performance
XC2000 Family / Base Line

Data Sheet

V2.1 2011-07

Microcontrollers

16/32-Bit Single-Chip Microcontroller with 32-Bit Performance

XC2785X (XC2000 Family)

1 Summary of Features

For a quick overview and easy reference, the features of the XC2785X are summarized here.

- High-performance CPU with five-stage pipeline and MPU
  - 12.5 ns instruction cycle at 80 MHz CPU clock (single-cycle execution)
  - One-cycle 32-bit addition and subtraction with 40-bit result
  - One-cycle multiplication (16 × 16 bit)
  - Background division (32 / 16 bit) in 21 cycles
  - One-cycle multiply-and-accumulate (MAC) instructions
  - Enhanced Boolean bit manipulation facilities
  - Zero-cycle jump execution
  - Additional instructions to support HLL and operating systems
  - Register-based design with multiple variable register banks
  - Fast context switching support with two additional local register banks
  - 16 Mbytes total linear address space for code and data
  - 1024 Bytes on-chip special function register area (C166 Family compatible)
  - Integrated Memory Protection Unit (MPU)
- Interrupt system with 16 priority levels for up to 96 sources
  - Selectable external inputs for interrupt generation and wake-up
  - Fastest sample-rate 12.5 ns
- Eight-channel interrupt-driven single-cycle data transfer with Peripheral Event Controller (PEC), 24-bit pointers cover total address space
- Clock generation from internal or external clock sources, using on-chip PLL or prescaler
- Hardware CRC-Checker with Programmable Polynomial to Supervise On-Chip Memory Areas
- On-chip memory modules
  - 8 Kbytes on-chip stand-by RAM (SBRAM)
  - 2 Kbytes on-chip dual-port RAM (DPRAM)
  - Up to 16 Kbytes on-chip data SRAM (DSRAM)
  - Up to 32 Kbytes on-chip program/data SRAM (PSRAM)
  - Up to 832 Kbytes on-chip program memory (Flash memory)
  - Memory content protection through Error Correction Code (ECC)
- On-Chip Peripheral Modules
  - Multi-functional general purpose timer unit with 5 timers
  - 16-channel general purpose capture/compare unit (CAPCOM2)
  - Up to 4 capture/compare units for flexible PWM signal generation (CCU6x)

1.2 Special Device Types

Special device types are only available for high-volume applications on request.

Table 2 Synopsis of XC2785X Special Device Types

Derivative[1)]	Flash Memory[2)]	PSRAM DSRAM[3)]	Capt./Comp. Modules	ADC[4)] Chan.	Interfaces[4)]
XC2785X-72FxxL	576 Kbytes	32 Kbytes 16 Kbytes	CC2 CCU60/1/2/3	16 + 8	2 CAN Nodes, 6 Serial Chan.

1) xx is a placeholder for the available speed grade (in MHz).

2) Specific information about the on-chip Flash memory in **Table 3**.

3) All derivatives additionally provide 8 Kbytes SBRAM and 2 Kbytes DPRAM.

4) Specific information about the available channels in **Table 5**.
Analog input channels are listed for each Analog/Digital Converter module separately (ADC0 + ADC1).

Table 6 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
25	P15.4	I	In/A	**Bit 4 of Port 15, General Purpose Input**
	ADC1_CH4	I	In/A	**Analog Input Channel 4 for ADC1**
	T6INA	I	In/A	**GPT12E Timer T6 Count/Gate Input**
26	P15.5	I	In/A	**Bit 5 of Port 15, General Purpose Input**
	ADC1_CH5	I	In/A	**Analog Input Channel 5 for ADC1**
	T6EUDA	I	In/A	**GPT12E Timer T6 External Up/Down Control Input**
27	P15.6	I	In/A	**Bit 6 of Port 15, General Purpose Input**
	ADC1_CH6	I	In/A	**Analog Input Channel 6 for ADC1**
28	P15.7	I	In/A	**Bit 7 of Port 15, General Purpose Input**
	ADC1_CH7	I	In/A	**Analog Input Channel 7 for ADC1**
29	V_{AREF1}	-	PS/A	**Reference Voltage for A/D Converter ADC1**
30	V_{AREF0}	-	PS/A	**Reference Voltage for A/D Converter ADC0**
31	V_{AGND}	-	PS/A	**Reference Ground for A/D Converters ADC0/1**
32	P5.0	I	In/A	**Bit 0 of Port 5, General Purpose Input**
	ADC0_CH0	I	In/A	**Analog Input Channel 0 for ADC0**
33	P5.1	I	In/A	**Bit 1 of Port 5, General Purpose Input**
	ADC0_CH1	I	In/A	**Analog Input Channel 1 for ADC0**
34	P5.2	I	In/A	**Bit 2 of Port 5, General Purpose Input**
	ADC0_CH2	I	In/A	**Analog Input Channel 2 for ADC0**
	TDI_A	I	In/A	**JTAG Test Data Input**
35	P5.3	I	In/A	**Bit 3 of Port 5, General Purpose Input**
	ADC0_CH3	I	In/A	**Analog Input Channel 3 for ADC0**
	T3INA	I	In/A	**GPT12E Timer T3 Count/Gate Input**

Table 6 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
84	P10.0	O0 / I	St/B	**Bit 0 of Port 10, General Purpose Input/Output**
	U0C1_DOUT	O1	St/B	**USIC0 Channel 1 Shift Data Output**
	CCU60_CC60	O2	St/B	**CCU60 Channel 0 Output**
	AD0	OH / IH	St/B	**External Bus Interface Address/Data Line 0**
	CCU60_CC60INA	I	St/B	**CCU60 Channel 0 Input**
	ESR1_2	I	St/B	**ESR1 Trigger Input 2**
	U0C0_DX0A	I	St/B	**USIC0 Channel 0 Shift Data Input**
	U0C1_DX0A	I	St/B	**USIC0 Channel 1 Shift Data Input**
85	P3.0	O0 / I	St/B	**Bit 0 of Port 3, General Purpose Input/Output**
	U2C0_DOUT	O1	St/B	**USIC2 Channel 0 Shift Data Output**
	$\overline{\text{BREQ}}$	OH	St/B	**External Bus Request Output**
	ESR1_1	I	St/B	**ESR1 Trigger Input 1**
	U2C0_DX0A	I	St/B	**USIC2 Channel 0 Shift Data Input**
	U2C0_DX1A	I	St/B	**USIC2 Channel 0 Shift Clock Input**
86	P10.1	O0 / I	St/B	**Bit 1 of Port 10, General Purpose Input/Output**
	U0C0_DOUT	O1	St/B	**USIC0 Channel 0 Shift Data Output**
	CCU60_CC61	O2	St/B	**CCU60 Channel 1 Output**
	AD1	OH / IH	St/B	**External Bus Interface Address/Data Line 1**
	CCU60_CC61INA	I	St/B	**CCU60 Channel 1 Input**
	U0C0_DX1A	I	St/B	**USIC0 Channel 0 Shift Clock Input**
	U0C0_DX0B	I	St/B	**USIC0 Channel 0 Shift Data Input**

Table 6 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
120	P1.2	O0 / I	St/B	**Bit 2 of Port 1, General Purpose Input/Output**
	CCU62_CC62	O1	St/B	**CCU62 Channel 2 Output**
	U1C0_SELO6	O2	St/B	**USIC1 Channel 0 Select/Control 6 Output**
	U2C1_SCLKOUT	O3	St/B	**USIC2 Channel 1 Shift Clock Output**
	A10	OH	St/B	**External Bus Interface Address Line 10**
	ESR1_4	I	St/B	**ESR1 Trigger Input 4**
	CCU61_T12HRB	I	St/B	**External Run Control Input for T12 of CCU61**
	CCU62_CC62INA	I	St/B	**CCU62 Channel 2 Input**
	U2C1_DX0D	I	St/B	**USIC2 Channel 1 Shift Data Input**
	U2C1_DX1C	I	St/B	**USIC2 Channel 1 Shift Clock Input**
121	P10.12	O0 / I	St/B	**Bit 12 of Port 10, General Purpose Input/Output**
	U1C0_DOUT	O1	St/B	**USIC1 Channel 0 Shift Data Output**
	TDO_B	OH / IH	St/B	**JTAG Test Data Output / DAP1 Input/Output** If DAP pos. 1 is selected during start-up, an internal pull-down device will hold this pin low when nothing is driving it.
	AD12	OH / IH	St/B	**External Bus Interface Address/Data Line 12**
	U1C0_DX0C	I	St/B	**USIC1 Channel 0 Shift Data Input**
	U1C0_DX1E	I	St/B	**USIC1 Channel 0 Shift Clock Input**
122	P9.3	O0 / I	St/B	**Bit 3 of Port 9, General Purpose Input/Output**
	CCU63_COUT60	O1	St/B	**CCU63 Channel 0 Output**
	$\overline{\text{BRKOUT}}$	O2	St/B	**OCDS Break Signal Output**

Table 6 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
123	P10.13	O0 / I	St/B	**Bit 13 of Port 10, General Purpose Input/Output**
	U1C0_DOUT	O1	St/B	**USIC1 Channel 0 Shift Data Output**
	U1C0_SELO 3	O3	St/B	**USIC1 Channel 0 Select/Control 3 Output**
	$\overline{WR}$/$\overline{WRL}$	OH	St/B	**External Bus Interface Write Strobe Output** Active for each external write access, when $\overline{WR}$, active for ext. writes to the low byte, when $\overline{WRL}$.
	U1C0_DX0D	I	St/B	**USIC1 Channel 0 Shift Data Input**
124	P1.3	O0 / I	St/B	**Bit 3 of Port 1, General Purpose Input/Output**
	CCU62_COU T63	O1	St/B	**CCU62 Channel 3 Output**
	U1C0_SELO 7	O2	St/B	**USIC1 Channel 0 Select/Control 7 Output**
	U2C0_SELO 4	O3	St/B	**USIC2 Channel 0 Select/Control 4 Output**
	A11	OH	St/B	**External Bus Interface Address Line 11**
	ESR2_4	I	St/B	**ESR2 Trigger Input 4**
	CCU62_T12 HRB	I	St/B	**External Run Control Input for T12 of CCU62**
125	P9.4	O0 / I	St/B	**Bit 4 of Port 9, General Purpose Input/Output**
	CCU63_COU T61	O1	St/B	**CCU63 Channel 1 Output**
	U2C0_DOUT	O2	St/B	**USIC2 Channel 0 Shift Data Output**
	CCU62_COU T63	O3	St/B	**CCU62 Channel 3 Output**

3.1 Memory Subsystem and Organization

The memory space of the XC2785X is configured in the von Neumann architecture. In this architecture all internal and external resources, including code memory, data memory, registers and I/O ports, are organized in the same linear address space.

Table 8 XC2785X Memory Map [1)]

Address Area	Start Loc.	End Loc.	Area Size[2)]	Notes
IMB register space	$FF'FF00_H$	$FF'FFFF_H$	256 Bytes	–
Reserved (Access trap)	$F0'0000_H$	$FF'FEFF_H$	<1 Mbyte	Minus IMB registers
Reserved for EPSRAM	$E8'8000_H$	$EF'FFFF_H$	480 Kbytes	Mirrors EPSRAM
Emulated PSRAM	$E8'0000_H$	$E8'7FFF_H$	32 Kbytes	With Flash timing
Reserved for PSRAM	$E0'8000_H$	$E7'FFFF_H$	480 Kbytes	Mirrors PSRAM
Program SRAM	$E0'0000_H$	$E0'7FFF_H$	32 Kbytes	Maximum speed
Reserved for Flash	$CD'0000_H$	$DF'FFFF_H$	<1.25 Mbytes	–
Program Flash 3	$CC'0000_H$	$CC'FFFF_H$	64 Kbytes	–
Program Flash 2	$C8'0000_H$	$CB'FFFF_H$	256 Kbytes	–
Program Flash 1	$C4'0000_H$	$C7'FFFF_H$	256 Kbytes	–
Program Flash 0	$C0'0000_H$	$C3'FFFF_H$	256 Kbytes	[3)]
External memory area	$40'0000_H$	$BF'FFFF_H$	8 Mbytes	–
Available Ext. IO area[4)]	$21'0000_H$	$3F'FFFF_H$	< 2 Mbytes	Minus USIC/CAN
Reserved	$20'BC00_H$	$20'FFFF_H$	17 Kbytes	–
USIC alternate regs.	$20'B000_H$	$20'BFFF_H$	4 Kbytes	Accessed via EBC
MultiCAN alternate regs.	$20'8000_H$	$20'AFFF_H$	12 Kbytes	Accessed via EBC
Reserved	$20'6000_H$	$20'7FFF_H$	8 Kbytes	–
USIC registers	$20'4000_H$	$20'5FFF_H$	8 Kbytes	Accessed via EBC
MultiCAN registers	$20'0000_H$	$20'3FFF_H$	16 Kbytes	Accessed via EBC
External memory area	$01'0000_H$	$1F'FFFF_H$	< 2 Mbytes	Minus segment 0
SFR area	$00'FE00_H$	$00'FFFF_H$	0.5 Kbyte	–
Dual-Port RAM	$00'F600_H$	$00'FDFF_H$	2 Kbytes	–
Reserved for DPRAM	$00'F200_H$	$00'F5FF_H$	1 Kbyte	–
ESFR area	$00'F000_H$	$00'F1FF_H$	0.5 Kbyte	–
XSFR area	$00'E000_H$	$00'EFFF_H$	4 Kbytes	–

3.2 External Bus Controller

All external memory access operations are performed by a special on-chip External Bus Controller (EBC). The EBC also controls access to resources connected to the on-chip LXBus (MultiCAN and the USIC modules). The LXBus is an internal representation of the external bus that allows access to integrated peripherals and modules in the same way as to external components.

The EBC can be programmed either to Single Chip Mode, when no external memory is required, or to an external bus mode with the following selections[1]:

- Address Bus Width with a range of 0 … 24-bit
- Data Bus Width 8-bit or 16-bit
- Bus Operation Multiplexed or Demultiplexed

The bus interface uses Port 10 and Port 2 for addresses and data. In the demultiplexed bus modes, the lower addresses are output separately on Port 0 and Port 1. The number of active segment address lines is selectable, restricting the external address space to 8 Mbytes … 64 Kbytes. This is required when interface lines shall be assigned to Port 2.

External $\overline{CS}$ signals (address windows plus default) can be generated and output on Port 4 in order to save external glue logic. External modules can be directly connected to the common address/data bus and their individual select lines.

A $\overline{HOLD}$/$\overline{HLDA}$ protocol is available for bus arbitration; this allows the sharing of external resources with other bus masters. The bus arbitration is enabled by software, after which pins P3.0 … P3.2 ($\overline{BREQ}$, $\overline{HLDA}$, $\overline{HOLD}$) are automatically controlled by the EBC. In Master Mode (default after reset) the $\overline{HLDA}$ pin is an output. In Slave Mode pin $\overline{HLDA}$ is switched to be an input. This allows the direct connection of the slave controller to another master controller without glue logic.

Important timing characteristics of the external bus interface are programmable (with registers TCONCSx/FCONCSx) to allow the user to adapt it to a wide range of different types of memories and external peripherals.
Access to very slow memories or modules with varying access times is supported by a special ‘Ready’ function. The active level of the control input signal is selectable.

In addition, up to four independent address windows may be defined (using registers ADDRSELx) to control access to resources with different bus characteristics. These address windows are arranged hierarchically where window 4 overrides window 3, and window 2 overrides window 1. All accesses to locations not covered by these four address windows are controlled by TCONCS0/FCONCS0. The currently active window can generate a chip select signal.

The external bus timing is based on the rising edge of the reference clock output CLKOUT. The external bus protocol is compatible with that of the standard C166 Family.

1) Bus modes are switched dynamically if several address windows with different mode settings are used.

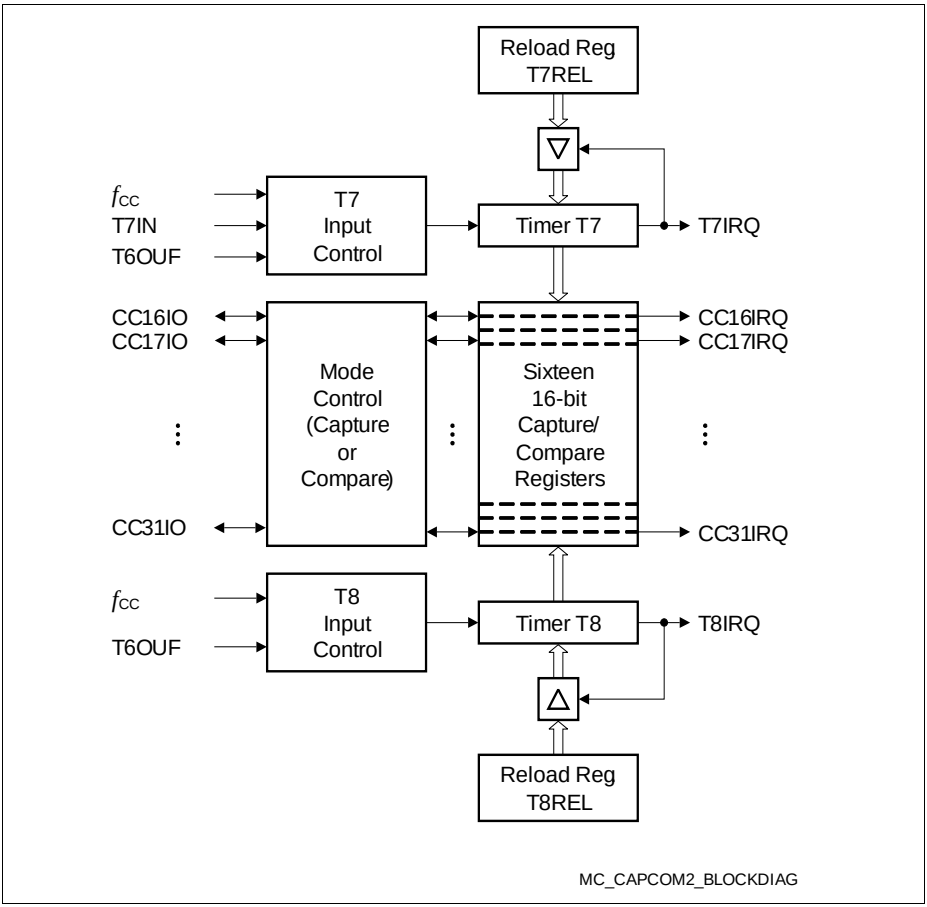

Figure 6 CAPCOM2 Unit Block Diagram

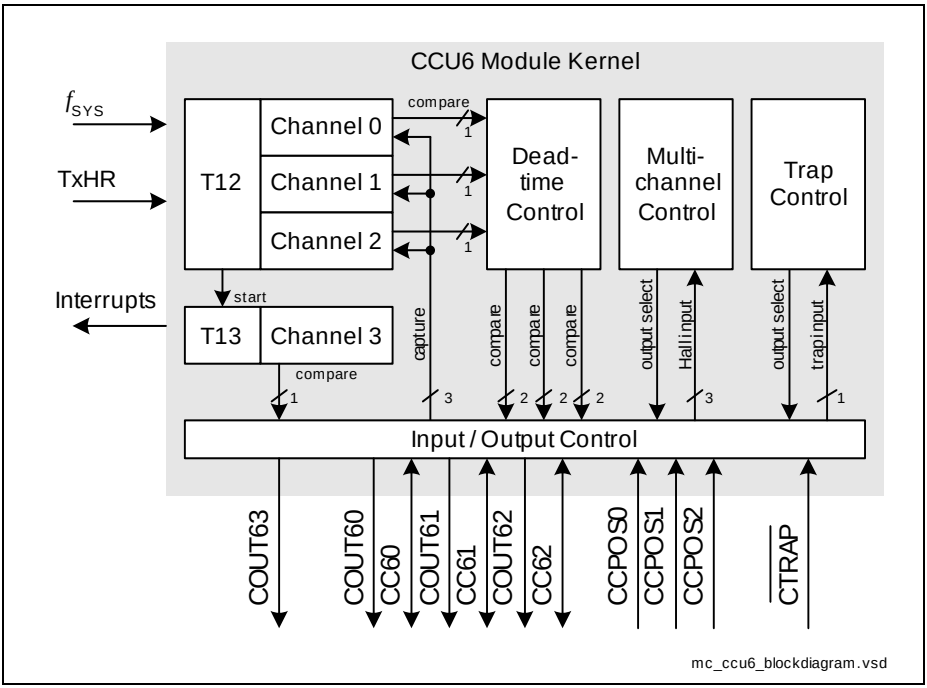

Figure 7 CCU6 Block Diagram

Timer T12 can work in capture and/or compare mode for its three channels. The modes can also be combined. Timer T13 can work in compare mode only. The multi-channel control unit generates output patterns that can be modulated by timer T12 and/or timer T13. The modulation sources can be selected and combined for signal modulation.

3.10 General Purpose Timer (GPT12E) Unit

The GPT12E unit is a very flexible multifunctional timer/counter structure which can be used for many different timing tasks such as event timing and counting, pulse width and duty cycle measurements, pulse generation, or pulse multiplication.

The GPT12E unit incorporates five 16-bit timers organized in two separate modules, GPT1 and GPT2. Each timer in each module may either operate independently in a number of different modes or be concatenated with another timer of the same module.

Each of the three timers T2, T3, T4 of **module GPT1** can be configured individually for one of four basic modes of operation: Timer, Gated Timer, Counter, and Incremental Interface Mode. In Timer Mode, the input clock for a timer is derived from the system clock and divided by a programmable prescaler. Counter Mode allows timer clocking in reference to external events.

Pulse width or duty cycle measurement is supported in Gated Timer Mode, where the operation of a timer is controlled by the ‘gate’ level on an external input pin. For these purposes each timer has one associated port pin (TxIN) which serves as a gate or clock input. The maximum resolution of the timers in module GPT1 is 4 system clock cycles.

The counting direction (up/down) for each timer can be programmed by software or altered dynamically by an external signal on a port pin (TxEUD), e.g. to facilitate position tracking.

In Incremental Interface Mode the GPT1 timers can be directly connected to the incremental position sensor signals A and B through their respective inputs TxIN and TxEUD. Direction and counting signals are internally derived from these two input signals, so that the contents of the respective timer Tx corresponds to the sensor position. The third position sensor signal TOP0 can be connected to an interrupt input.

Timer T3 has an output toggle latch (T3OTL) which changes its state on each timer overflow/underflow. The state of this latch may be output on pin T3OUT e.g. for time out monitoring of external hardware components. It may also be used internally to clock timers T2 and T4 for measuring long time periods with high resolution.

In addition to the basic operating modes, T2 and T4 may be configured as reload or capture register for timer T3. A timer used as capture or reload register is stopped. The contents of timer T3 is captured into T2 or T4 in response to a signal at the associated input pin (TxIN). Timer T3 is reloaded with the contents of T2 or T4, triggered either by an external signal or a selectable state transition of its toggle latch T3OTL. When both T2 and T4 are configured to alternately reload T3 on opposite state transitions of T3OTL with the low and high times of a PWM signal, this signal can be continuously generated without software intervention.

With its maximum resolution of 2 system clock cycles, the **GPT2 module** provides precise event control and time measurement. It includes two timers (T5, T6) and a capture/reload register (CAPREL). Both timers can be clocked with an input clock which is derived from the CPU clock via a programmable prescaler or with external signals. The counting direction (up/down) for each timer can be programmed by software or altered dynamically with an external signal on a port pin (TxEUD). Concatenation of the timers is supported with the output toggle latch (T6OTL) of timer T6, which changes its state on each timer overflow/underflow.

The state of this latch may be used to clock timer T5, and/or it may be output on pin T6OUT. The overflows/underflows of timer T6 can also be used to clock the CAPCOM2 timers and to initiate a reload from the CAPREL register.

The CAPREL register can capture the contents of timer T5 based on an external signal transition on the corresponding port pin (CAPIN); timer T5 may optionally be cleared after the capture procedure. This allows the XC2785X to measure absolute time differences or to perform pulse multiplication without software overhead.

The capture trigger (timer T5 to CAPREL) can also be generated upon transitions of GPT1 timer T3 inputs T3IN and/or T3EUD. This is especially advantageous when T3 operates in Incremental Interface Mode.

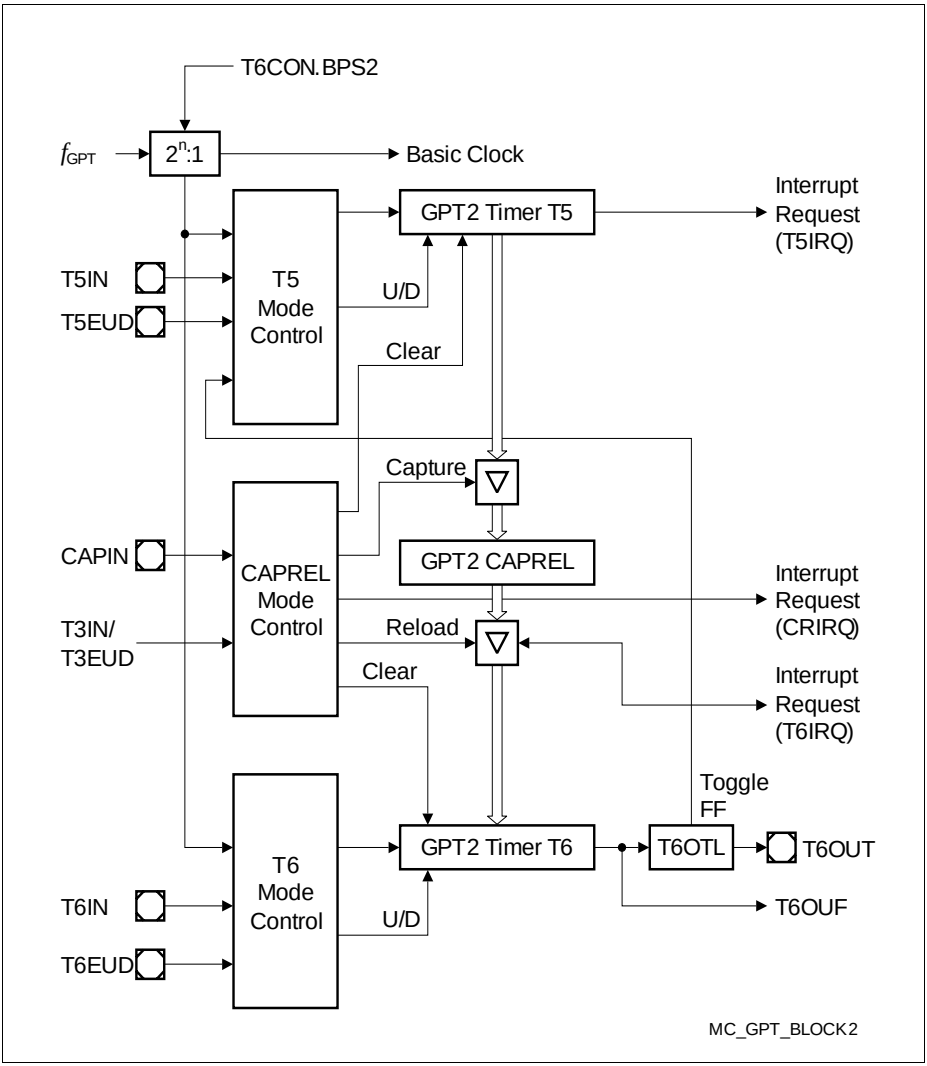

Figure 9 Block Diagram of GPT2

3.11 Real Time Clock

The Real Time Clock (RTC) module of the XC2785X can be clocked with a clock signal selected from internal sources or external sources (pins).

The RTC basically consists of a chain of divider blocks:

- Selectable 32:1 and 8:1 dividers (on - off)
- The reloadable 16-bit timer T14
- The 32-bit RTC timer block (accessible via registers RTCH and RTCL) consisting of:
  - a reloadable 10-bit timer
  - a reloadable 6-bit timer
  - a reloadable 6-bit timer
  - a reloadable 10-bit timer

All timers count up. Each timer can generate an interrupt request. All requests are combined to a common node request.

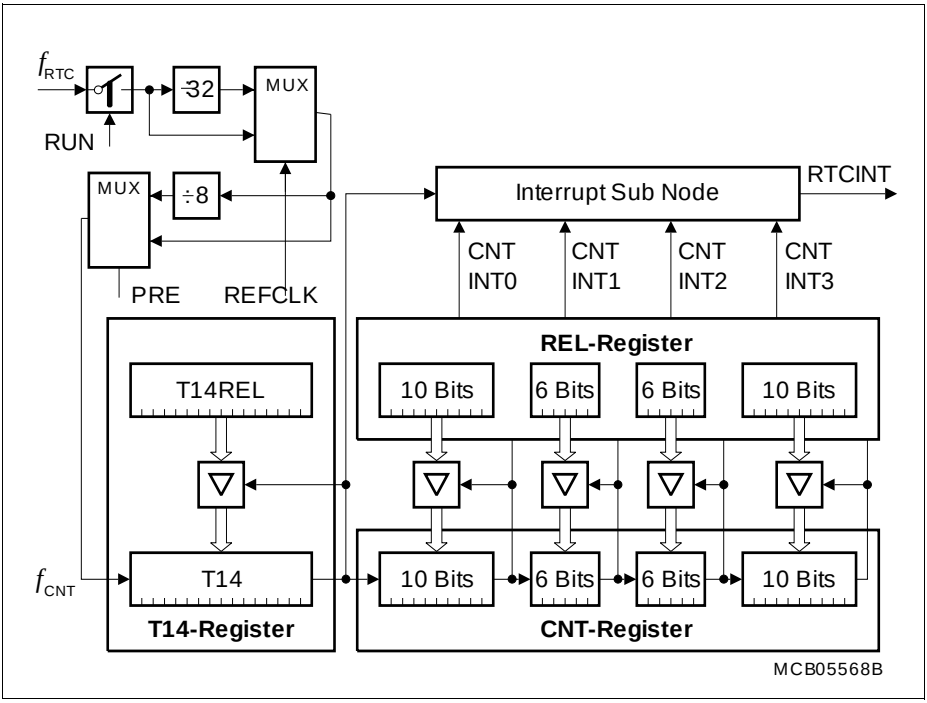

Figure 10 RTC Block Diagram

Note: The registers associated with the RTC are only affected by a power reset.

3.12 A/D Converters

For analog signal measurement, up to two 10-bit A/D converters (ADC0, ADC1) with 16 + 8 multiplexed input channels and a sample and hold circuit have been integrated on-chip. 4 inputs can be converted by both A/D converters. Conversions use the successive approximation method. The sample time (to charge the capacitors) and the conversion time are programmable so that they can be adjusted to the external circuit. The A/D converters can also operate in 8-bit conversion mode, further reducing the conversion time.

Several independent conversion result registers, selectable interrupt requests, and highly flexible conversion sequences provide a high degree of programmability to meet the application requirements. Both modules can be synchronized to allow parallel sampling of two input channels.

For applications that require more analog input channels, external analog multiplexers can be controlled automatically. For applications that require fewer analog input channels, the remaining channel inputs can be used as digital input port pins.

The A/D converters of the XC2785X support two types of request sources which can be triggered by several internal and external events.

- Parallel requests are activated at the same time and then executed in a predefined sequence.
- Queued requests are executed in a user-defined sequence.

In addition, the conversion of a specific channel can be inserted into a running sequence without disturbing that sequence. All requests are arbitrated according to the priority level assigned to them.

Data reduction features reduce the number of required CPU access operations allowing the precise evaluation of analog inputs (high conversion rate) even at a low CPU speed. Result data can be reduced by limit checking or accumulation of results.

The Peripheral Event Controller (PEC) can be used to control the A/D converters or to automatically store conversion results to a table in memory for later evaluation, without requiring the overhead of entering and exiting interrupt routines for each data transfer. Each A/D converter contains eight result registers which can be concatenated to build a result FIFO. Wait-for-read mode can be enabled for each result register to prevent the loss of conversion data.

In order to decouple analog inputs from digital noise and to avoid input trigger noise, those pins used for analog input can be disconnected from the digital input stages. This can be selected for each pin separately with the Port x Digital Input Disable registers.

The Auto-Power-Down feature of the A/D converters minimizes the power consumption when no conversion is in progress.

Broken wire detection for each channel and a multiplexer test mode provide information to verify the proper operation of the analog signal sources (e.g. a sensor system).

Table 11 Instruction Set Summary (cont'd)

Mnemonic	Description	Bytes
ROL/ROR	Rotate left/right direct word GPR	2
ASHR	Arithmetic (sign bit) shift right direct word GPR	2
MOV(B)	Move word (byte) data	2 / 4
MOVBS/Z	Move byte operand to word op. with sign/zero extension	2 / 4
JMPA/I/R	Jump absolute/indirect/relative if condition is met	4
JMPS	Jump absolute to a code segment	4
JB(C)	Jump relative if direct bit is set (and clear bit)	4
JNB(S)	Jump relative if direct bit is not set (and set bit)	4
CALLA/I/R	Call absolute/indirect/relative subroutine if condition is met	4
CALLS	Call absolute subroutine in any code segment	4
PCALL	Push direct word register onto system stack and call absolute subroutine	4
TRAP	Call interrupt service routine via immediate trap number	2
PUSH/POP	Push/pop direct word register onto/from system stack	2
SCXT	Push direct word register onto system stack and update register with word operand	4
RET(P)	Return from intra-segment subroutine (and pop direct word register from system stack)	2
RETS	Return from inter-segment subroutine	2
RETI	Return from interrupt service subroutine	2
SBRK	Software Break	2
SRST	Software Reset	4
IDLE	Enter Idle Mode	4
PWRDN	Unused instruction[1)]	4
SRVWDT	Service Watchdog Timer	4
DISWDT/ENWDT	Disable/Enable Watchdog Timer	4
EINIT	End-of-Initialization Register Lock	4
ATOMIC	Begin ATOMIC sequence	2
EXTR	Begin EXTended Register sequence	2
EXTP(R)	Begin EXTended Page (and Register) sequence	2 / 4
EXTS(R)	Begin EXTended Segment (and Register) sequence	2 / 4

4 Electrical Parameters

The operating range for the XC2785X is defined by its electrical parameters. For proper operation the specified limits must be respected when integrating the device in its target environment.

4.1 General Parameters

These parameters are valid for all subsequent descriptions, unless otherwise noted.

4.1.1 Absolut Maximum Rating Conditions

Stresses above the values listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for an extended time may affect device reliability.
During absolute maximum rating overload conditions ($V_{IN} > V_{DDP}$ or $V_{IN} < V_{SS}$) the voltage on V_{DDP} pins with respect to ground (V_{SS}) must not exceed the values defined by the absolute maximum ratings.

Table 12 Absolute Maximum Rating Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Output current on a pin when high value is driven	I_{OH} SR	-30	–	–	mA	
Output current on a pin when low value is driven	I_{OL} SR	–	–	30	mA	
Overload current	I_{OV} SR	-10	–	10	mA	1)
Absolute sum of overload currents	$\Sigma\lvert I_{OV}\rvert$ SR	–	–	100	mA	1)
Junction Temperature	T_J SR	-40	–	150	°C	
Storage Temperature	T_{ST} SR	-65	–	150	°C	
Digital supply voltage for IO pads and voltage regulators	V_{DDPA}, V_{DDPB} SR	-0.5	–	6.0	V	
Voltage on any pin with respect to ground (Vss)	V_{IN} SR	-0.5	–	V_{DDP} + 0.5	V	$V_{IN} \le V_{DDP(max)}$

1) Overload condition occurs if the input voltage V_{IN} is out of the absolute maximum rating range. In this case the current must be limited to the listed values by design measures.

Table 26 is valid under the following conditions:
$V_{DDP} \geq 4.5$ V; $V_{DDPtyp} = 5$ V; $V_{DDP} \leq 5.5$ V; $C_L \geq 20$ pF; $C_L \leq 100$ pF;

Table 26 Standard Pad Parameters for Upper Voltage Range

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Maximum output driver current (absolute value)[1]	I_{Omax} CC	–	–	10	mA	Strong driver
		–	–	4.0	mA	Medium driver
		–	–	0.5	mA	Weak driver
Nominal output driver current (absolute value)	I_{Onom} CC	–	–	2.5	mA	Strong driver
		–	–	1.0	mA	Medium driver
		–	–	0.1	mA	Weak driver
Rise and Fall times (10% - 90%)	t_{RF} CC	–	–	4.2 + 0.14 x C_L	ns	Strong driver; Sharp edge
		–	–	11.6 + 0.22 x C_L	ns	Strong driver; Medium edge
		–	–	20.6 + 0.22 x C_L	ns	Strong driver; Slow edge
		–	–	23 + 0.6 x C_L	ns	Medium driver
		–	–	212 + 1.9 x C_L	ns	Weak driver

1) The total output current that may be drawn at a given time must be limited to protect the supply rails from damage. For any group of 16 neighboring output pins, the total output current in each direction (ΣI_{OL} and ΣI_{OH}) must remain below 50 mA.

4.6.5 External Bus Timing

The following parameters specify the behavior of the XC2785X bus interface.

Note: These parameters are not subject to production test but verified by design and/or characterization.

Note: Operating Conditions apply.

Bus Interface Performance Limits

The output frequency at the bus interface pins is limited by the performance of the output drivers. The fast clock driver (used for CLKOUT) can drive 80-MHz signals, the standard drivers can drive 40-MHz signals
Therefore, the speed of the EBC must be limited, either by limiting the system frequency to $f_{SYS} \leq 80$ MHz or by adding waitstates so that signal transitions have a minimum distance of 12.5 ns.
For a description of the bus protocol and the programming of its variable timing parameters, please refer to the User's Manual.

Table 28 EBC Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
CLKOUT Cycle Time[1)]	t_5 CC	–	1 / f_{SYS}	–	ns	
CLKOUT high time	t_6 CC	2	–	–		
CLKOUT low time	t_7 CC	2	–	–		
CLKOUT rise time	t_8 CC	–	–	3	ns	
CLKOUT fall time	t_9 CC	–	–	3		

1) The CLKOUT cycle time is influenced by PLL jitter. For longer periods the relative deviation decreases (see PLL deviation formula).

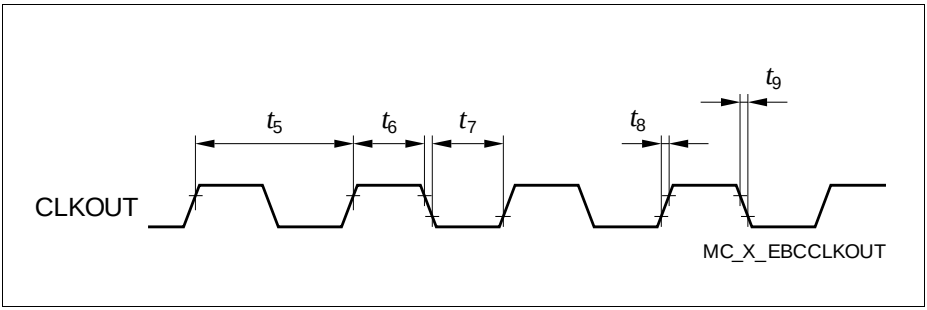

Figure 22 CLKOUT Signal Timing