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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	Z8S180
Number of Cores/Bus Width	1 Core, 8-Bit
Speed	20MHz
Co-Processors/DSP	-
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	5.0V
Operating Temperature	0°C ~ 70°C (TA)
Security Features	-
Package / Case	100-QFP
Supplier Device Package	100-QFP
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8019520fsc

GENERAL DESCRIPTION (Continued)

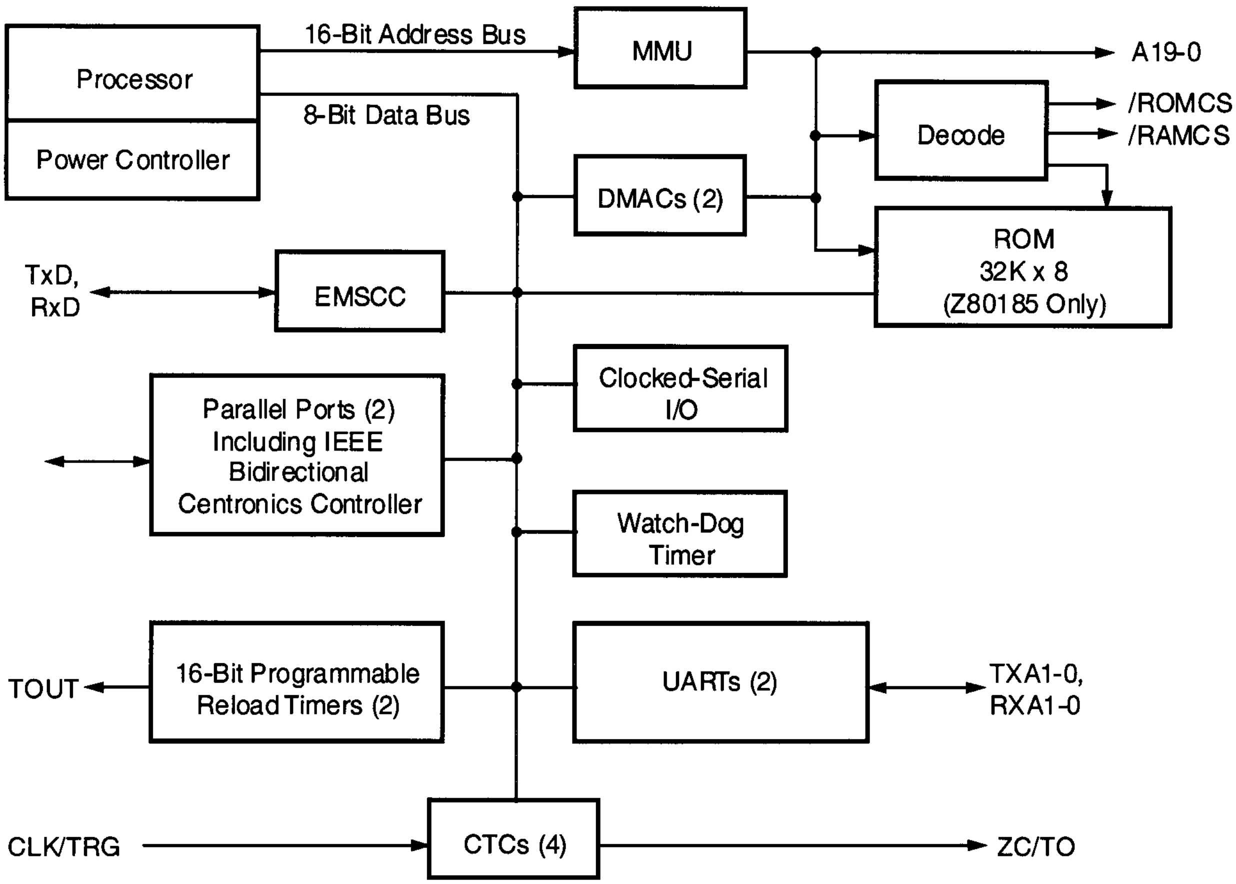

Figure 1. Z80185/195 Functional Block Diagram

PIN DESCRIPTION

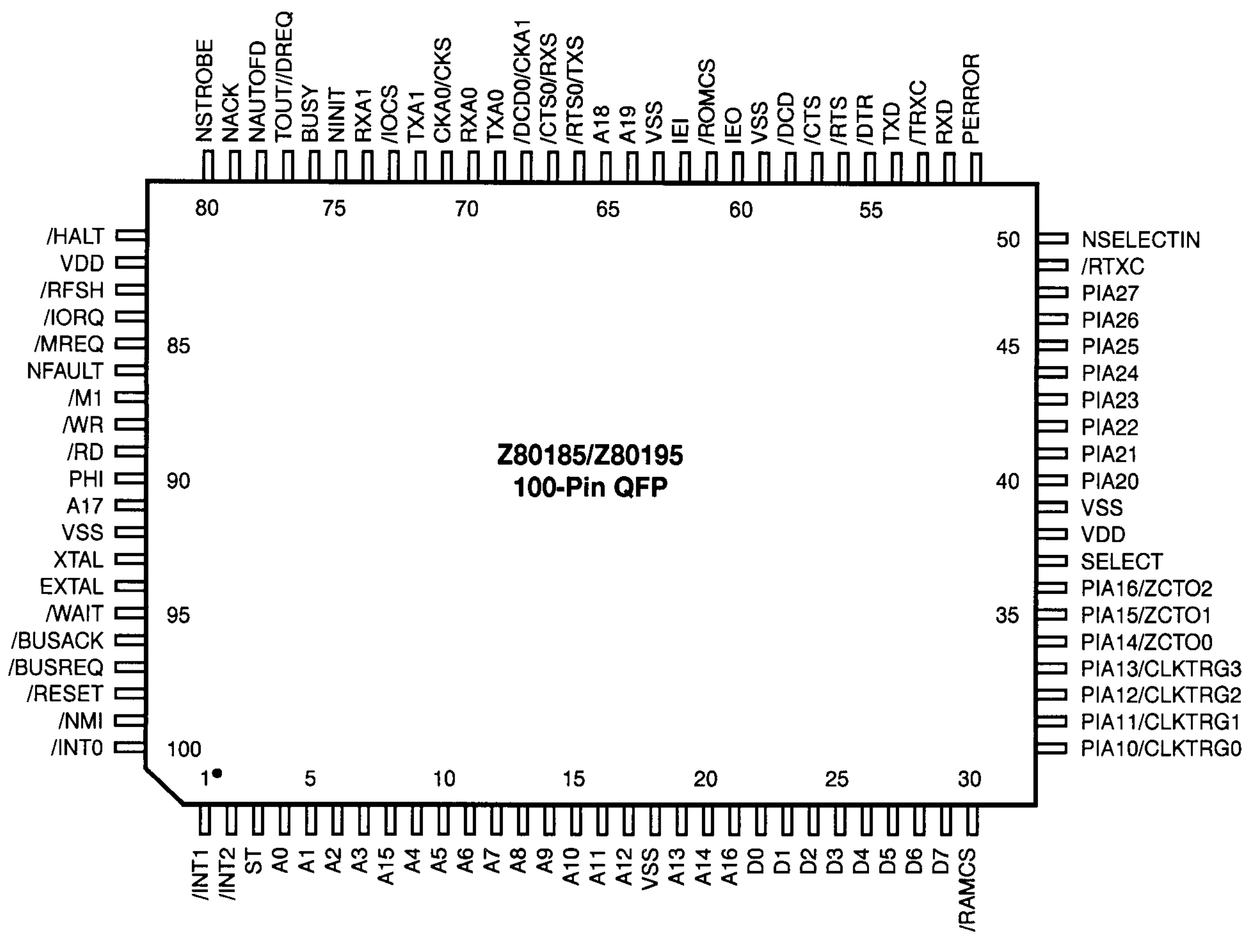

Figure 2. 100-Pin QFP Pin Assignments

Z80185 CTC, AND MISCELLANEOUS REGISTERS (Continued)

Interrupt Edge Register

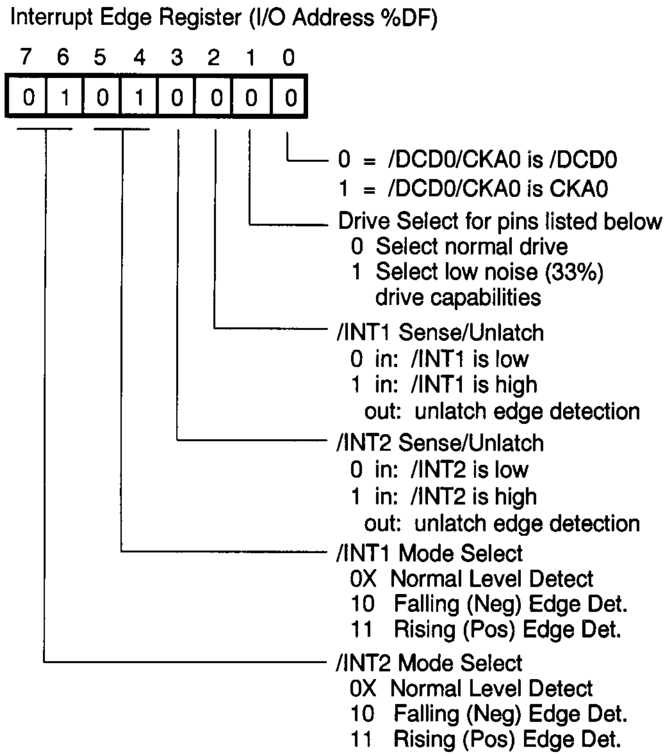

Figure 87. Interrupt Edge Register
(I/O Address %DF)

Bits 7-6. These bits control the interrupt capture logic for the /INT2 pin. When these bits are 0X, the /INT2 pin is level sensitive and Low active. When these bits are 10, negative edge detection is enabled. Any falling edge will latch an active Low on the internal /INT2 to the processor. This interrupt must be cleared by writing a 1 to bit 3 of this register. Programming these bits to 11 enables rising edge interrupts to be latched. The latch must be cleared in the same fashion as for a falling edge.

Bits 5-4. These bits control the interrupt capture logic for the external /INT1 pin. When these bits are 0X, the /INT1 pin is level sensitive and Low active. When these bits are 10, negative edge detection is enabled. Any falling edge will latch an active Low on the internal /INT1 to the processor. This interrupt must be cleared by writing a 1 to bit 2 of this register. Programming these bits to 11 enables rising edge interrupts to be latched. The latch must be cleared in the same fashion as for a falling edge.

Bit 3. Software can read this register to sense the state of the /INT2 pin. Writing a 1 to this bit clears the edge detection logic for /INT2.

Bit 2. Software can read this register to sense the state of the /INT1 pin. Writing a 1 to this bit clears the edge detection logic for /INT1.

Bit 1. This bit selects low noise or normal drive for the parallel ports, bidirectional Centronics controller pins, Chip Select pins, and EMSCC pins as follows:

PIA 10-13	/RTS	nFault
PIA 14-16/ZCTO 0-2	/DTR	nInit
PIA 27-20	TXD	nSelectIn
/ROMCS	/TRXC	nStrobe
/RAMCS	BUSY	PError
/IOCS	nAck	Select
IEO	nAutoFd	

A 1 in this bit selects the low noise option, which is a 33 percent reduction in drive capability. A 0 selects normal drive, and is the default after power-up. Additionally, refer to CPU Register (CCR) for a list of the pins that are programmable for low drive, via the CCR register.

Bit 0. If this bit is 1, the /DCD0/CKA1 pin has the CKA1 function. The pin is always connected to the DCD input of ASCI0, so if this pin is 1, and ASCI0 is used, it should not be programmed to use DCD as a receive auto-enable.

ELECTRICAL CHARACTERISTICS (Continued)

The following table shows the characteristics of each pin in terms of the above classifications. A dash "–" in the input or output column indicates the pin does not have that function.

Table 9. Pin Classification Characteristics

Pin	Input Class	Output Class
/BUSREQ	I	–
/CTS	I	–
/CTS0/RxS	I	–
/DCD	I	–
/DCD0/CKA1	I	3
/DTR	–	O
/HALT	–	O
/INT0	I	D
/INT1	I	–
/INT2	I	–
/IOCS	–	O
/IORQ	I	3
/M1	I	3
/MREQ	I	3
/NMI	R	–
/RAMCS	–	O
/RD	I	3
/RESET	R	D
/RFSH	–	O
/ROMCS	–	O
/RTS	–	O
/RTS0/TxS	–	O
/RTXC	I	3
/TRXC	I	3
/WAIT	I	D
/WR	I	3
A0-A19	I	3

Pin	Input Class	Output Class
Busy	S	T
CKA0/CKS	I	3
D0-D7	I	3
EXTAL	R	–
IEI	I	–
IEO	–	O
nAck	S	T
nAutoFd	S	T
nFault	S	T
nInit	S	T
nSelectIn	S	T
nStrobe	S	T
PError	S	T
PHI	–	H
PIA13-10/CLKTRG3-0	I	3
PIA15-13/ZCTO2-0	I	3
PIA27-20	S	T
RXA0	I	–
RXA1	I	–
RXD	I	–
/ST	–	O
Select	S	T
TOUT//DREQ	I	O
TXA0	–	O
TXA1	–	O
TXD	–	O
XTAL	–	O