Zilog - Z8019533FSG Datasheet

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	Z8S180
Number of Cores/Bus Width	1 Core, 8-Bit
Speed	33MHz
Co-Processors/DSP	-
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	5.0V
Operating Temperature	0°C ~ 70°C (TA)
Security Features	-
Package / Case	100-QFP
Supplier Device Package	100-QFP
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8019533fsg

GENERAL DESCRIPTION (Continued)

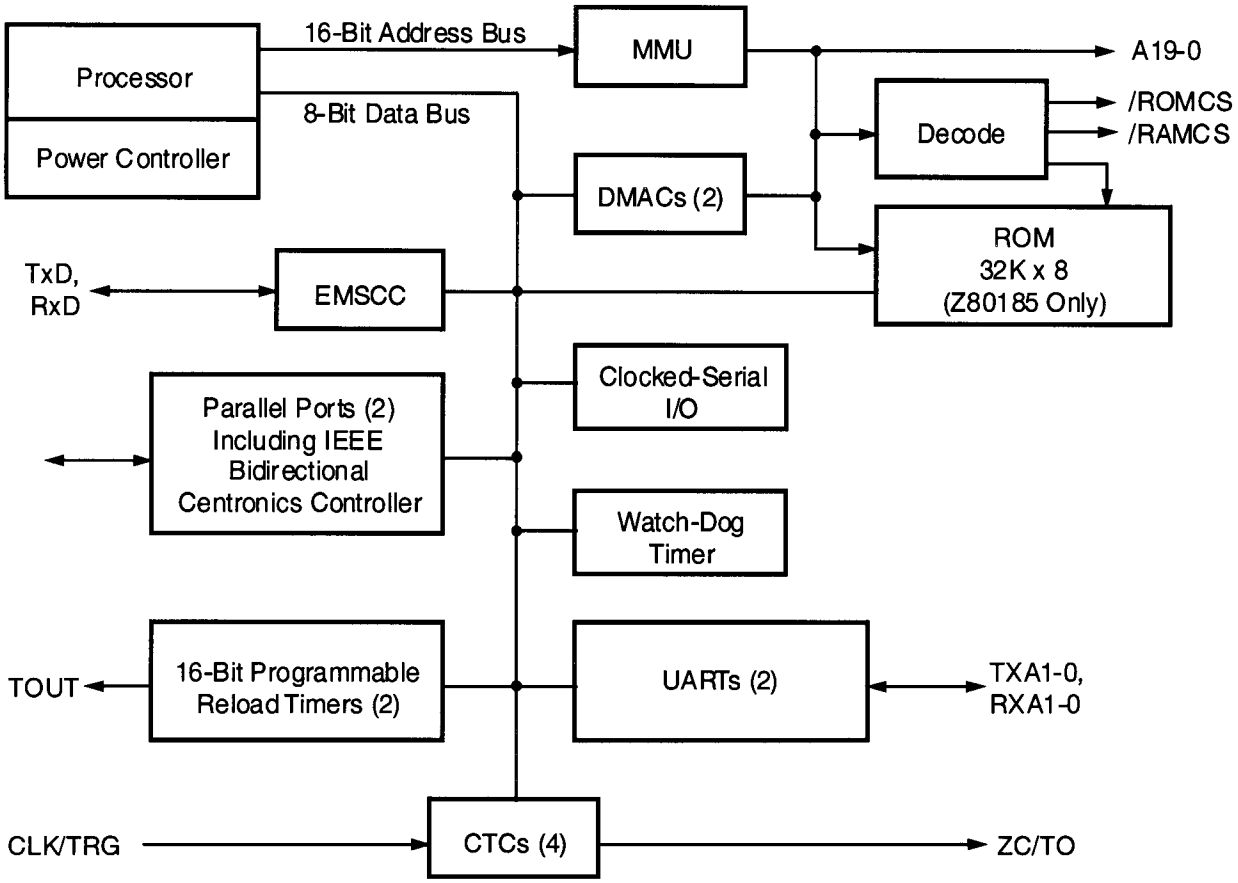


Figure 1. Z80185/195 Functional Block Diagram

PIN DESCRIPTION

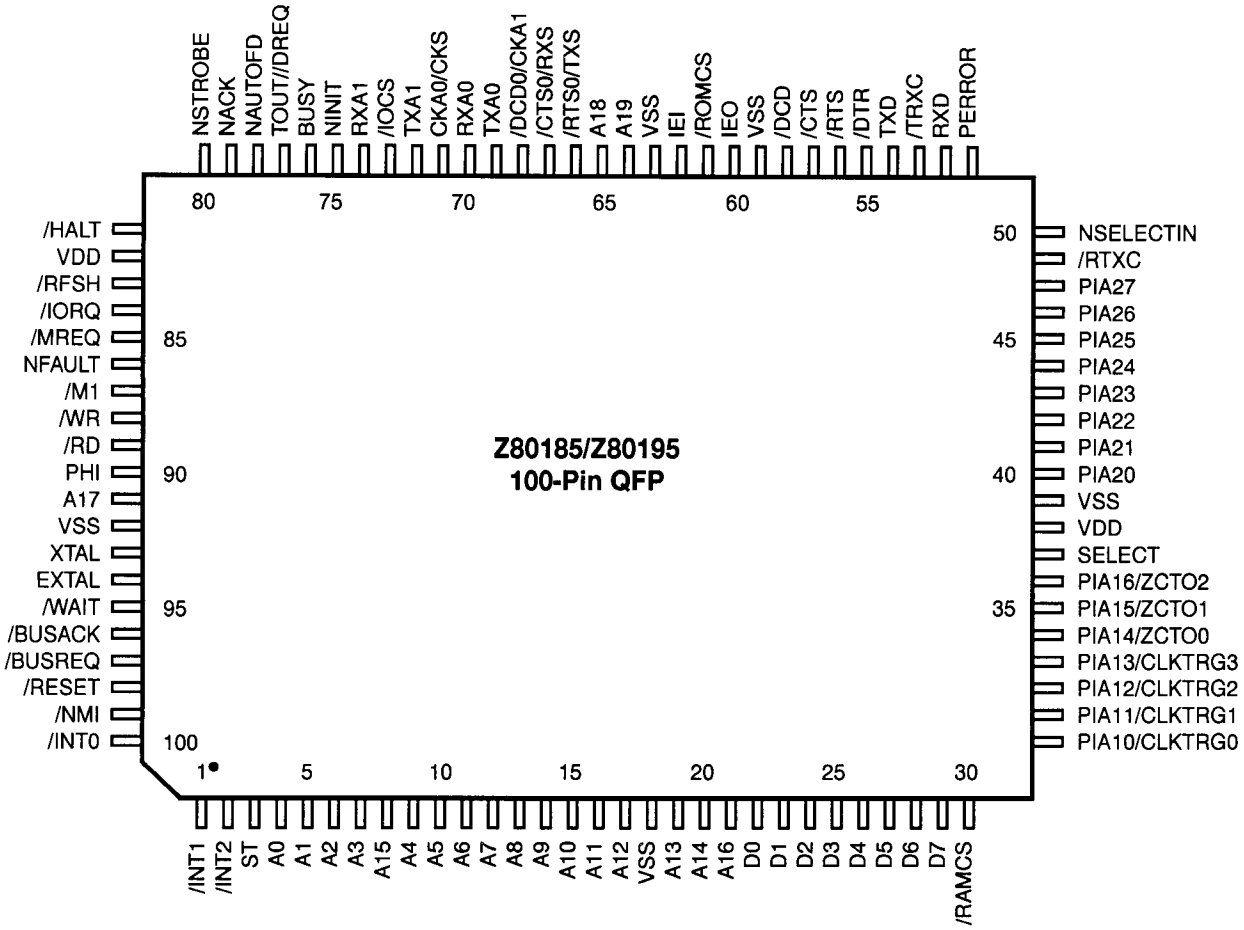


Figure 2. 100-Pin QFP Pin Assignments

TIMING DIAGRAMS

Z8S180 MPU Timing

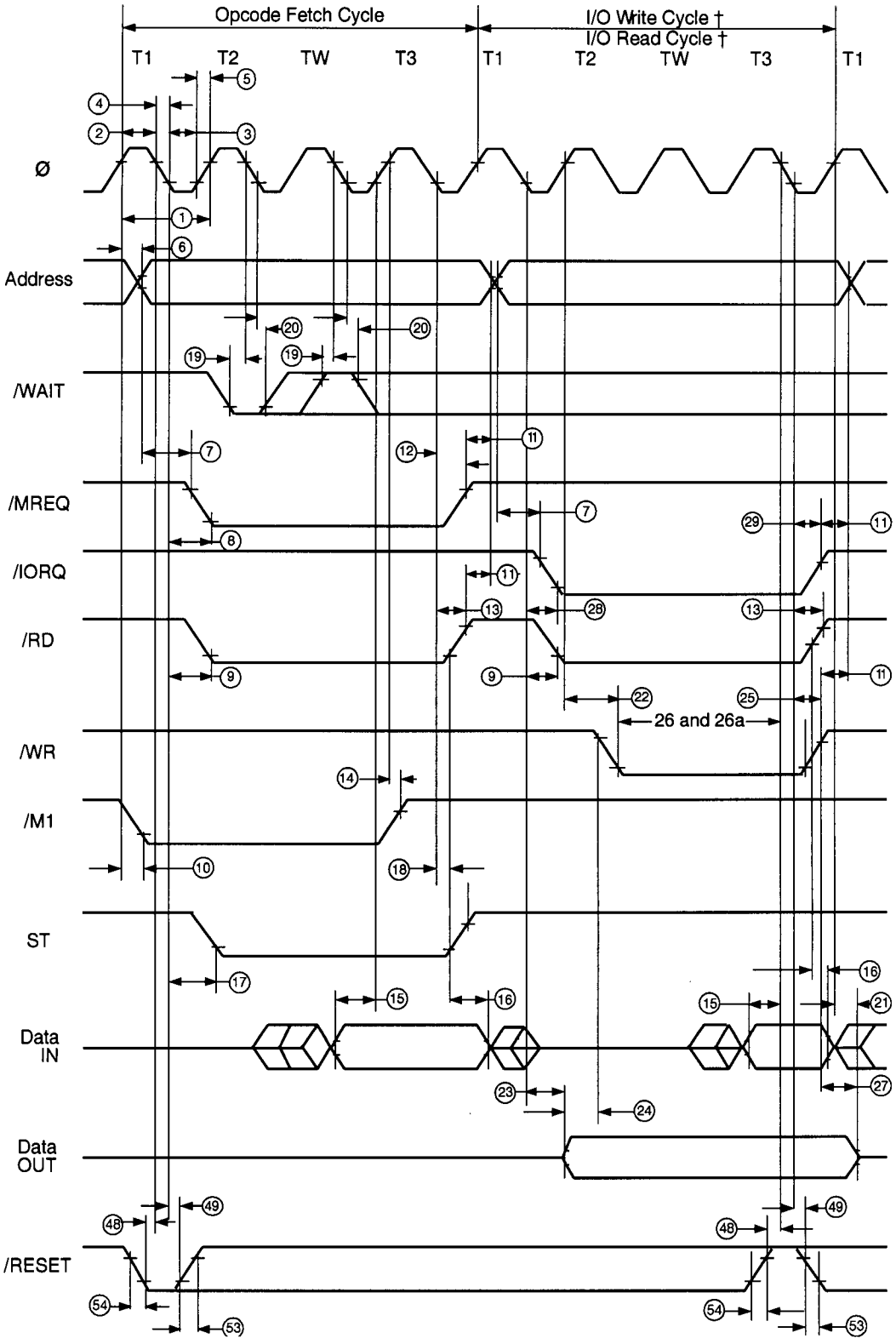


Figure 4. CPU Timing
(Opcode Fetch Cycle, Memory Read/Write Cycle
I/O Read/Write Cycle)

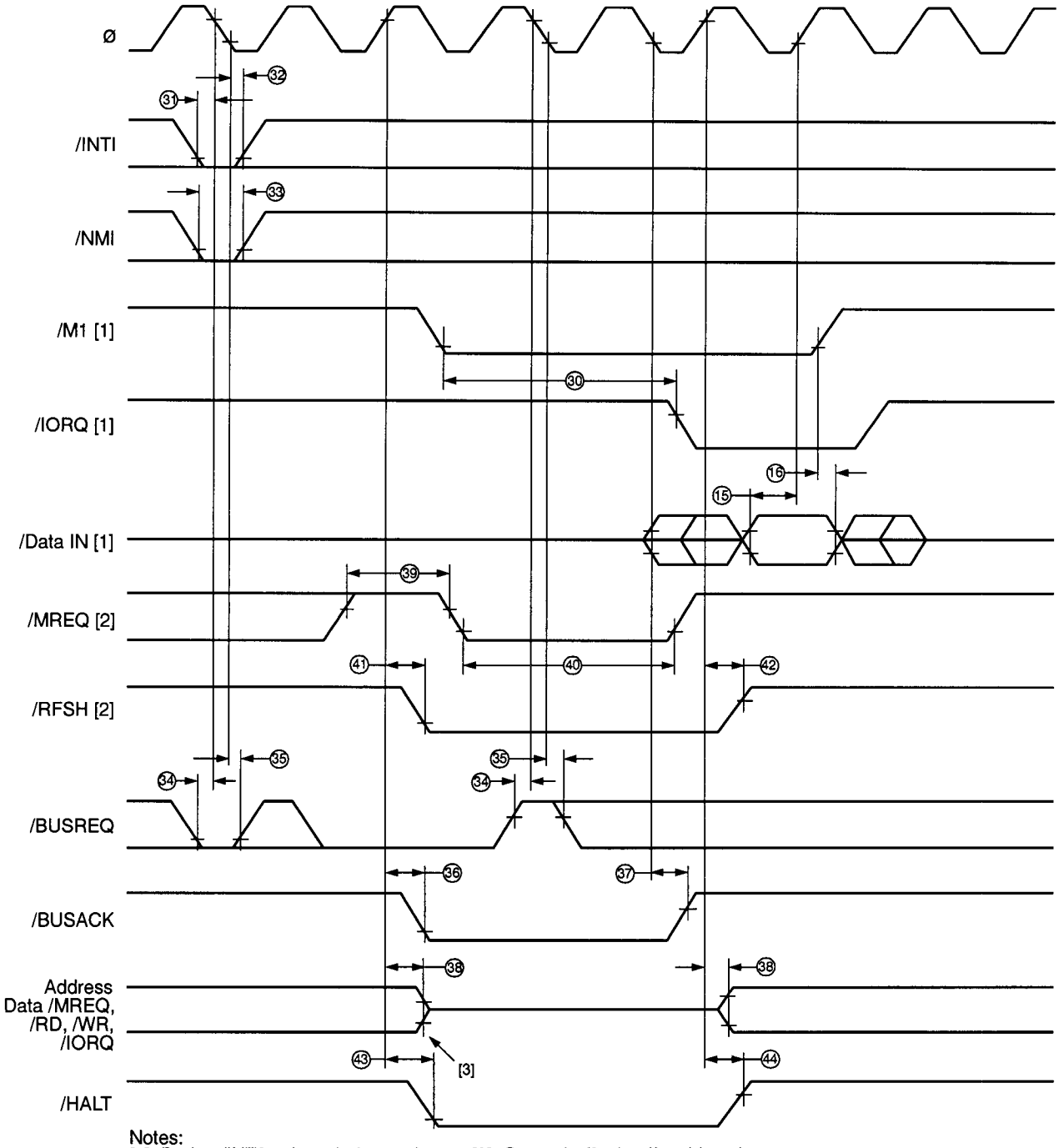


Figure 5. CPU Timing
(/INT0 Acknowledge Cycle, Refresh Cycle, BUS RELEASE mode
HALT mode, SLEEP mode, SYSTEM STOP mode)

TIMING DIAGRAMS (Continued)

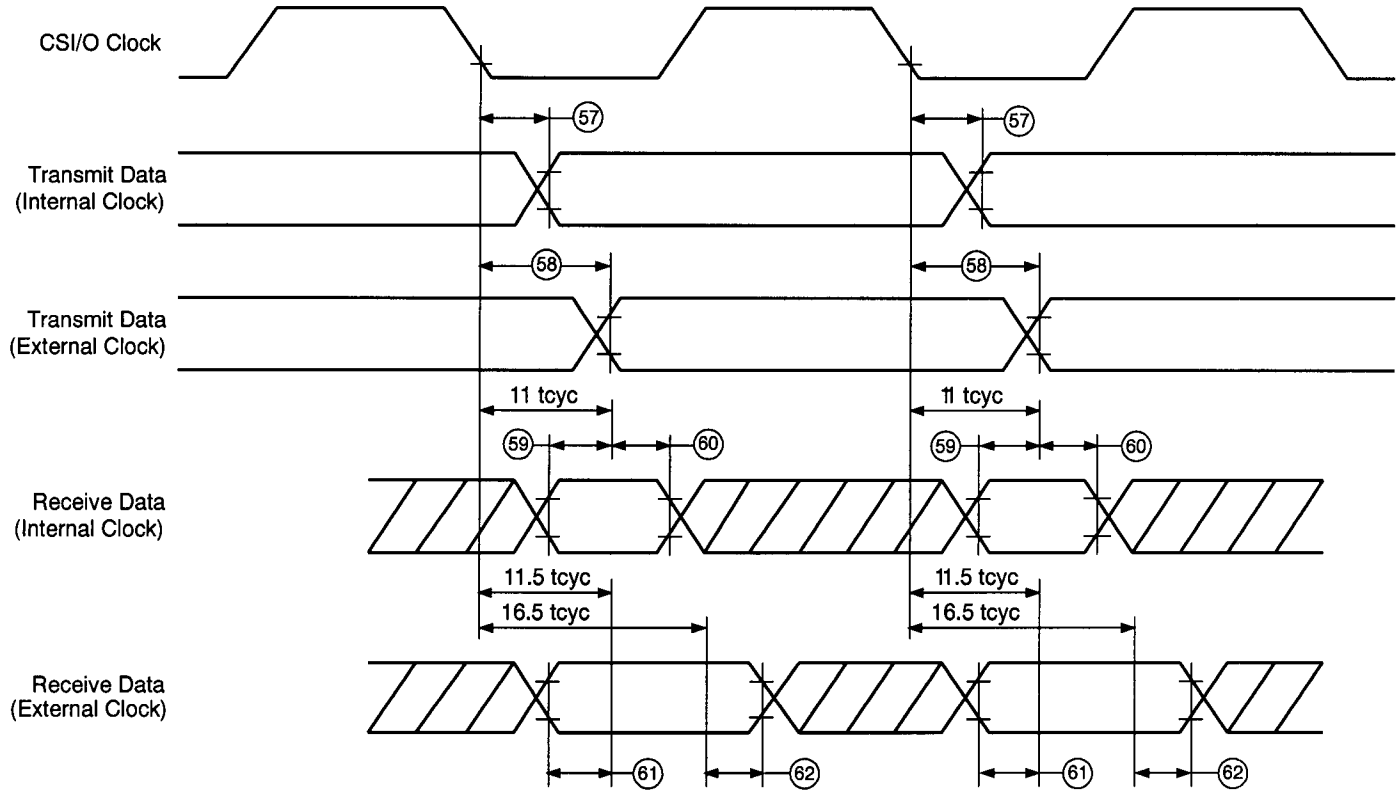


Figure 10. CSI/O Receive/Transmit Timing

EMSCC Timing

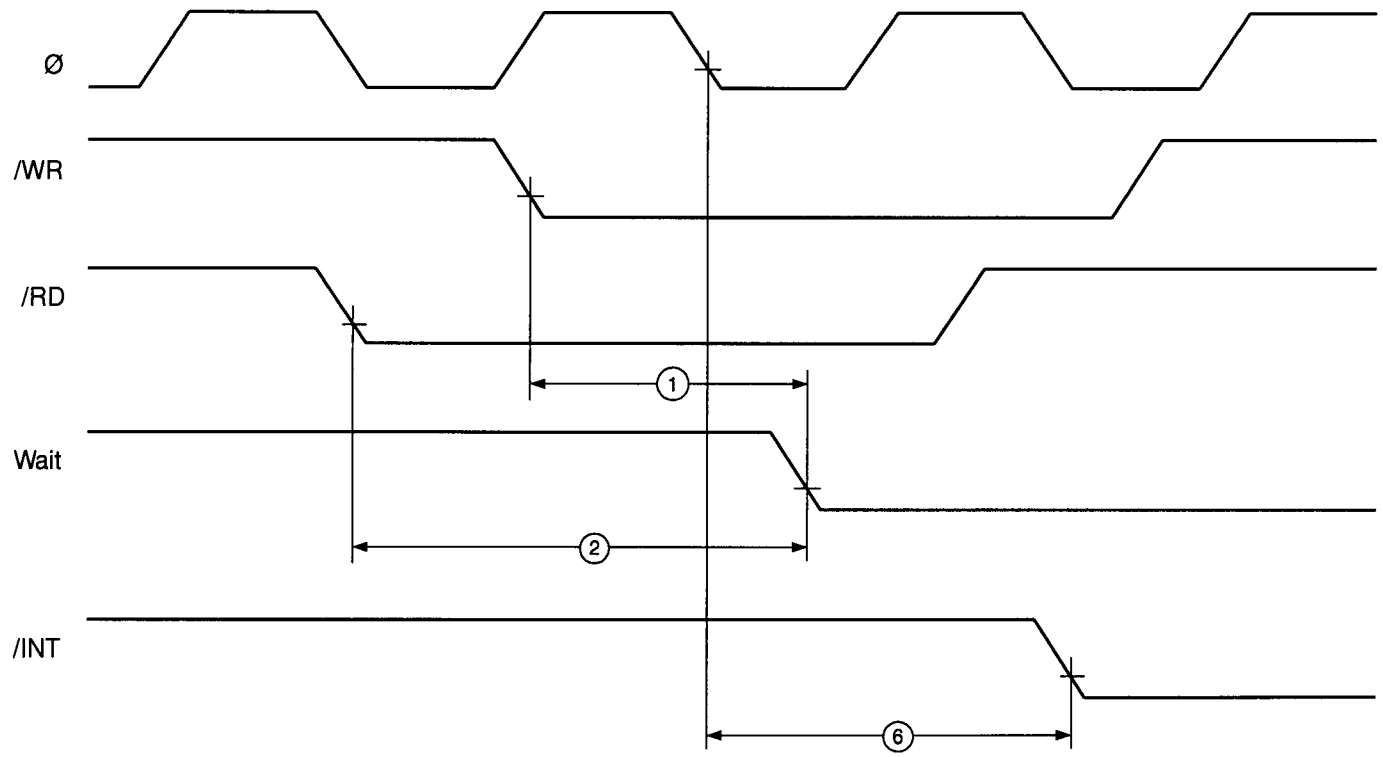


Figure 16. EMSCC AC Parameters

EMSCC Timing Parameters

No.	Symbol	Parameter	20 MHz Min	20 MHz Max	Unit
1	TdWR(W)	/WR Fall to Wait Valid Delay		50	ns
2	TdRD(W)	/RD Fall to Wait Valid Delay		50	
6	TdPC(INT)	Clock to /INT Valid Delay		160	

AC CHARACTERISTICS (Continued)

EMSCC System Timing Diagram

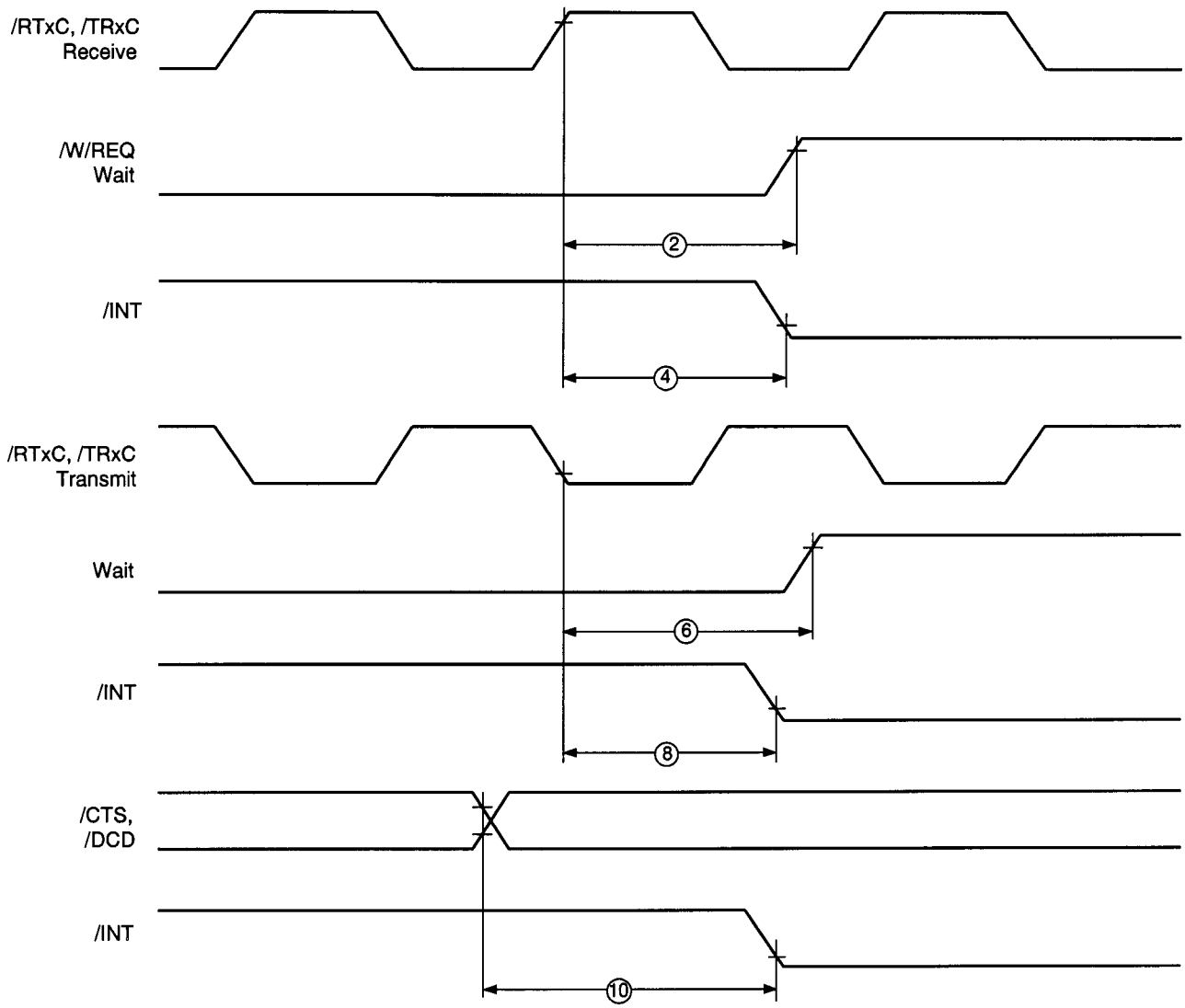


Figure 18. EMSCC System Timing

EMSCC System Timing

No.	Symbol	Parameter	20 MHz Min	20 MHz Max	Notes
2	TdRxC(W)	/RxC to /Wait Inactive	13	18	(1,2)
4	TdRxC(INT)	/RxC to /INT Valid	15	22	(1,2)
6	TdTxC(W)	/TxC to /Wait Inactive	8	17	(1,3)
8	TdTxC(INT)	/TxC to /INT Valid	9	17	(1,3)
10	TdExT(INT)	/DCD or /CTS to /INT Valid	3	9	(1)

Notes:
1. Open-drain output, measured with open-drain test load.
2. /RxC is /RTxC or /TRxC, whichever is supplying the receive clock.
3. /TxC is /TRxC or /RTxC, whichever is supplying the transmit clock.
4. Units equal to TcPc

These AC parameter values are preliminary and subject to change without notice.

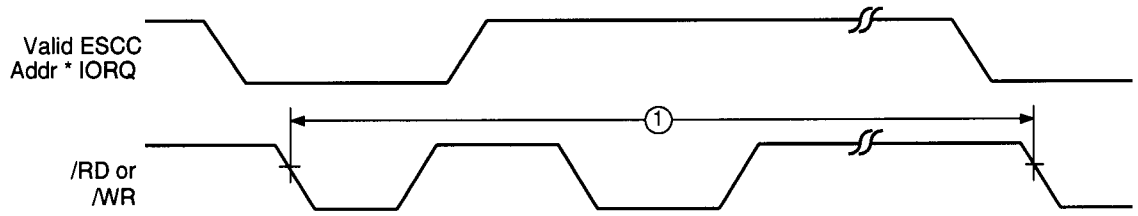


Figure 19. EMSCC External Bus Master Timing

External Bus Master Interface Timing (SCC Related Timing)

No	Symbol	Parameter	Z80185 / Z80195 (20 MHz) Min	Z80185 / Z80195 (20 MHz) Max	Z80185 / Z80195 (33 MHz) Min	Z80185 / Z80195 (33 MHz) Max	Unit	Notes
1	TrC	Valid Access Recovery Time	4TcC		4TcC		ns	(1)

Notes:
1. Applies only between transactions involving the EMSCC.

These AC parameter values are preliminary and subject to change without notice.

T_{CC} = EMSCC Clock Period Time

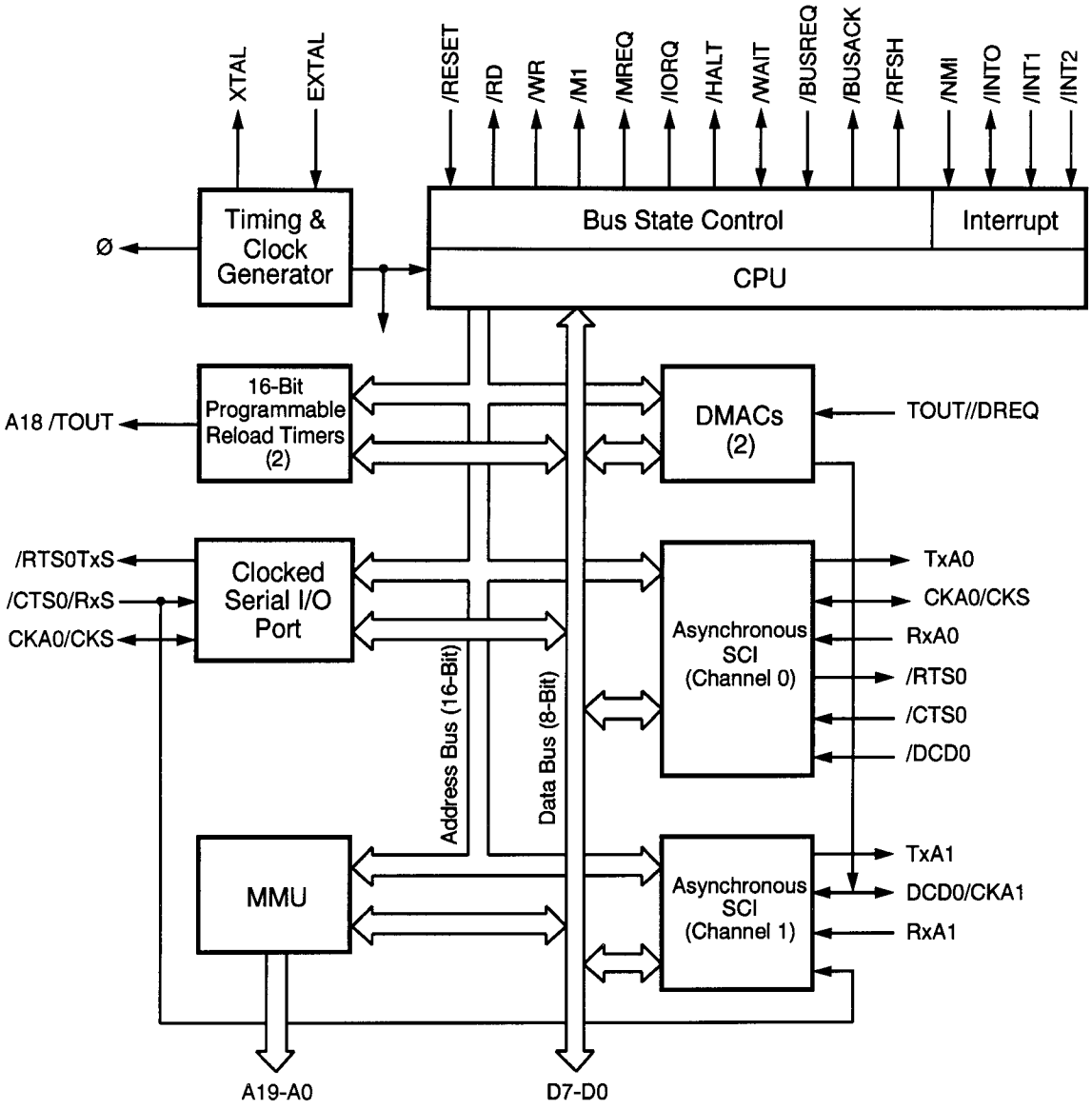


Figure 21. Z8S180 MPU Block Diagram

Z80185 MPU FUNCTIONAL DESCRIPTION (Continued)

DMA Controller

The two DMA channels of the Z80185 can transfer data to or from the EMSCC channel, the parallel interface, the async ports, or an external device. The I/O device encoding in SAR18-16 and DAR18-16 of the existing Z80180 is modified as shown in Table 1.

DMA request signals between the various cells are handled internally by the mechanisms described in this section, and are not pinned-out, nor are the TEND termination count outputs of the DMA channels.

Table 1. SAR18-16 and DAR18-16 I/O Device Encoding

SM1-0	SAR18-16	Source	DM1-0	DAR18-16	Destination
11	000	ext (TOUT/DREQ)	11	000	ext (TOUT/DREQ)
11	001	ASCI0 Rx	11	001	ASCI0 Tx
11	010	ASCI1 Rx	11	010	ASCI1 Tx
11	011	EMSCC Rx	11	011	EMSCC Tx
11	10X	Reserved, do not program.	11	10X	Reserved, do not program.
11	1X0		11	1X0	
11	111	PIA27-20 in	11	111	PIA27-20 out

Asynchronous Serial Communications Interface (ASCI)

The ASCI logic provides two individual full-duplex UARTs. Each channel includes a programmable baud rate generator and modem control signals. The ASCI channels can also support a multiprocessor communications format. For ASCI0, up to three modem control signals and one clock signal can be pinned out, while ASCI1 has a data-only interface.

The receiver includes a 4-byte FIFO, plus a shift register as shown in Figure 22.

During Reset and in I/O Stop state, and for ASCI0 if /DCD0 is auto-enabled and is High, an ASCI is forced to the following conditions:

- FIFO Empty
- All Error Bits Cleared (including those in the FIFO)
- Receive Enable Cleared (cntla bit 6 = 0)
- Transmit Enable Cleared (cntla bit 5 = 0).

If DCD is not auto-enabled, the /DCD pin has no effect on the FIFOs or enable bits.

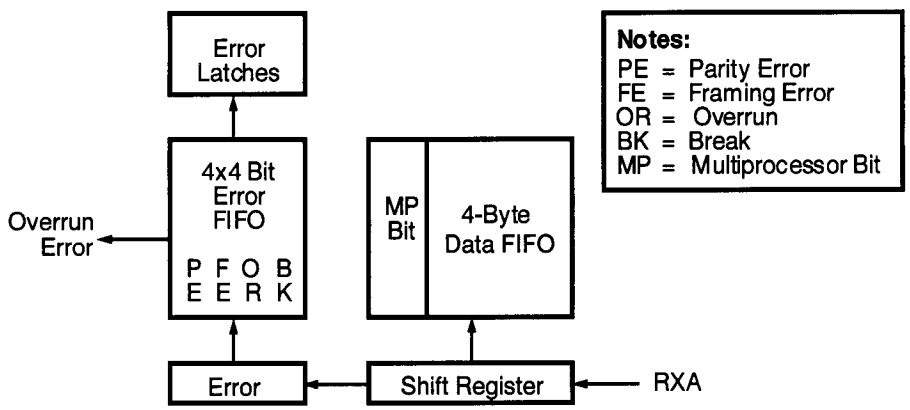


Figure 22. ASCI Receiver

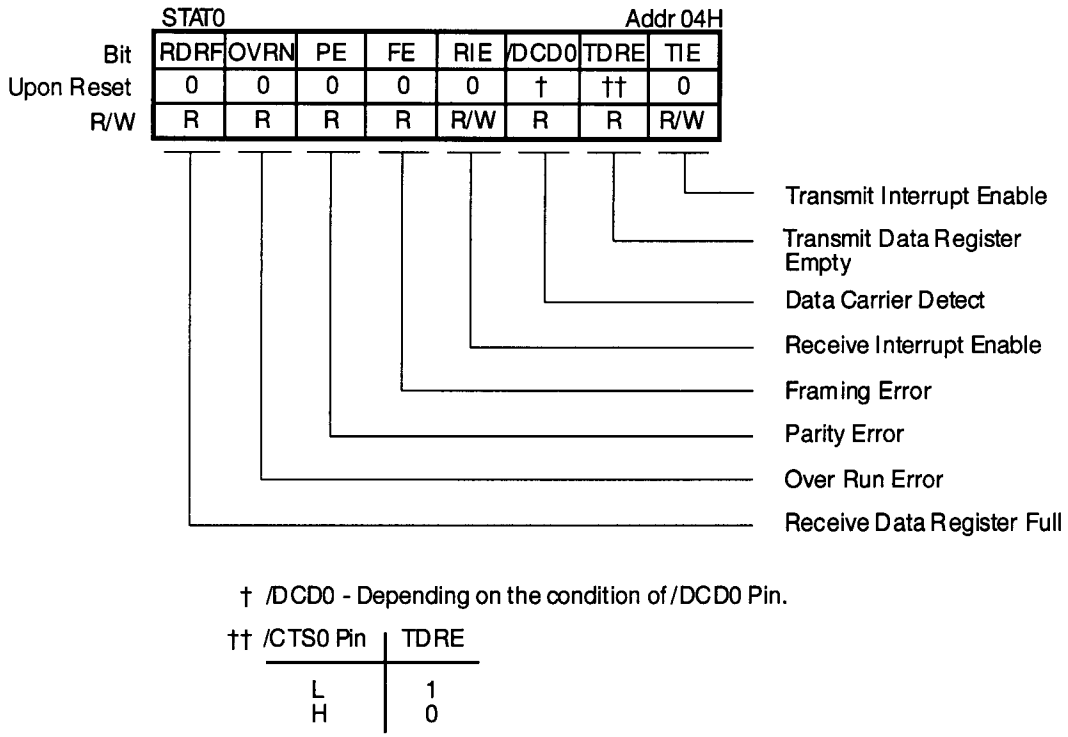


Figure 26. ASCI Status Register (Ch. 0)

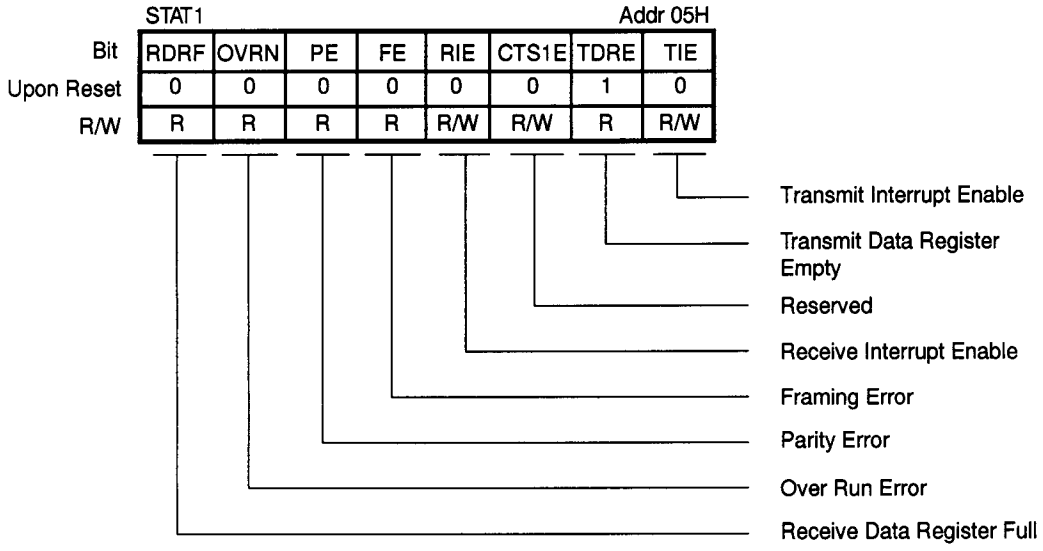


Figure 27. ASCI Status Register (Ch. 1)

TIMER CONTROL REGISTER

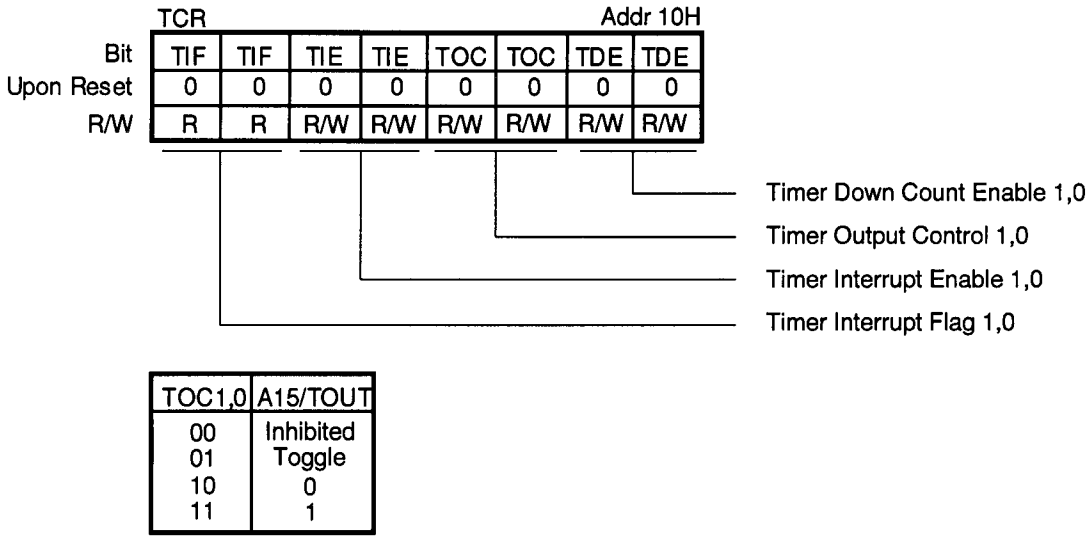


Figure 44. Timer Control Register

FREE RUNNING COUNTER

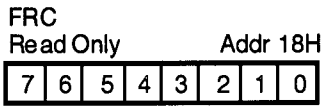


Figure 45. Free Running Counter

CPU CONTROL REGISTER

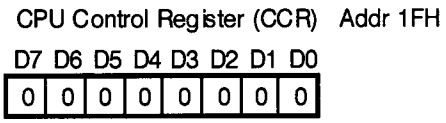
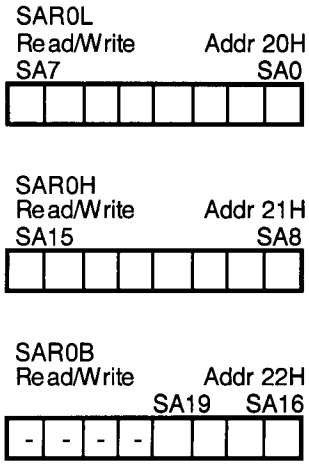


Figure 46. CPU Control Register

Note: See Figure 87 for full description.

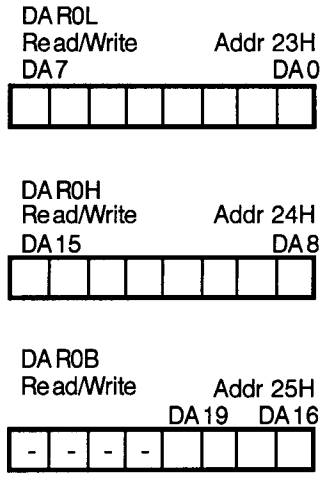
DMA REGISTERS



Bits 0-3 are used for SAR0B

SM1-0	SAR18-16	Source
11	000	ext (TOUT/DREQ)
11	001	ASCI0 Rx
11	010	ASCI1 Rx
11	011	ESCC Rx
11	111	PIA27-20 IN

Figure 47. DMA 0 Source Address Registers



Bits 0-3 are used for DAR0B

DM1-0	DAR18-16	Destination
11	000	ext (TOUT/DREQ)
11	001	ASCI0 Tx
11	010	ASCI1 Tx
11	011	ESCC Tx
11	111	PIA27-20 OUT

Figure 48. DMA 0 Destination Address Registers

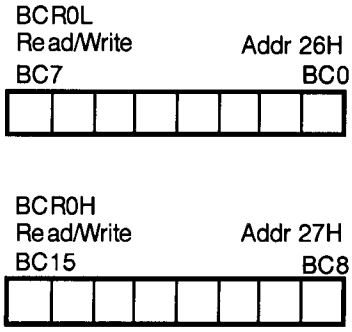


Figure 49. DMA 0 Byte Counter Registers

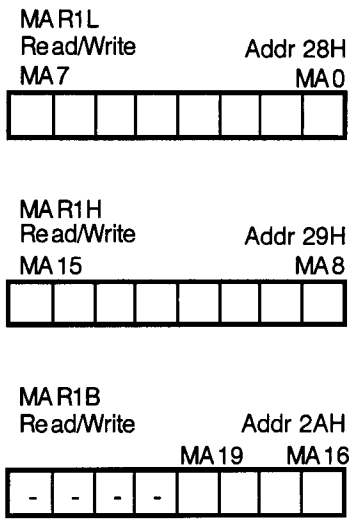


Figure 50. DMA 1 Memory Address Registers

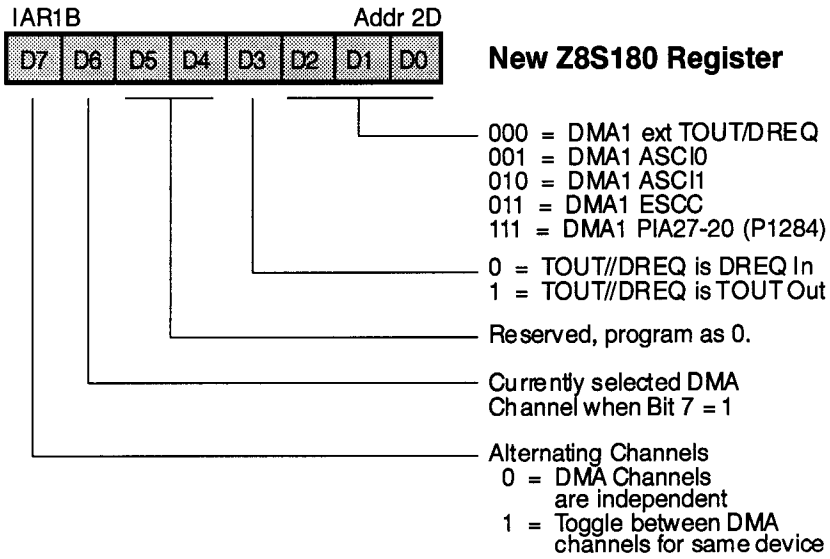


Figure 51. DMA I/O Address Register Ch. 1

CPU CONTROL REGISTER

The CPU Control Register allows the programmer to select options that directly affect the CPU performance as well as controlling the STANDBY operating mode of the chip. The CPU Control Register (CCR) allows the programmer to change the divide-by-two internal clock to divide-by-one. In addition, applications where EMI noise is a problem, the Z8S180 can reduce the output drivers on selected groups of pins to 33 percent of normal pad driver capability which minimizes the EMI noise generated by the part (Figure 65).

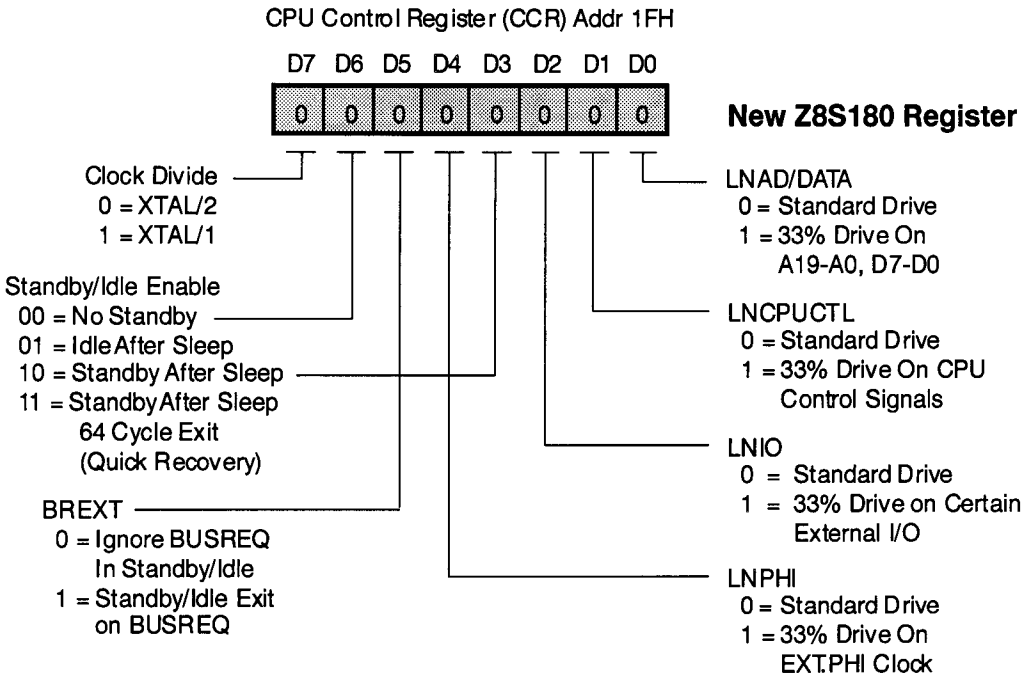


Figure 65. CPU Control Register

P1284 REGISTER MAP

Register Name		I/O Addr/Access
PARM Register		%D9 R/W
PARC Register	(asymmetric)	%DA R/W
PARC2 Register		%DB WO
PART Register		%DC R/W
PARV Register		%DD R/W

Z80185 BIDIRECTIONAL CENTRONICS P1284 CONTROLLER

The Centronics P1284 Controller can operate in either the Host or Peripheral role in Compatibility mode (host to printer), Nibble or Byte mode (printer to host), and ECP mode (bidirectional). It provides no hardware support for the EPP mode, although it may be possible to implement this mode by software.

Nine control signals have dedicated hardware pins, and have ±12 mA drive (P1284 Level 2) capability as does the 8-bit data port PIA27-20. **Note:** Signal names listed below are those for the original Compatible mode. The names shown in parentheses represent the same signal, but in a more recent mode. The Z80185 does not include hardware support for the P1284 EPP mode.

The following signals are outputs in a Peripheral mode, inputs in a Host mode:

- Busy (PtrBusy, PeriphAck)
- nAck (PtrClk, PeriphClk)
- PError (AckDataReq, nAckReverse)
- nFault (nDataAvail, nPeriphRequest)
- Select (Xflag)

The following signals are inputs in a Peripheral mode, outputs in a Host mode:

- nStrobe (HostClk)
- nAutoFd (HostBusy, HostAck)
- nSelectIn (P1284Active)
- nInit (nReverseRequest)

Note that, because the Host/Peripheral mode is fully controlled by software, a Z80185-based product can operate as a Host in one system, or as a Peripheral in another, without any change to the hardware. A Z80185-based product could even act as a Host at one time and a Peripheral at another time within the same system, if there is a mechanism to control such alternate use.

In general, the interface architecture automates operations that are seen as performance-critical, while leaving less frequent operations to software control. To achieve top performance, software should assign a DMA channel to the current direction of data flow.

Note: The IEEE 1284 Interface should be used with the/IOC bit (bit D5) in the OMCR set to 0. The setting of this bit primarily affects RLE expansion in peripheral ECP forward and host ECP reverse modes.

Interrupts

As in other Zilog peripherals, the controller includes an interrupt pending bit (IP), and an interrupt under service bit (IUS). The controller is part of an on-chip interrupt acknowledge daisy-chain that extends from the IEI pin, through the EMSCC, CTC, and this controller in a programmable priority order, and from the lowest-priority of these devices to the IEO pin. The interrupt request from the controller is logically ORed with /INT0 and other on-chip interrupt requests to the processor.

The controller sets its IP bit whenever any of three conditions occurs:

1. PARM4 is 1, and the controller sets the DREQ bit. This does not include when the controller forces the DREQ bit to 1, when software first places the controller in Peripheral Nibble, Peripheral Byte, Peripheral ECP Reverse, Host Compatible, or Host ECP Forward mode.

2. PARM5 is 1, and a mode-dependent "status interrupt" condition occurs. The following sections describe the status interrupt conditions (if any) for each mode.

3. PARM6 is 1, and the controller sets the Idle bit, except when the controller forces the Idle bit to 1, when software first places the controller in Peripheral Nibble, Peripheral Byte, Peripheral ECP Reverse, Host Compatible, or Host ECP Forward mode. The following sections describe when Idle is set in each mode.

Once IP is set, it remains set until software writes a 1 to PART6.

The controller will begin requesting an interrupt of the processor whenever IP is set, its IEI signal from the on-chip daisy-chain is High/true, and its IUS bit is 0. Once it starts requesting an interrupt, the controller will continue to do so until /IORQ goes Low in an interrupt-acknowledge cycle, or IP is 0, or IUS is 1.

The controller drives its IEO output High, if its IEI input is High, and its IP and IUS bits are both 0. A Z80 interrupt acknowledge cycle is signalled by /M1 going Low, followed by /IORQ going Low. The controller, and all other devices in the daisy-chain, freeze the contribution of their IP bits to their IEO outputs while /M1 is Low, which prevents new events from affecting the daisy-chain. By the time/IORQ goes Low, one and only one device will have its IEI pin High and its IEO pin Low — this device responds to the interrupt by providing an interrupt vector, and setting its IUS bit. This controller also clears its IP bit when it responds to an interrupt acknowledge cycle.

The interrupt service routine, that is initiated when the interrupt vector value identifies an interrupt from this controller, should save the processor context and then proceed as follows:

1. If the ISR does not allow nested interrupts, it can clear the IP and IUS bits by writing hex 60, plus the "critical time" value to the PART, then read the status from PARC and proceed based on that status. Near the end of the ISR it should re-enable processor interrupts.

2. If the ISR allows nested interrupts, it can re-enable processor interrupts, clear IP by writing hex 40 plus the "critical time" value to the PART, and then read the status from PARC and proceed based on that status. At the end of the ISR it should clear IUS to allow further interrupts from this controller and devices lower on the daisy-chain, by writing hex 20 plus the "critical time" value to the PART.

The remainder of this section describes the operation of the various PARM register modes that can be selected.

Non-P1284 Mode

The Z80185 defaults to this mode after a Reset, and this mode is compatible with the use of PIA27-20 on the Z80181. The directions of PIA27-20 can be controlled individually by writing to register E2, as on the Z80181. The state of outputs among PIA27-20 can be set by writing to register E3, and the state of all eight pins can be sensed by reading register E3. The Busy, nAck, PError, nFault, and Select pins are tri-stated in this mode, while nStrobe, nAutoFd, nSelectIn, and nInit are inputs. There are no status interrupts in this mode.

Peripheral Inactive Mode

This mode operates identically to Non-P1284 mode as described above, except that the Busy, nAck, PError, nFault, and Select pins are outputs that can be controlled via the PARC and PARC2 registers, and status interrupts can occur in response to any edge on nAutoFd, nStrobe, nSelectIn, or nInit. This mode differs from Peripheral Compatibility/Negotiation mode with nSelectIn (P1284 Active) High, only in that the controller will not operate in Compatibility mode if nSelectIn goes Low.

Z80185 BIDIRECTIONAL CENTRONICS P1284 CONTROLLER (Continued)

Host Compatible Mode

1. Setting this mode configures PIA27-20 as outputs regardless of the contents of register E2. When entering this mode, the controller sets the Idle and DREQ bits, but these settings do not request an interrupt.

2. If software, or a DMA channel, writes eight bits to the Output Holding Register (OHR) when Idle is set, the controller transfers the byte to the Input/Output Register and negates DREQ only momentarily, so as to request another byte from software or the DMA channel.

3. In this mode, the nAutoFd line is not under control of the PARC register, but rather under control of which register the software uses to write data to the OHR. Each time the controller transfers a byte from the OHR to the Input/Output Register, it sets nAutoFd High if the byte was written to address E3, and Low if the byte was written to the "alternate" address EE. In a DMA application all of the bytes transferred from one output buffer will have the same state of nAutoFd, but this state can be changed from one buffer to the next by changing thel/O address used by the DMA channel. In non-DMA applications software can set the state of nAutoFd for each character, by writing data to the two different register addresses.

4. When a data byte has been valid on PIA27-20 for 750 ns (as controlled by the PART register), and the Busy and PError lines are Low and the Select, nAck, and nFault lines are High, the controller drives nStrobe Low. After the controller has held nStrobe Low for 750 ns it drives nStrobe back to High. Then it waits for 750 ns of data hold time to elapse. If software or a DMA channel has written another byte to the Output Holding Register (thus clearing DREQ) by the time this wait is satisfied, the controller transfers the byte from the Output Holding Register to the Input/Output Register, sets DREQ again, and returns to the event sequence at the start of this paragraph. Otherwise, it sets Idle and returns to the event sequence at the start of paragraph #2.

Status interrupts in this mode include rising and falling edges on PError, nFault, and Select.

Host Negotiation Mode

Setting this mode puts PIA27-20 under control of registers E2 and E3, as on the Z80181.

Software has complete control of the controller, and can either revert to Host Compatibility mode, or set one of the following Host modes, depending on how the peripheral responds to the Negotiation value(s).

Status interrupts in this mode include rising and falling edges on PtrClk (nAck), nAckReverse (PError), and nPeriphRequest (nFault). nFault is not used during actual P1284 negotiation, but is included because these events are significant during Byte and ECP mode idle times.

Host Reserved Mode

This mode differs from Host Negotiation mode only in that there are no status interrupts in this mode.

Peripheral Compatible/Negotiation Mode

In this mode, if P1284Active (nSelectIn) is Low, the controller sets PIA27-20 as inputs, regardless of the contents of register E2; when P1284Active (nSelectIn) is High, PIA27-20 are under the control of registers E2 and E3. On entry to this mode, the controller sets the Idle bit, if DREQ is set from a previous mode.

If, in this mode, nStrobe goes (is) Low, P1284Active (nSelectIn) is Low, and DREQ is 0, indicating that any previous data has been taken by the processor or DMA channel, the controller captures the data on PIA27-20 into the Input/Output Register, sets DREQ to notify software or the DMA channel to take the byte, drives the Busy line High, and one PHI clock later drives nAck Low. When at least 500 ns (as controlled by the PART register) have elapsed, the controller drives nAck back to High. One PHI clock later, if the CPU or DMA has taken the data and thus cleared DREQ, the controller drives Busy back to Low, otherwise it sets Idle.

Select, PError and nFault are under software control in this mode, and nAutoFd can be sensed by software, but has no other effect on operation.

Z80185 CTC, AND MISCELLANEOUS REGISTERS (Continued)

CTC Control Registers

Channel Control Byte
This byte is used to set the operating modes and parameters. Bit D0 must be a 1 to indicate that this is a Control Byte (Figure 82).

The Channel Control Byte register has the following fields:

Bit D7. *Interrupt Enable.* This bit enables the interrupt logic so that an internal INT is generated at zero count. Interrupts are programmed in either mode, and may be enabled or disabled at any time.

Bit D6. *Mode Bit.* This bit, along with bit 3, is used to select either Timer mode or Counter mode (Table 8).

Bit D5. *Prescaler Factor.* This bit selects the prescaler factor for use in the timer mode. Either divide-by-16 or divide-by-256 is available.

Bit D4. *Clock/Trigger Edge Selector.* This bit selects the active edge of the CLK/TRG input pulses.

Bit D3. *Mode Bit.* This bit, along with bit 6, selects either Timer mode or Counter mode (Table 8).

Bit D2. *Time Constant.* This bit indicates that the next byte programmed is time *constant data for the downcounter.*

Bit D1. *Software Reset.* Writing a 1 to this bit indicates a software reset operation, which stops counting activities until another time constant word is written.

Table 8. CTC Operation Modes

CCW6	CCW3	Operation
0	0	(Auto Start) Timer mode. The prescaler is clocked by PHI, and the counter is clocked by the prescaler. Counting is enabled when the timer constant is loaded.
0	1	Timer with CLK/TRG Trigger. The prescaler is clocked by PHI, and the counter is clocked by the prescaler. Timing starts when the transition specified by D4 is detected on the PIA pin, or for CTC3-1, the ZC/T0 output of CTC2-0, respectively.
1	0	Classic Counter mode. The counter is clocked by the PIA pin, or for CTC3-1 the ZC/TO output of CTC-2 respectively.
1	1	Long Counter mode. The prescaler is clocked by the PIA pin, or for CTC3-1 the ZC/TO output of CTC-2, respectively, and the counter is clocked by the prescaler.

ELECTRICAL CHARACTERISTICS (Continued)

The following table shows the characteristics of each pin in terms of the above classifications. A dash "–" in the input or output column indicates the pin does not have that function.

Table 9. Pin Classification Characteristics

Pin	Input Class	Output Class
/BUSREQ	I	–
/CTS	I	–
/CTS0/RxS	I	–
/DCD	I	–
/DCD0/CKA1	I	3
/DTR	–	O
/HALT	–	O
/INT0	I	D
/INT1	I	–
/INT2	I	–
/IOCS	–	O
/IORQ	I	3
/M1	I	3
/MREQ	I	3
/NMI	R	–
/RAMCS	–	O
/RD	I	3
/RESET	R	D
/RFSH	–	O
/ROMCS	–	O
/RTS	–	O
/RTS0/TxS	–	O
/RTXC	I	3
/TRXC	I	3
/WAIT	I	D
/WR	I	3
A0-A19	I	3
Busy	S	T
CKA0/CKS	I	3
D0-D7	I	3
EXTAL	R	–
IEI	I	–
IEO	–	O
nAck	S	T
nAutoFd	S	T
nFault	S	T
nInit	S	T
nSelectIn	S	T
nStrobe	S	T
PError	S	T
PHI	–	H
PIA13-10/CLKTRG3-0	I	3
PIA15-13/ZCTO2-0	I	3
PIA27-20	S	T
RXA0	I	–
RXA1	I	–
RXD	I	–
/ST	–	O
Select	S	T
TOUT//DREQ	I	O
TXA0	–	O
TXA1	–	O
TXD	–	O
XTAL	–	O