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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	180MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, LINbus, SAI, SDIO, SPI, UART/USART, USB, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	161
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	384K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	208-LQFP
Supplier Device Package	208-LQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f479bgt6

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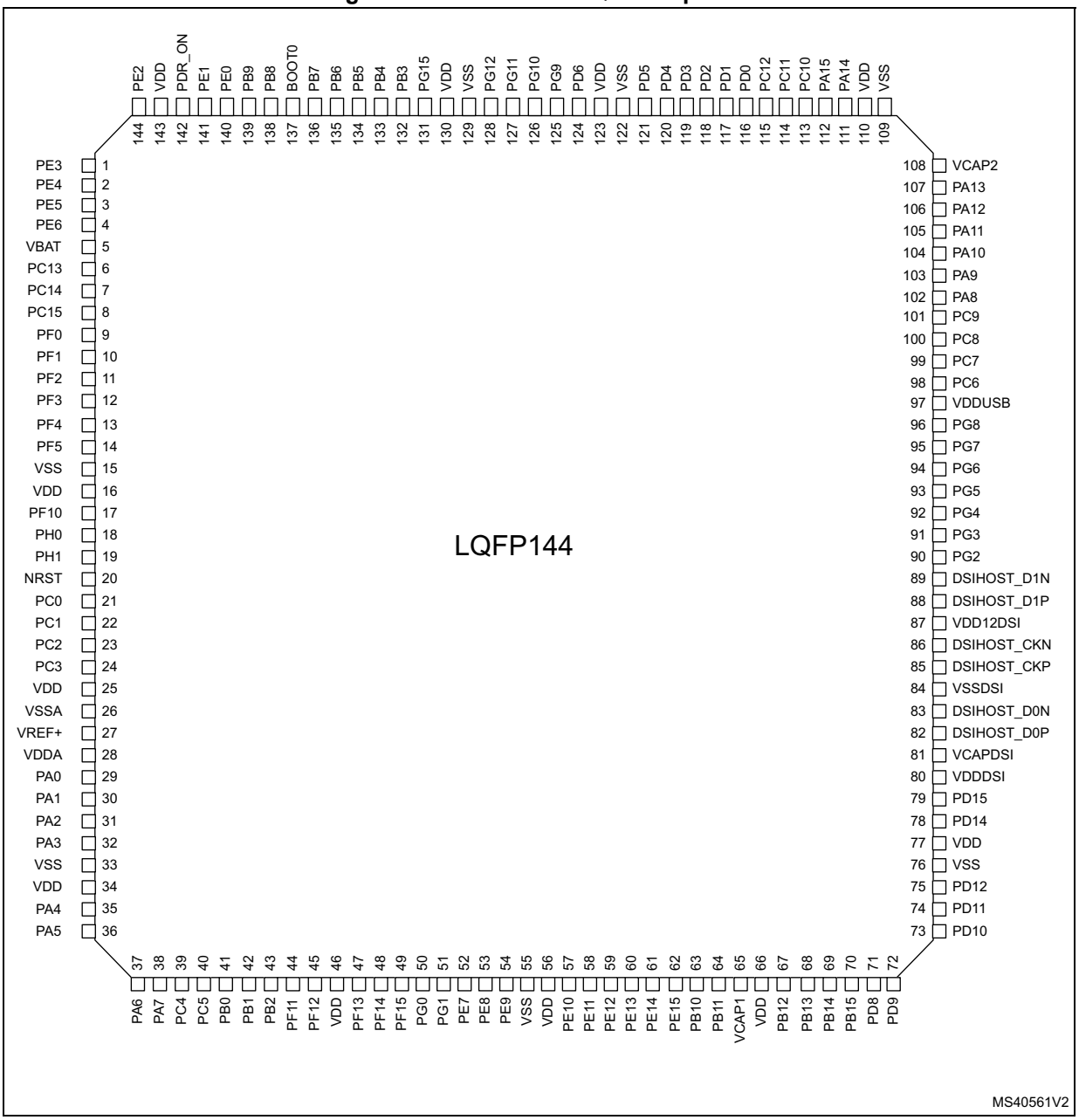
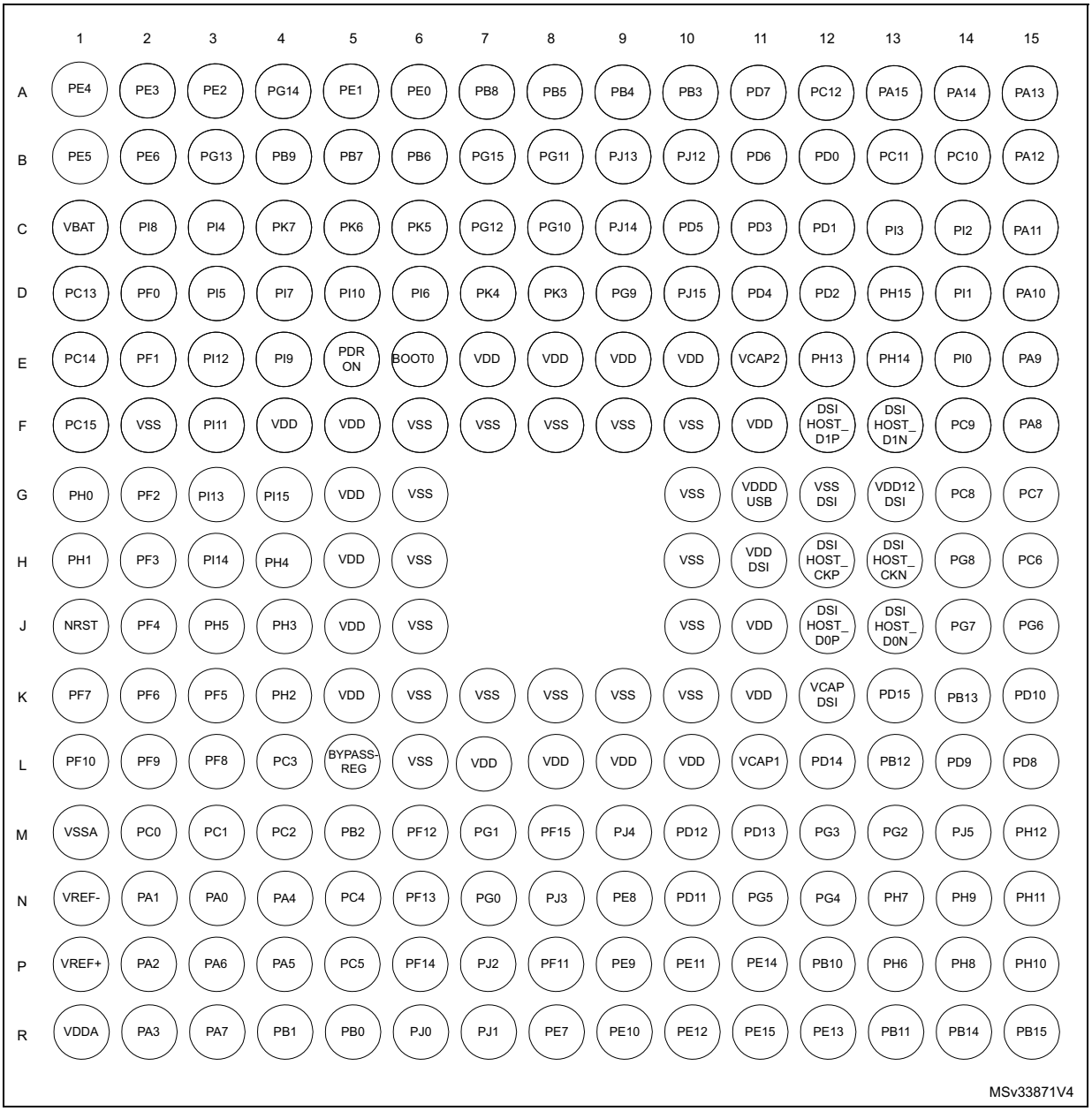
Figure 14. STM32F47x LQFP144 pinout



1. The above figure shows the package top view.

Figure 20. STM32F47x TFBGA216 ballout



1. The above figure shows the package top view.

Table 11. FMC pin definition

Pin name	NOR/PSRAM/SRAM	NOR/PSRAM Mux	NAND16	SDRAM
PF0	A0	-	-	A0
PF1	A1	-	-	A1
PF2	A2	-	-	A2
PF3	A3	-	-	A3
PF4	A4	-	-	A4
PF5	A5	-	-	A5
PF12	A6	-	-	A6
PF13	A7	-	-	A7
PF14	A8	-	-	A8
PF15	A9	-	-	A9
PG0	A10	-	-	A10
PG1	A11	-	-	A11
PG2	A12	-	-	A12
PG3	A13	-	-	
PG4	A14	-	-	BA0
PG5	A15	-	-	BA1
PD11	A16	A16	CLE	-
PD12	A17	A17	ALE	-
PD13	A18	A18	-	-
PE3	A19	A19	-	-
PE4	A20	A20	-	-
PE5	A21	A21	-	-
PE6	A22	A22	-	-
PE2	A23	A23	-	-
PG13	A24	A24	-	-
PG14	A25	A25	-	-
PD14	D0	DA0	D0	D0
PD15	D1	DA1	D1	D1
PD0	D2	DA2	D2	D2
PD1	D3	DA3	D3	D3
PE7	D4	DA4	D4	D4
PE8	D5	DA5	D5	D5
PE9	D6	DA6	D6	D6
PE10	D7	DA7	D7	D7
PE11	D8	DA8	D8	D8

Table 13. STM32F479xx register boundary addresses(1)

Bus	Boundary address	Peripheral
-	0xE00F FFFF - 0xFFFF FFFF	Reserved
Cortex®-M4	0xE000 0000 - 0xE00F FFFF	Cortex®-M4 internal peripherals
AHB3	0xD000 0000 - 0xDFFF FFFF	FMC bank 6
	0xC000 0000 - 0xCFFF FFFF	FMC bank 5
	0xA000 1000 - 0xA0001FFF	Quad-SPI control register
	0xA000 2000 - 0xBFFF FFFF	Reserved
	0xA000 0000- 0xA000 0FFF	FMC control register
	0x9000 0000 - 0x9FFF FFFF	Quad-SPI bank
	0x8000 0000 - 0x8FFF FFFF	FMC bank 3
	0x7000 0000 - 0x7FFF FFFF	FMC bank 2 (reserved)
	0x6000 0000 - 0x6FFF FFFF	FMC bank 1
-	0x5006 0C00- 0x5FFF FFFF	Reserved
AHB2	0x5006 0800 - 0x5006 0BFF	RNG
	0x5006 0400 - 0x5006 07FF	HASH
	0x5006 0000 - 0x5006 03FF	CRYP
	0x5005 0400 - 0x5005 FFFF	Reserved
	0x5005 0000 - 0x5005 03FF	DCMI
	0x5004 0000- 0x5004 FFFF	Reserved
	0x5000 0000 - 0x5003 FFFF	USB OTG FS

5 Electrical characteristics

5.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

5.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = 25 °C and T_A = $T_A$max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean±3σ).

5.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = 3.3 V (for the 1.7 V ≤V_{DD} ≤3.6 V voltage range). They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean±2σ).

5.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

5.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 22*.

5.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 23*.

Figure 22. Pin loading conditions

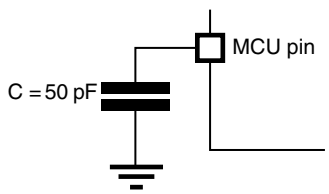
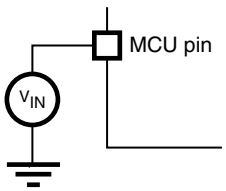


Figure 23. Pin input voltage



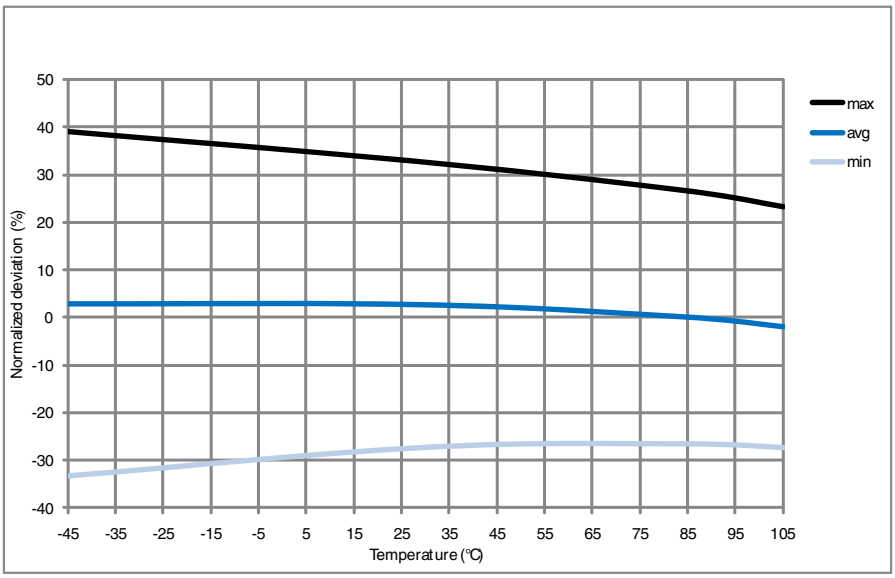
Low-speed internal (LSI) RC oscillator

Table 40. LSI oscillator characteristics (1)

Symbol	Parameter	Min	Typ	Max	Unit
f_{LSI}(2)	Frequency	17	32	47	kHz
$t_{su(LSI)}$(3)	Startup time	-	15	40	µs
$I_{DD(LSI)}$(3)	Power consumption	-	0.4	0.6	µA

1. V_{DD} = 3 V, T_A = –40 to 105 °C unless otherwise specified.
2. Based on test during characterization.
3. Guaranteed by design.

Figure 34. ACC_{LSI} versus temperature



MS19013V1

5.3.11 PLL characteristics

The parameters given in *Table 41* and *Table 42* are derived from tests performed under temperature and V_{DD} supply voltage conditions summarized in *Table 17*.

Table 41. Main PLL characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PLL_IN}	PLL input clock(1)	-	0.95(2)	1	2.10	MHz
f_{PLL_OUT}	PLL multiplier output clock	-	24	-	180	
f_{PLL48_OUT}	48 MHz PLL multiplier output clock	-	-	48	75	
f_{VCO_OUT}	PLL VCO output	-	192	-	432	

Table 42. PLLI2S (audio PLL) characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{DD(PLLI2S)}$(4)	PLLI2S power consumption on V_{DD}	VCO freq = 192 MHz VCO freq = 432 MHz	0.15 0.45	-	0.40 0.75	mA
$I_{DDA(PLLI2S)}$(4)	PLLI2S power consumption on V_{DDA}	VCO freq = 192 MHz VCO freq = 432 MHz	0.30 0.55	-	0.40 0.85	

1. Take care of using the appropriate division factor M to have the specified PLL input clock values.
2. Guaranteed by design.
3. Value given with main PLL running.
4. Based on test during characterization.

Table 43. PLLSAI (audio and LCD-TFT PLL) characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{PLLSAI_IN}	PLLSAI input clock(1)	-		0.95(2)	1	2.10	MHz
f_{PLLSAI_OUT}	PLLSAI multiplier output clock	-		-	-	216	
f_{VCO_OUT}	PLLSAI VCO output	-		192	-	432	
t_{LOCK}	PLLSAI lock time	VCO freq = 192 MHz		75	-	200	µs
		VCO freq = 432 MHz		100	-	300	
Jitter(3)	Main SAI clock jitter	Cycle to cycle at 12.288 MHz on 48KHz period, N=432, R=5	RMS	-	90	-	ps
			peak to peak	-	±280	-	
		Average frequency of 12.288 MHz N = 432, R = 5 on 1000 samples		-	90	-	ps
	FS clock jitter	Cycle to cycle at 48 KHz on 1000 samples		-	400	-	ps
$I_{DD(PLLSAI)}$(4)	PLLSAI power consumption on V_{DD}	VCO freq = 192 MHz VCO freq = 432 MHz		0.15 0.45	-	0.40 0.75	mA
$I_{DDA(PLLSAI)}$(4)	PLLSAI power consumption on V_{DDA}	VCO freq = 192 MHz VCO freq = 432 MHz		0.30 0.55	-	0.40 0.85	

1. Take care of using the appropriate division factor M to have the specified PLL input clock values.
2. Guaranteed by design.
3. Value given with main PLL running.
4. Based on test during characterization.

Table 45. MIPI D-PHY characteristics(1) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CMTX}	HS transmit common mode voltage	-	150	200	250	mV
$\|\Delta V_{CMTX}\|$	V_{CMTX} mismatch when output is Differential-1 or Differential-0	-	-	-	5	
$\|V_{OD}\|$	HS transmit differential voltage	-	140	200	270	
$\|\Delta V_{OD}\|$	V_{OD} mismatch when output is Differential-1 or Differential-0	-	-	-	14	
V_{OHHS}	HS output high voltage	-	-	-	360	
Z_{OS}	Single ended output impedance	-	40	50	62.5	Ω
ΔZ_{OS}	Single ended output impedance mismatch	-	-	-	10	%
t_{HSr} & t_{HSf}	20%-80% rise and fall time	-	100	-	0.35*UI	ps
LP Receiver Input Characteristics						
V_{IL}	Logic 0 input voltage (not in ULP State)	-	-	-	550	mV
$V_{IL-ULPS}$	Logic 0 input voltage in ULP State	-	-	-	300	
V_{IH}	Input high level voltage	-	880	-	-	
V_{hys}	Voltage hysteresis	-	25	-	-	
LP Emitter Output Characteristics						
V_{IL}	Output low level voltage	-	1.1	1.2	1.2	V
$V_{IL-ULPS}$	Output high level voltage	-	-50	-	50	mV
V_{IH}	Output impedance of LP transmitter	-	110	-	-	Ω
V_{hys}	15%-85% rise and fall time	-	-	-	25	ns
LP Contention Detector Characteristics						
V_{ILCD}	Logic 0 contention threshold	-	-	-	200	mV
V_{IHCD}	Logic 0 contention threshold	-	450	-	-	

1. Guaranteed based on test during characterization.

Table 55. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Class	Maximum value(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C conforming to ANSI/ESDA/JEDEC JS-001	2	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = +25 °C conforming to ANSI/ESD S5.3.1, LQFP176, LQFP208, UFBGA169, UFBGA176, TFBGA216 and WLCSP148 packages	C3	250	

1. Guaranteed based on test during characterization.

Static latchup

Two complementary static tests are required on six parts to assess the latchup performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with EIA/JESD 78A IC latchup standard.

Table 56. Electrical sensitivities(1)

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	T_A = +105 °C conforming to JESD78A	II level A

1. MSV on PA4 and PA5 is 5 V, versus 5.4 V on all IOs.

5.3.19 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DD} (for standard, 3 V-capable I/O pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

Functional susceptibility to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (>5 LSB TUE), out of conventional limits of induced leakage current on adjacent pins (out of –5 µA/+0 µA range), or other functional failure (for example reset, oscillator frequency deviation).

Negative induced leakage current is caused by negative injection and positive induced leakage current by positive injection.

The test results are given in *Table 57*.

1. Guaranteed based on test during characterization.
2. Spikes with widths below $t_{AF(min)}$ are filtered.
3. Spikes with widths above $t_{AF(max)}$ are not filtered

SPI interface characteristics

Unless otherwise specified, the parameters given in *Table 64* for the SPI interface are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in *Table 17*, with the following configuration:

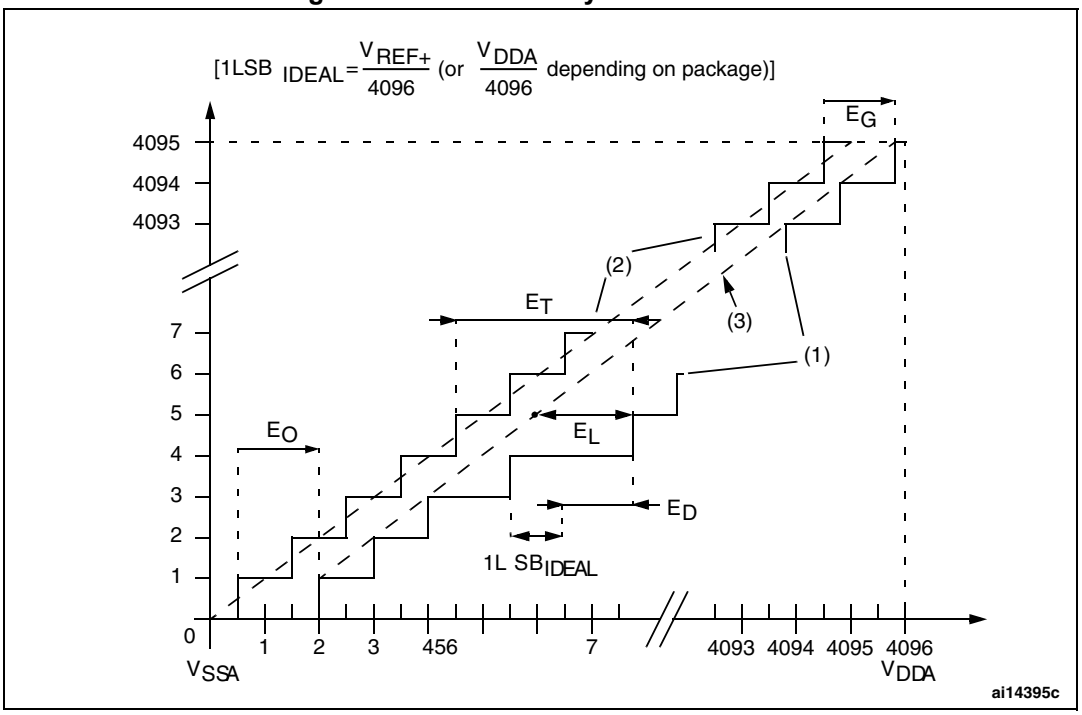
- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: 0.5 V_{DD}

Refer to *Section 5.3.20* for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO for SPI).

Table 64. SPI dynamic characteristics(1)

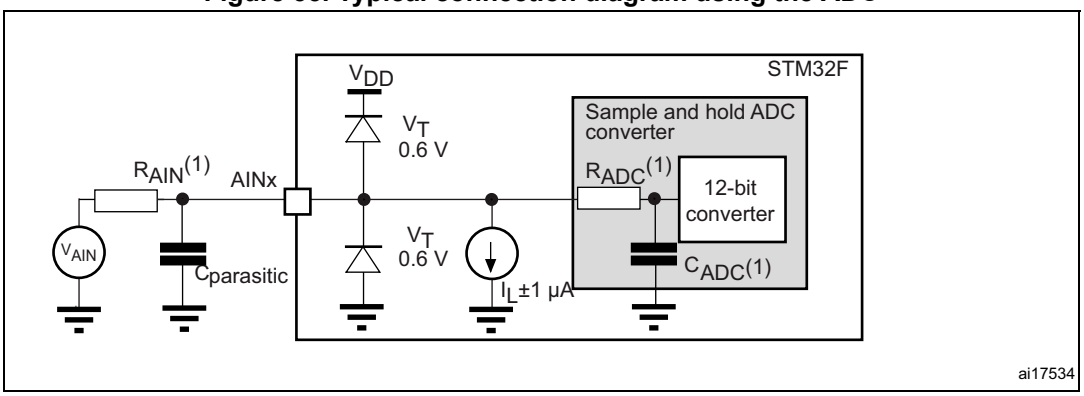
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode, 2.7 V≤V_{DD}≤3.6 V, SPI1,4,5,6,	-	-	45	MHz
		Master mode, 1.71 V≤V_{DD}≤3.6 V, SPI1,4,5,6	-	-	22.5(2)	
		Master transmitter mode, 1.7 V≤V_{DD}≤3.6 V, SPI1,4,5,6	-	-	45	
		Slave full duplex mode, 2.7 V≤V_{DD}≤3.6 V, SPI1,4,5,6	-	-	22.5	
		Slave transmitter mode, 1.71 V≤V_{DD}≤3.6 V, SPI1,4,5,6	-	-	33	
		Slave transmitter mode, 2.7 V≤V_{DD}≤3.6 V, SPI1,4,5,6	-	-	45	
		Slave mode, 1.71 V≤V_{DD}≤3.6 V, SPI2,3	-	-	22.5	
Duty(SCK)	Duty cycle of SPI clock frequency	Slave mode	30	50	70	%

Figure 54. ADC accuracy characteristics



1. See also *Table 78*.
2. Example of an actual transfer curve.
3. Ideal transfer curve.
4. End point correlation line.
5. E_T = Total Unadjusted Error: maximum deviation between the actual and the ideal transfer curves.
   EO = Offset Error: deviation between the first actual transition and the first ideal one.
   EG = Gain Error: deviation between the last ideal transition and the last actual one.
   ED = Differential Linearity Error: maximum deviation between actual steps and the ideal one.
   EL = Integral Linearity Error: maximum deviation between any actual transition and the end point correlation line.

Figure 55. Typical connection diagram using the ADC



1. Refer to *Table 76* for the values of R_{AIN}, R_{ADC} and C_{ADC}.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 5 pF). A high $C_{parasitic}$ value downgrades conversion accuracy. To remedy this, f_{ADC} should be reduced.

Table 92. Asynchronous multiplexed PSRAM/NOR read timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$3T_{HCLK} - 1$	$3T_{HCLK}+0.5$	ns
$t_{v(NOE\_NE)}$	FMC_NEx low to FMC_NOE low	$2T_{HCLK} - 0.5$	$2T_{HCLK}$	
$t_{tw(NOE)}$	FMC_NOE low time	$T_{HCLK} - 1$	$T_{HCLK}+1$	
$t_{h(NE\_NOE)}$	FMC_NOE high to FMC_NE high hold time	1	-	
$t_{v(A\_NE)}$	FMC_NEx low to FMC_A valid	-	2	
$t_{v(NADV\_NE)}$	FMC_NEx low to FMC_NADV low	0	2	
$t_{w(NADV)}$	FMC_NADV low time	$T_{HCLK} - 0.5$	$T_{HCLK}+0.5$	
$t_{h(AD\_NADV)}$	FMC_AD(address) valid hold time after FMC_NADV high)	0	-	
$t_{h(A\_NOE)}$	Address hold time after FMC_NOE high	$T_{HCLK} - 0.5$	-	
$t_{h(BL\_NOE)}$	FMC_BL time after FMC_NOE high	0	-	
$t_{v(BL\_NE)}$	FMC_NEx low to FMC_BL valid	-	2	
$t_{su(Data\_NE)}$	Data to FMC_NEx high setup time	$T_{HCLK}+1.5$	-	
$t_{su(Data\_NOE)}$	Data to FMC_NOE high setup time	$T_{HCLK}+1$	-	
$t_{h(Data\_NE)}$	Data hold time after FMC_NEx high	0	-	
$t_{h(Data\_NOE)}$	Data hold time after FMC_NOE high	0	-	

1. Based on test during characterization.

Table 93. Asynchronous multiplexed PSRAM/NOR read-NWAIT timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$8T_{HCLK}+0.5$	$8T_{HCLK}+2$	ns
$t_{w(NOE)}$	FMC_NWE low time	$5T_{HCLK} - 1$	$5T_{HCLK} +1.5$	
$t_{su(NWAIT\_NE)}$	FMC_NWAIT valid before FMC_NEx high	$5T_{HCLK} +1.5$	-	
$t_{h(NE\_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	$4T_{HCLK}+1$	-	

1. Based on test during characterization.

Table 95. Asynchronous multiplexed PSRAM/NOR write-NWAIT timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$9T_{HCLK}$	$9T_{HCLK}+0.5$	ns
$t_{w(NWE)}$	FMC_NWE low time	$7T_{HCLK}$	$7T_{HCLK}+2$	
$t_{su(NWAIT\_NE)}$	FMC_NWAIT valid before FMC_NEx high	$6T_{HCLK}+1.5$	-	
$t_{h(NE\_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	$4T_{HCLK}-1$	-	

1. Based on test during characterization.

Synchronous waveforms and timings

Figures *63* through *66* represent synchronous waveforms and *Table 96* through *Table 99* provide the corresponding timings. The results shown in these tables are obtained with the following FMC configuration:

- BurstAccessMode = FMC_BurstAccessMode_Enable;
- MemoryType = FMC_MemoryType_CRAM;
- WriteBurst = FMC_WriteBurst_Enable;
- CLKDivision = 1;
- DataLatency = 1 for NOR Flash; DataLatency = 0 for PSRAM
- C_L = 30 pF on data and address lines. C_L = 10 pF on FMC_CLK unless otherwise specified.

In all timing tables, the T_{HCLK} is the HCLK clock period:

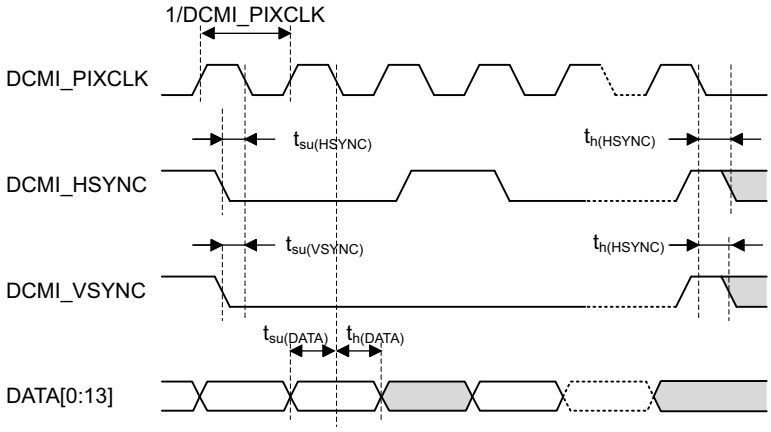
- For 2.7 V≤ V_{DD}≤ 3.6 V, maximum FMC_CLK = 90 MHz at C_L = 30 pF (on FMC_CLK).
- For 1.71 V≤ V_{DD}<1.9 V, maximum FMC_CLK = 60 MHz at C_L = 10 pF (on FMC_CLK).

Table 108. DCMI characteristics(1)

Symbol	Parameter	Min	Max	Unit
-	Frequency ratio DCMI_PIXCLK/f_{HCLK}	-	0.4	-
DCMI_PIXCLK	Pixel clock input	-	54	MHz
D_{Pixel}	Pixel clock input duty cycle	30	70	%
$t_{su(DATA)}$	Data input setup time	4	-	ns
$t_{h(DATA)}$	Data input hold time	1	-	
$t_{su(HSYNC)}$ $t_{su(VSYNC)}$	DCMI_HSYNC/DCMI_VSYNC input setup time	3.5	-	
$t_{h(HSYNC)}$ $t_{h(VSYNC)}$	DCMI_HSYNC/DCMI_VSYNC input hold time	0	-	

1. 1.Guaranteed based on test during characterization.

Figure 75. DCMI timing diagram



5.3.32 LCD-TFT controller (LTDC) characteristics

Unless otherwise specified, the parameters given in *Table 109* for LCD-TFT are derived from tests performed under the ambient temperature, f_{HCLK} frequency and VDD supply voltage summarized in *Table 17*, with the following configuration:

- LCD_CLK polarity: high
- LCD_DE polarity: low
- LCD_VSYNC and LCD_HSYNC polarity: high
- Pixel formats: 24 bits
- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load C_L = 30 pF
- Measurement points are done at CMOS levels: 0.5 V_{DD}

Figure 79. SD default mode

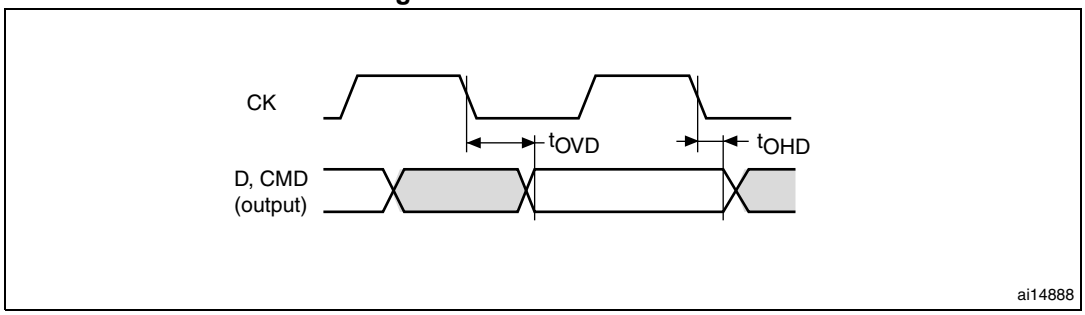


Table 110. Dynamic characteristics: SD / MMC characteristics, V_{DD} = 2.7 to 3.6 V(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PP}	Clock frequency in data transfer mode	-	0	-	50	MHz
-	SDIO_CK/fPCLK2 frequency ratio	-	-	-	8/3	-
$t_{W(CKL)}$	Clock low time	f_{pp} =50 MHz	9.5	10.5	-	ns
$t_{W(CKH)}$	Clock high time		8.5	9.5	-	
CMD, D inputs (referenced to CK) in MMC and SD HS mode						
t_{ISU}	Input setup time HS	f_{pp} =50 MHz	2.0	-	-	ns
t_{IH}	Input hold time HS		2.0	-	-	
CMD, D outputs (referenced to CK) in MMC and SD HS mode						
t_{OV}	Output valid time HS	f_{pp} =50 MHz	-	13	13.5	ns
t_{OH}	Output hold time HS		12.5	-	-	
CMD, D inputs (referenced to CK) in SD default mode						
t_{ISUD}	Input setup time SD	f_{pp} =25 MHz	2.0	-	-	ns
t_{IHD}	Input hold time SD		2.5	-	-	
CMD, D outputs (referenced to CK) in SD default mode						
t_{OVD}	Output valid default time SD	f_{pp} =25 MHz	-	1.5	2.0	ns
t_{OHD}	Output hold default time SD		1.0	-	-	

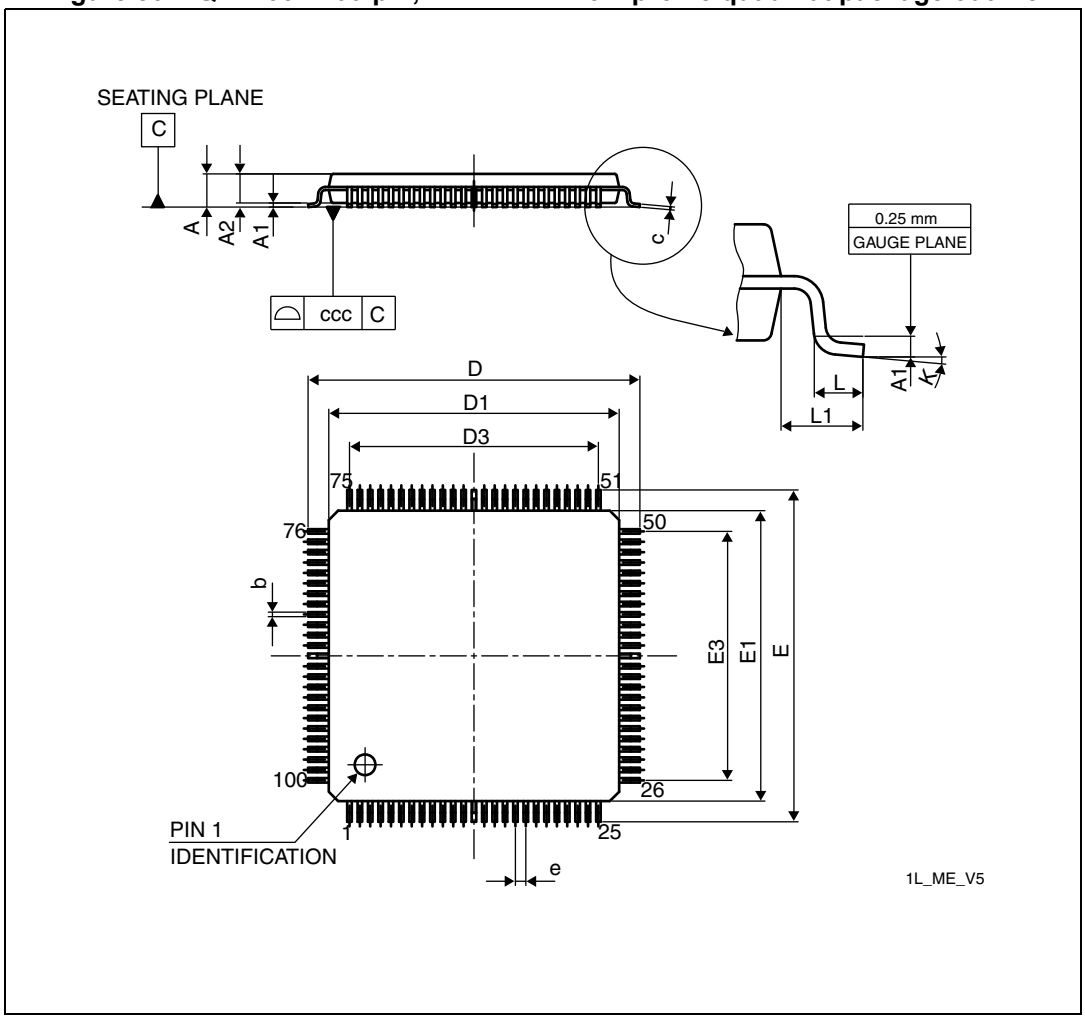
1. Guaranteed based on test during characterization.

6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com.* ECOPACK® is an ST trademark.

6.1 LQFP100 package information

Figure 80. LQFP100 - 100-pin, 14 x 14 mm low-profile quad flat package outline



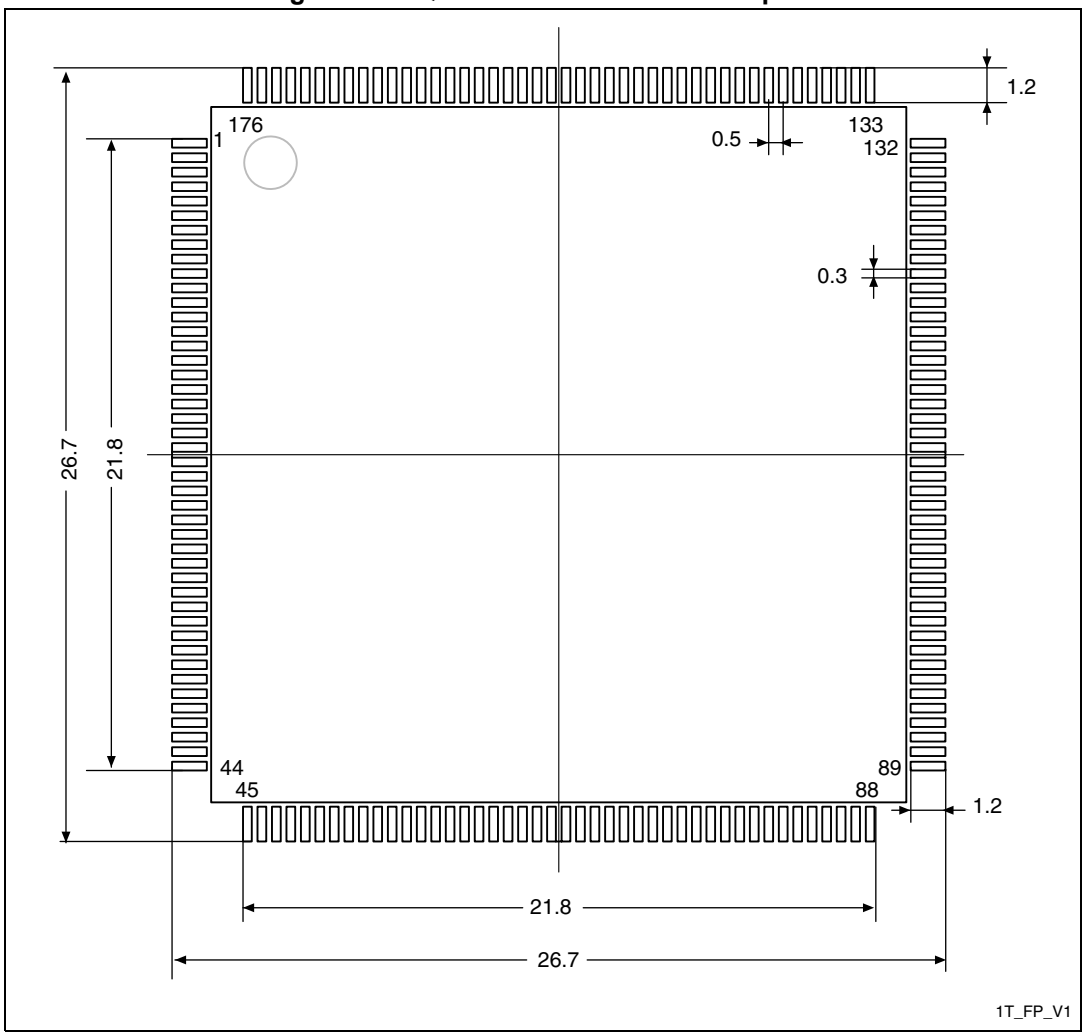
1. Drawing is not to scale.

Table 117. LQFP176, 24 x 24 mm, 176-pin low-profile quad flat package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
e	-	0.500	-	-	0.0197	-
HD	25.900	-	26.100	1.0200	-	1.0276
HE	25.900	-	26.100	1.0200	-	1.0276
L	0.450	-	0.750	0.0177	-	0.0295
L1	-	1.000	-	-	0.0394	-
ZD	-	1.250	-	-	0.0492	-
ZE	-	1.250	-	-	0.0492	-
ccc	-	-	0.080	-	-	0.0031
k	0 °	-	7 °	0 °	-	7 °

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 90. LQFP176 recommended footprint



1. Dimensions are expressed in millimeters.

7 Part numbering

Table 123. Ordering information scheme

Example: STM32 F 479 V I T 6 xxx

Device family

STM32 = ARM-based 32-bit microcontroller

Product type

F = general-purpose

Device subfamily

479= STM32F479xx, USB OTG FS/HS, camera interface, Ethernet, LCD-TFT, DSIHost, cryptographic acceleration, Quad-SPI, Chrom-ART graphical accelerator.

Pin count

V = 100 pins

Z = 144 pins

A = 168 and 169 pins

I = 176 pins

B = 208 pins

N = 216 pins

Flash memory size

G = 1024 Kbytes of Flash memory

I = 2048 Kbytes of Flash memory

Package

T = LQFP

H = BGA

Y = WLCSP

Temperature range

6 = Industrial temperature range, –40 to 85 °C.

7 = Industrial temperature range, –40 to 105 °C.

Options

xxx = programmed parts

TR = tape and reel

For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest ST sales office.