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What is "Embedded - Microcontrollers"?

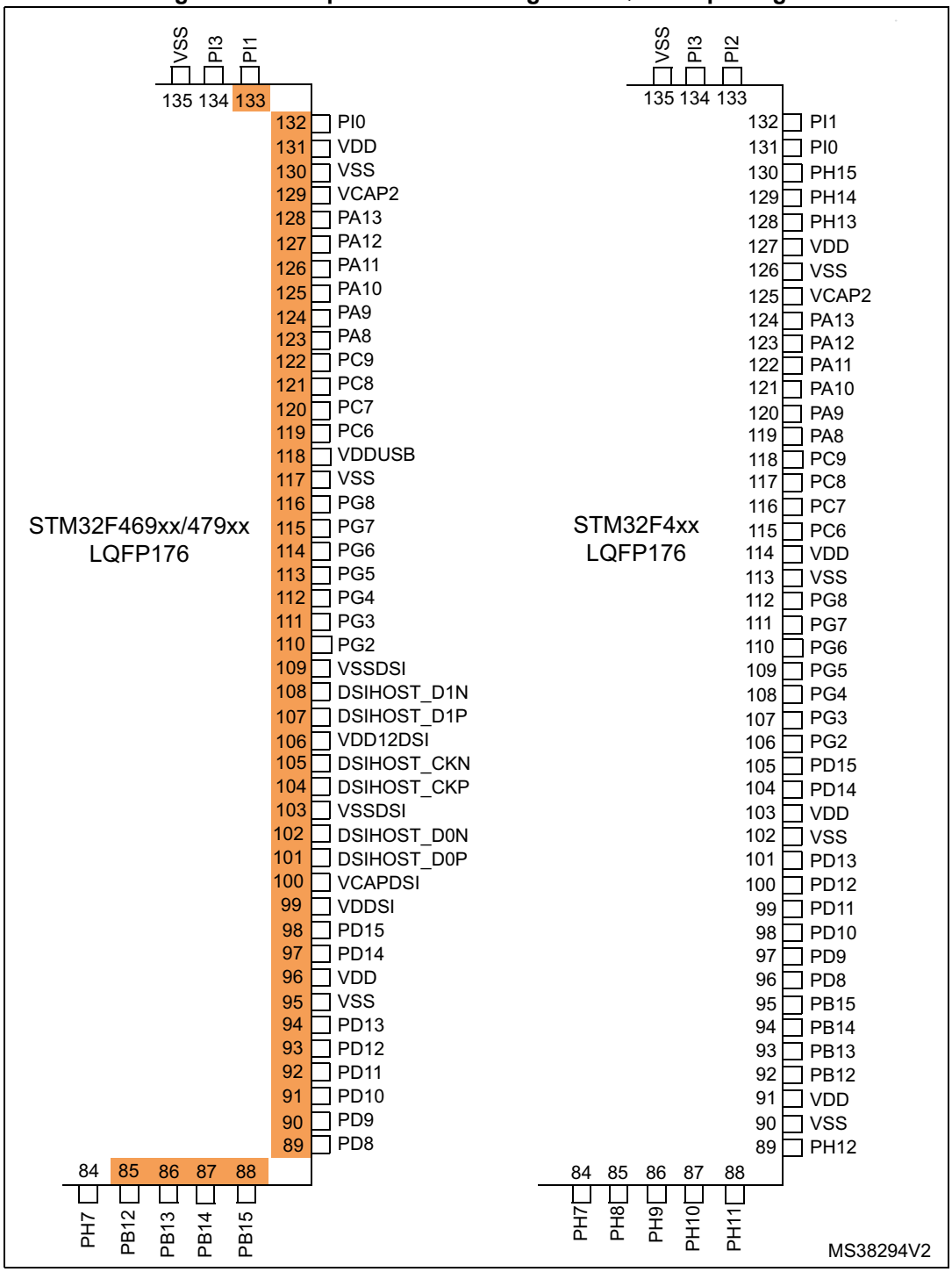
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	180MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, LINbus, SAI, SDIO, SPI, UART/USART, USB, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	161
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	384K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	208-LQFP
Supplier Device Package	208-LQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f479bit6

1.1.1 LQFP176 package

Figure 1. Incompatible board design for LQFP176 package



1. Pins from 85 to 133 are not compatible.

The DMA can be used with the main peripherals:

- SPI and I^2S
- I^2C
- USART
- General-purpose, basic and advanced-control timers TIMx
- DAC
- SDIO
- Camera interface (DCMI)
- ADC
- SAI1
- QUADSPI.

2.9 Flexible Memory Controller (FMC)

The Flexible memory controller (FMC) includes three memory controllers:

- The NOR/PSRAM memory controller
- The NAND/memory controller
- The Synchronous DRAM (SDRAM/Mobile LPSDR SDRAM) controller

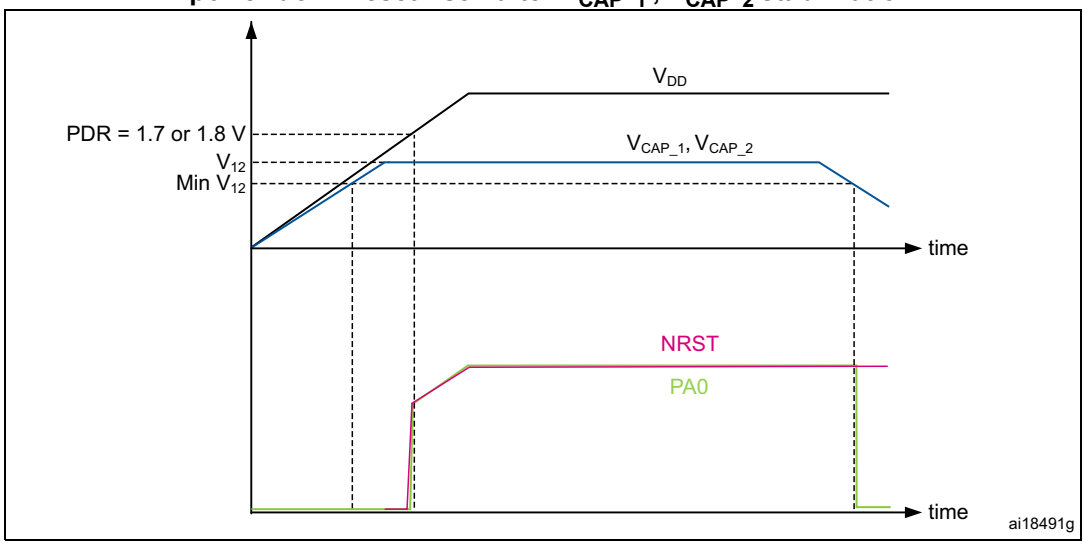
The main features of the FMC controller are the following:

- Interface with static-memory mapped devices including:
  - Static random access memory (SRAM)
  - NOR Flash memory/OneNAND Flash memory
  - PSRAM
  - NAND Flash memory with ECC hardware to check up to 8 Kbytes of data
- Interface with synchronous DRAM (SDRAM/Mobile LPSDR SDRAM) memories
- 8-,16-,32-bit data bus width
- Independent Chip Select control for each memory bank
- Independent configuration for each memory bank
- Write FIFO
- Read FIFO for SDRAM controller
- The Maximum FMC_CLK/FMC_SDCLK frequency for synchronous accesses is HCLK/2.

LCD parallel interface

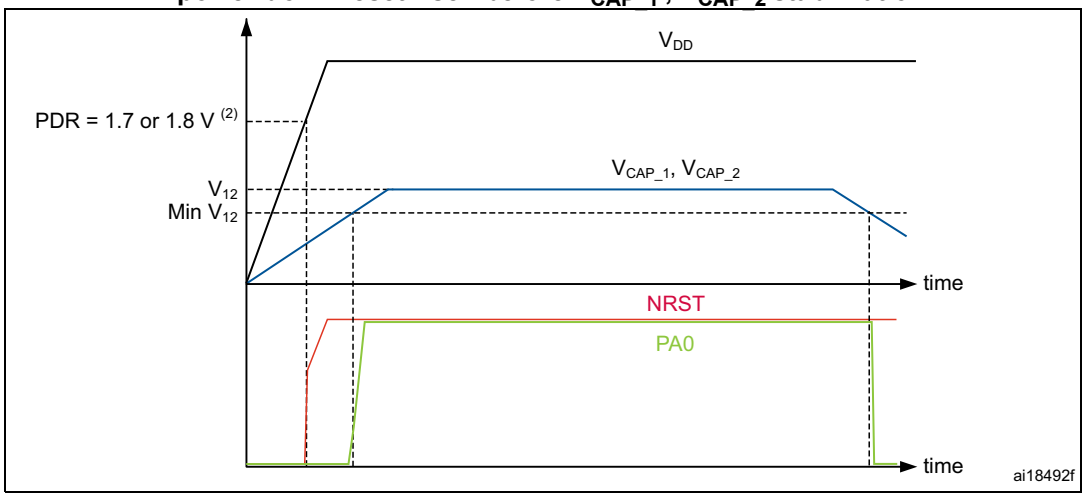
The FMC can be configured to interface seamlessly with most graphic LCD controllers. It supports the Intel 8080 and Motorola 6800 modes, and is flexible enough to adapt to specific LCD interfaces. This LCD parallel interface capability makes it easy to build cost effective graphic applications using LCD modules with embedded controllers or high performance solutions using external controllers with dedicated acceleration.

Figure 11. Startup in regulator OFF: slow V_{DD} slope - power-down reset risen after V_{CAP_1}, V_{CAP_2} stabilization



1. This figure is valid whatever the internal reset mode (ON or OFF).

Figure 12. Startup in regulator OFF mode: fast V_{DD} slope - power-down reset risen before V_{CAP_1}, V_{CAP_2} stabilization



1. This figure is valid whatever the internal reset mode (ON or OFF).

2.20.3 Regulator ON/OFF and internal reset ON/OFF availability

Table 4. Regulator ON/OFF and internal reset ON/OFF availability

Package	Regulator ON	Regulator OFF	Internal reset ON	Internal reset OFF
WLCSP168 UFBGA169 LQFP208	Yes	No	Yes PDR_ON set to V_{DD}	Yes PDR_ON set to V_{SS}
LQFP176 UFBGA176 TFBGA216	Yes BYPASS_REG set to V_{SS}	Yes BYPASS_REG set to V_{DD}		

USART1, USART2, USART3 and USART6 also provide hardware management of the CTS and RTS signals, Smart Card mode (ISO 7816 compliant) and SPI-like communication capability. All interfaces can be served by the DMA controller.

Table 8. USART feature comparison(1)

Name	Standard features	Modem (RTS/CTS)	LIN	SPI master	irDA	Smartcard (ISO 7816)	Max. baud rate in Mbit/s		APB mapping
							Oversampling by 16	Oversampling by 8	
USART1	X	X	X	X	X	X	5.62	11.25	APB2 (max. 90 MHz)
USART2	X	X	X	X	X	X	2.81	5.62	APB1 (max. 45 MHz)
USART3	X	X	X	X	X	X	2.81	5.62	APB1 (max. 45 MHz)
UART4	X	-	X	-	X	-	2.81	5.62	APB1 (max. 45 MHz)
UART5	X	-	X	-	X	-	2.81	5.62	APB1 (max. 45 MHz)
USART6	X	X	X	X	X	X	5.62	11.25	APB2 (max. 90 MHz)
UART7	X	-	X	-	X	-	2.81	5.62	APB1 (max. 45 MHz)
UART8	X	-	X	-	X	-	2.81	5.62	APB1 (max. 45 MHz)

1. X = feature supported.

2.27 Serial peripheral interface (SPI)

The devices feature up to six SPIs in slave and master modes in full-duplex and simplex communication modes. SPI1, SPI4, SPI5, and SPI6 can communicate at up to 45 Mbits/s, SPI2 and SPI3 can communicate at up to 22.5 Mbit/s. The 3-bit prescaler gives 8 master mode frequencies and the frame is configurable to 8 bits or 16 bits. The hardware CRC generation/verification supports basic SD Card/MMC modes. All SPIs can be served by the DMA controller.

The SPI interface can be configured to operate in TI mode for communications in master mode and slave mode.

Table 10. STM32F479xx pin and ball definitions (continued)

Pin number								Pin name (function after reset)(1)	Pin types	I/O structures	Notes	Alternate functions	Additional functions
LQFP100	LQFP144	UFBGA169	WLCSP168	UFBGA176	LQFP176	LQFP208	TFBGA216						
-	-	L3	K8	J4	46	49	J3	PH5	I/O	FT	-	I2C2_SDA, SPI5_NSS, FMC_SDNWE, EVENTOUT	-
22	32	K3	N10	R2	47	50	R2	PA3	I/O	FT	(5)	TIM2_CH4, TIM5_CH4, TIM9_CH2, USART2_RX, LCD_B2, OTG_HS_ULPI_D0, ETH_MII_COL, LCD_B5, EVENTOUT	ADC123_IN3
23	33	J1	N11	-	-	51	K6	VSS	S	-	-	-	-
-	-	-	-	L4	48	-	L5	BYPASS_REG	I	FT	-	-	-
24	34	J4	P12	K4	49	52	K5	VDD	S	-	-	-	-
25	35	N2	M9	N4	50	53	N4	PA4	I/O	TTa	-	SPI1_NSS, SPI3_NSS/I2S3_WS, USART2_CK, OTG_HS_SOF, DCMI_HSYNC, LCD_VSYNC, EVENTOUT	ADC12_IN4, DAC_OUT1
26	36	M3	L8	P4	51	54	P4	PA5	I/O	TTa	-	TIM2_CH1/TIM2_ETR, TIM8_CH1N, SPI1_SCK, OTG_HS_ULPI_CK, LCD_R4, EVENTOUT	ADC12_IN5, DAC_OUT2
27	37	N3	P11	P3	52	55	P3	PA6	I/O	FT	(5)	TIM1_BKIN, TIM3_CH1, TIM8_BKIN, SPI1_MISO, TIM13_CH1, DCMI_PIXCLK, LCD_G2, EVENTOUT	ADC12_IN6
28	38	K4	J8	R3	53	56	R3	PA7	I/O	FT	(5)	TIM1_CH1N, TIM3_CH2, TIM8_CH1N, SPI1_MOSI, TIM14_CH1, QUADSPI_CLK, ETH_MII_RX_DV/ETH_RMII_CRS_DV, FMC_SDNWE, EVENTOUT	ADC12_IN7
NC (2)	39	-	-	N5	54	57	N5	PC4	I/O	FT	(5)	ETH_MII_RXD0/ETH_RMII_RXD0, FMC_SDNE0, EVENTOUT	ADC12_IN14
NC (2)	40	-	-	P5	55	58	P5	PC5	I/O	FT	(5)	ETH_MII_RXD1/ETH_RMII_RXD1, FMC_SDCKE0, EVENTOUT	ADC12_IN15
-	-	-	-	-	-	59	L7	VDD	S	-	-	-	-
-	-	-	-	-	-	60	L6	VSS	S	-	-	-	-
29	41	N4	P10	R5	56	61	R5	PB0	I/O	FT	(5)	TIM1_CH2N, TIM3_CH3, TIM8_CH2N, LCD_R3, OTG_HS_ULPI_D1, ETH_MII_RXD2, LCD_G1, EVENTOUT	ADC12_IN8

Table 10. STM32F479xx pin and ball definitions (continued)

Pin number								Pin name (function after reset)(1)	Pin types	I/O structures	Notes	Alternate functions	Additional functions
LQFP100	LQFP144	UFBGA169	WLCSP168	UFBGA176	LQFP176	LQFP208	TFBGA216						
30	42	K5	N9	R4	57	62	R4	PB1	I/O	FT	(5)	TIM1_CH3N, TIM3_CH4, TIM8_CH3N, LCD_R6, OTG_HS_ULPI_D2, ETH_MII_RXD3, LCD_G0, EVENTOUT	ADC12_IN9
31	43	L5	P9	M6	58	63	M5	PB2-BOOT1(PB2)	I/O	FT	-	EVENTOUT	-
-	-	-	-	-	-	64	G4	PI15	I/O	FT	-	LCD_G2, LCD_R0, EVENTOUT	-
-	-	-	-	-	-	65	R6	PJ0	I/O	FT	-	LCD_R7, LCD_R1, EVENTOUT	-
-	-	-	-	-	-	66	R7	PJ1	I/O	FT	-	LCD_R2, EVENTOUT	-
-	-	-	-	-	-	67	P7	PJ2	I/O	FT	-	DSIHOST_TE, LCD_R3, EVENTOUT	-
-	-	-	-	-	-	68	N8	PJ3	I/O	FT	-	LCD_R4, EVENTOUT	-
-	-	-	-	-	-	69	M9	PJ4	I/O	FT	-	LCD_R5, EVENTOUT	-
-	44	M5	K7	R6	59	70	P8	PF11	I/O	FT	-	SPI5_MOSI, FMC_SDNRAS, DCMI_D12, EVENTOUT	-
-	45	N5	M8	P6	60	71	M6	PF12	I/O	FT	-	FMC_A6, EVENTOUT	-
-	-	J6	N8	M8	61	72	K7	VSS	S	-	-	-	-
-	46	K6	P8	N8	62	73	L8	VDD	S	-	-	-	-
-	47	M4	J7	N6	63	74	N6	PF13	I/O	FT	-	FMC_A7, EVENTOUT	-
-	48	H5	L7	R7	64	75	P6	PF14	I/O	FT	-	FMC_A8, EVENTOUT	-
-	49	M6	H8	P7	65	76	M8	PF15	I/O	FT	-	FMC_A9, EVENTOUT	-
-	50	N6	J6	N7	66	77	N7	PG0	I/O	FT	-	FMC_A10, EVENTOUT	-
-	51	M7	P7	M7	67	78	M7	PG1	I/O	FT	-	FMC_A11, EVENTOUT	-
32	52	N7	N7	R8	68	79	R8	PE7	I/O	FT	-	TIM1_ETR, UART7_Rx, QUADSPI_BK2_IO0, FMC_D4, EVENTOUT	-
33	53	G6	M7	P8	69	80	N9	PE8	I/O	FT	-	TIM1_CH1N, UART7_Tx, QUADSPI_BK2_IO1, FMC_D5, EVENTOUT	-
34	54	H6	K6	P9	70	81	P9	PE9	I/O	FT	-	TIM1_CH1, QUADSPI_BK2_IO2, FMC_D6, EVENTOUT	-
-	55	J7	-	M9	71	82	K8	VSS	S	-	-	-	-
-	56	L6	-	N9	72	83	L9	VDD	S	-	-	-	-
35	57	H7	P6	R9	73	84	R9	PE10	I/O	FT	-	TIM1_CH2N, QUADSPI_BK2_IO3, FMC_D7, EVENTOUT	-

Table 10. STM32F479xx pin and ball definitions (continued)

Pin number								Pin name (function after reset)(1)	Pin types	I/O structures	Notes	Alternate functions	Additional functions
LQFP100	LQFP144	UFBGA169	WLCSP168	UFBGA176	LQFP176	LQFP208	TFBGA216						
96	136	B4	A9	B5	165	196	B5	PB7	I/O	FT	-	TIM4_CH2, I2C1_SDA, USART1_RX, FMC_NL, DCMI_VSYNC, EVENTOUT	-
97	137	A5	F8	D6	166	197	E6	BOOT0	I	B	-	-	VPP
98	138	D4	B9	A5	167	198	A7	PB8	I/O	FT	-	TIM4_CH3, TIM10_CH1, I2C1_SCL, CAN1_RX, ETH_MII_TXD3, SDIO_D4, DCMI_D6, LCD_B6, EVENTOUT	-
99	139	C4	E9	B4	168	199	B4	PB9	I/O	FT	-	TIM4_CH4, TIM11_CH1, I2C1_SDA, SPI2_NSS/I2S2_WS, CAN1_TX, SDIO_D5, DCMI_D7, LCD_B7, EVENTOUT	-
NC (2)	140	A4	A10	A4	169	200	A6	PE0	I/O	FT	-	TIM4_ETR, UART8_Rx, FMC_NBL0, DCMI_D2, EVENTOUT	-
NC (2)	141	A3	C9	A3	170	201	A5	PE1	I/O	FT	-	UART8_Tx, FMC_NBL1, DCMI_D3, EVENTOUT	-
-	-	E3	B10	D5	-	202	F6	VSS	S	-	-	-	-
-	142	C3	D9	C6	171	203	E5	PDR_ON	S	-	-	-	-
100	143	D3	A11	C5	172	204	E7	VDD	S	-	-	-	-
-	-	B3	D10	D4	173	205	C3	PI4	I/O	FT	-	TIM8_BKIN, FMC_NBL2, DCMI_D5, LCD_B4, EVENTOUT	-
-	-	A2	C10	C4	174	206	D3	PI5	I/O	FT	-	TIM8_CH1, FMC_NBL3, DCMI_VSYNC, LCD_B5, EVENTOUT	-
-	-	A1	B11	C3	175	207	D6	PI6	I/O	FT	-	TIM8_CH2, FMC_D28, DCMI_D6, LCD_B6, EVENTOUT	-
-	-	B1	A12	C2	176	208	D4	PI7	I/O	FT	-	TIM8_CH3, FMC_D29, DCMI_D7, LCD_B7, EVENTOUT	-

1. **Function availability depends on the chosen device.**
2. NC (not-connected) pins are not bonded. They must be configured by software to output push-pull and forced to “0” in the output data register to avoid extra current consumption in low power modes.
3. PC13, PC14, PC15 and PI8 are supplied through the power switch. Since the switch only sinks a limited amount of current (3 mA), the use of GPIOs PC13 to PC15 and PI8 in output mode is limited:
   - The speed should not exceed 2 MHz with a maximum load of 30 pF.
   - These I/Os must not be used as a current source (e.g. to drive an LED).
4. Main function after the first backup domain power-up. Later on, it depends on the contents of the RTC registers even after reset (because these registers are not reset by the main reset). For details on how to manage these I/Os, refer to the RTC register description sections in the STM32F4xx reference manual, available from the STMicroelectronics website: www.st.com.
5. FT = 5 V tolerant except when in analog mode or oscillator mode (for PC14, PC15, PH0 and PH1).

Table 11. FMC pin definition (continued)

Pin name	NOR/PSRAM/SRAM	NOR/PSRAM Mux	NAND16	SDRAM
PF8	-	-	-	-
PF9	-	-	-	-
PF10	-	-	-	-
PG6	-	-	-	-
PG7	-	-	INT	-
PE0	NBL0	NBL0	-	NBL0
PE1	NBL1	NBL1	-	NBL1
PI4	NBL2	-	-	NBL2
PI5	NBL3	-	-	NBL3
PG8	-	-	-	SDCLK
PC0	-	-	-	SDNWE
PF11	-	-	-	SDNRAS
PG15	-	-	-	SDNCAS
PH2	-	-	-	SDCKE0
PH3	-	-	-	SDNE0
PH6	-	-	-	SDNE1
PH7	-	-	-	SDCKE1
PH5	-	-	-	SDNWE
PC2	-	-	-	SDNE0
PC3	-	-	-	SDCKE0
PB5	-	-	-	SDCKE1
PB6	-	-	-	SDNE1

Table 26. Typical and maximum current consumption in Run mode, code with data processing running from Flash memory (ART accelerator enabled except prefetch), regulator OFF

Symbol	Parameter	Conditions	f_{HCLK} (MHz)	Typ		Max(1)						Unit
				I_{DD12}	I_{DD}	T_A = 25 °C		T_A = 85 °C		T_A = 105 °C		
						I_{DD12}	I_{DD}	I_{DD12}	I_{DD}	I_{DD12}	I_{DD}	
I_{DD12} / I_{DD}	Supply current in RUN mode from V_{12} and V_{DD} supply	All Peripherals enabled(2) (3)	168	93	1	98	1	123	1	148	1	mA
			150	83	1	88	1	113	1	138	1	
			144	76	1	80	1	103	1	126	1	
			120	56	1	59	1	78	1	97	1	
			90	43	1	45	1	64	1	83	1	
			60	29	1	32	1	50	1	70	1	
			30	15	1	18	1	36	1	56	1	
			25	13	1	15	1	34	1	53	1	
		All Peripherals disabled	168	44	1	50	1	72	1	94	1	
			150	40	1	45	1	68	1	90	1	
			144	36	1	40	1	62	1	82	1	
			120	27	1	30	1	48	1	66	1	
			90	20	1	23	1	41	1	60	1	
			60	14	1	16	1	35	1	53	1	
			30	8	1	10	1	28	1	47	1	
			25	7	1	9	1	27	1	46	1	

1. Guaranteed based on test during characterization.
2. When analog peripheral blocks such as ADCs, DACs, HSE, LSE, HSI, or LSI are ON, DSI regulator, an additional power consumption should be considered.
3. When the ADC is ON (ADON bit set in the ADC_CR2 register), add an additional power consumption of 1.6 mA per ADC for the analog part.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers...)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device are monitored while a simple application, executing EEMBC? code, is running. This emission test is compliant with SAE IEC61967-2 standard which specifies the test board and the pin loading.

Table 54. EMI characteristics

Symbol	Parameter	Conditions	Monitored frequency band	Max vs. [f_{HSE}/f_{CPU}]		Unit
				8/168 MHz	8/180 MHz	
S_{EMI}	Peak level	V_{DD} = 3.3 V, T_A = 25 °C, TFBGA216 package, conforming to SAE J1752/3 EEMBC, ART ON, all peripheral clocks enabled, clock dithering disabled.	0.1 to 30 MHz	2	2	dBµV
			30 to 130 MHz	4	1	
			130 MHz to 1GHz	10	10	
			SAE EMI Level	3	3	-
		V_{DD} = 3.3 V, T_A = 25 °C, TFBGA216 package, conforming to SAE J1752/3 EEMBC, ART ON, all peripheral clocks enabled, clock dithering enabled	0.1 to 30 MHz	5	-10	dBµV
			30 to 130 MHz	3	-15	
			130 MHz to 1GHz	8	0	
			SAE EMI level	2	2	-

5.3.18 Absolute maximum ratings (electrical sensitivity)

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the ANSI/ESDA/JEDEC JS-001 and ANSI/ESD S5.3.1 standards.

Figure 44. SPI timing diagram - master mode(1)

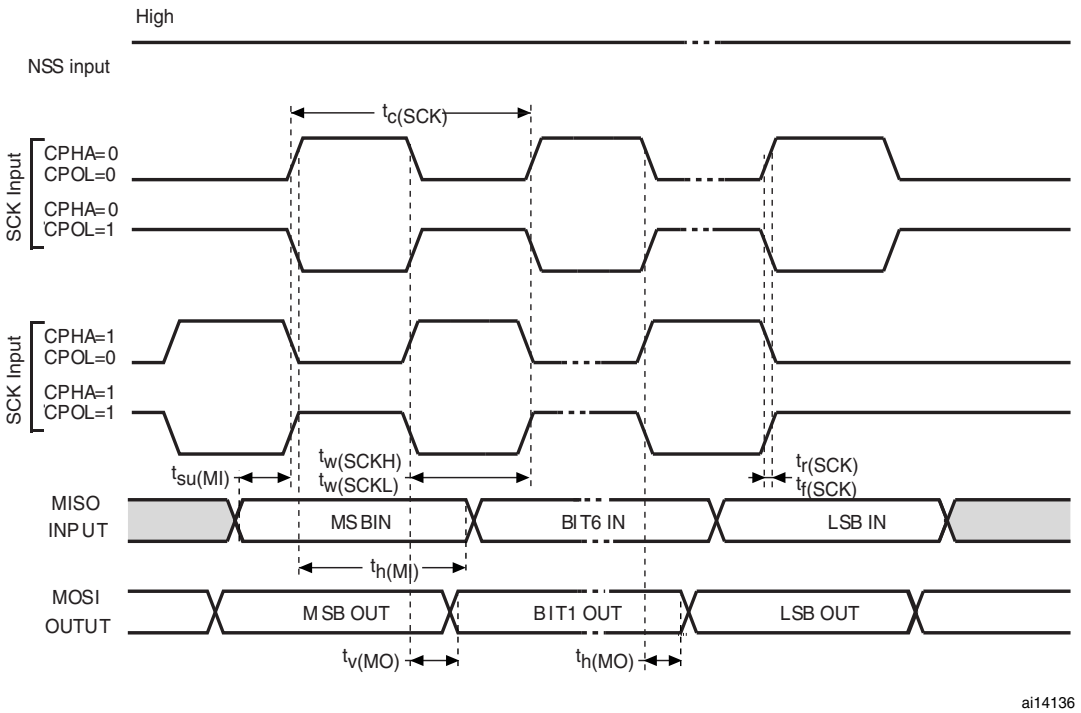


Table 73. Dynamics characteristics: Ethernet MAC signals for SMI(1)

Symbol	Parameter	Min	Typ	Max	Unit
t_{MDC}	MDC cycle time(2.38 MHz)	400	400	403	ns
$T_{d(MDIO)}$	Write data valid time	T_{HCLK} - 1	T_{HCLK}	T_{HCLK} + 1.5	
$t_{su(MDIO)}$	Read data setup time	12.5	-	-	
$t_{h(MDIO)}$	Read data hold time	0	-	-	

1. Guaranteed based on test during characterization.

Table 74 gives the list of Ethernet MAC signals for the RMII and *Figure 52* shows the corresponding timing diagram.

Figure 52. Ethernet RMII timing diagram

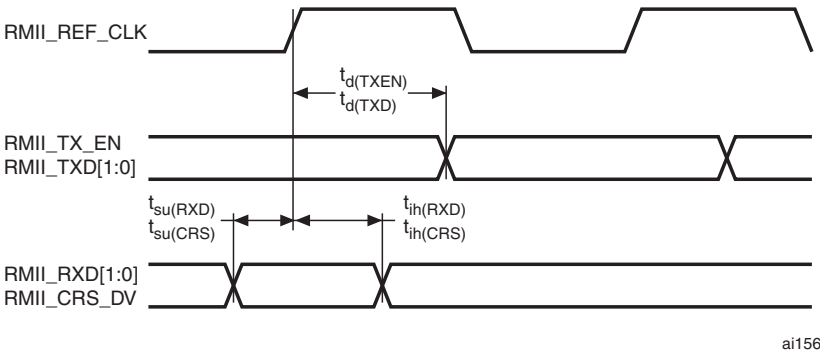
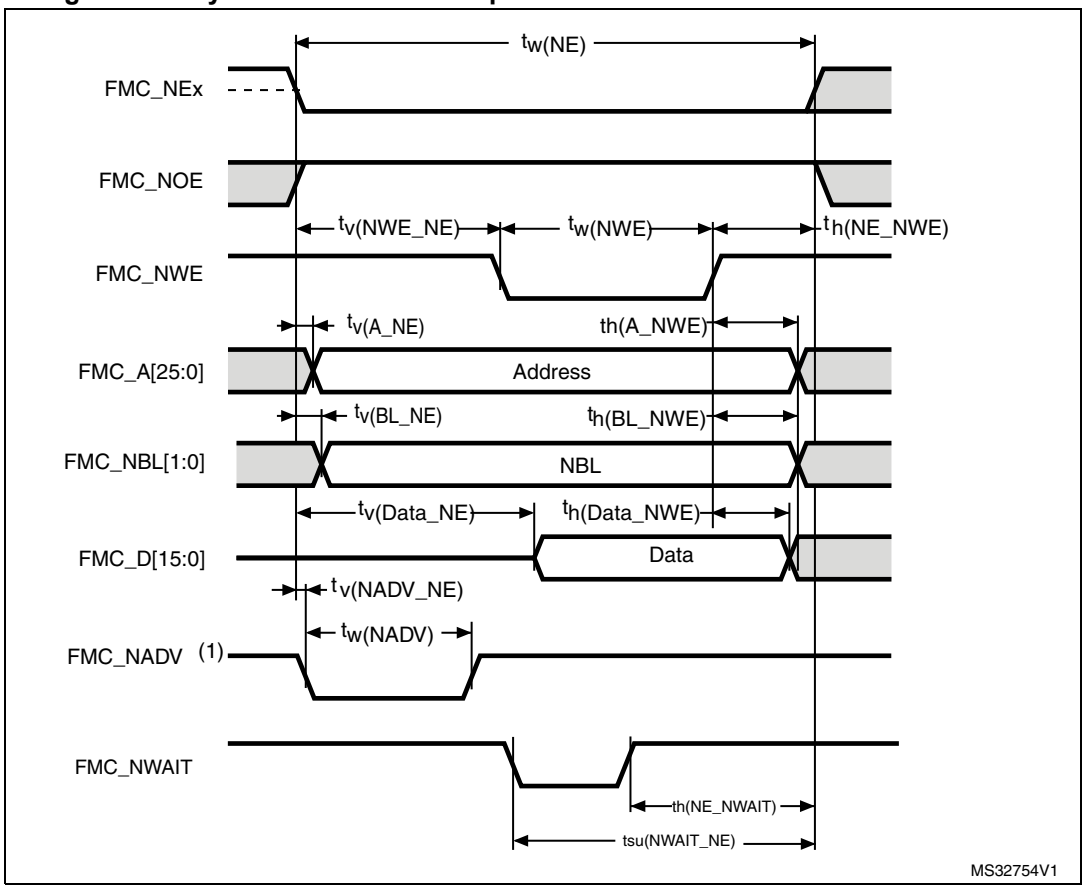


Figure 60. Asynchronous non-multiplexed SRAM/PSRAM/NOR write waveforms



1. Mode 2/B, C and D only. In Mode 1, FMC_NADV is not used.

Table 90. Asynchronous non-multiplexed SRAM/PSRAM/NOR write timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$3T_{HCLK}$	$3T_{HCLK}+1$	ns
$t_{v(NWE\_NE)}$	FMC_NEx low to FMC_NWE low	$T_{HCLK} - 0.5$	$T_{HCLK}+ 0.5$	
$t_{w(NWE)}$	FMC_NWE low time	T_{HCLK}	$T_{HCLK}+ 0.5$	
$t_{h(NE\_NWE)}$	FMC_NWE high to FMC_NE high hold time	T_{HCLK} +1.5	-	
$t_{v(A\_NE)}$	FMC_NEx low to FMC_A valid	-	0	
$t_{h(A\_NWE)}$	Address hold time after FMC_NWE high	T_{HCLK}+0.5	-	
$t_{v(BL\_NE)}$	FMC_NEx low to FMC_BL valid	-	1.5	
$t_{h(BL\_NWE)}$	FMC_BL hold time after FMC_NWE high	T_{HCLK}+0.5	-	
$t_{v(Data\_NE)}$	Data to FMC_NEx low to Data valid	-	$T_{HCLK}+ 2$	
$t_{h(Data\_NWE)}$	Data hold time after FMC_NWE high	T_{HCLK}+0.5	-	
$t_{v(NADV\_NE)}$	FMC_NEx low to FMC_NADV low	-	0.5	
$t_{w(NADV)}$	FMC_NADV low time	-	$T_{HCLK}+ 0.5$	

1. Based on test during characterization.

Table 95. Asynchronous multiplexed PSRAM/NOR write-NWAIT timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$9T_{HCLK}$	$9T_{HCLK}+0.5$	ns
$t_{w(NWE)}$	FMC_NWE low time	$7T_{HCLK}$	$7T_{HCLK}+2$	
$t_{su(NWAIT\_NE)}$	FMC_NWAIT valid before FMC_NEx high	$6T_{HCLK}+1.5$	-	
$t_{h(NE\_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	$4T_{HCLK}-1$	-	

1. Based on test during characterization.

Synchronous waveforms and timings

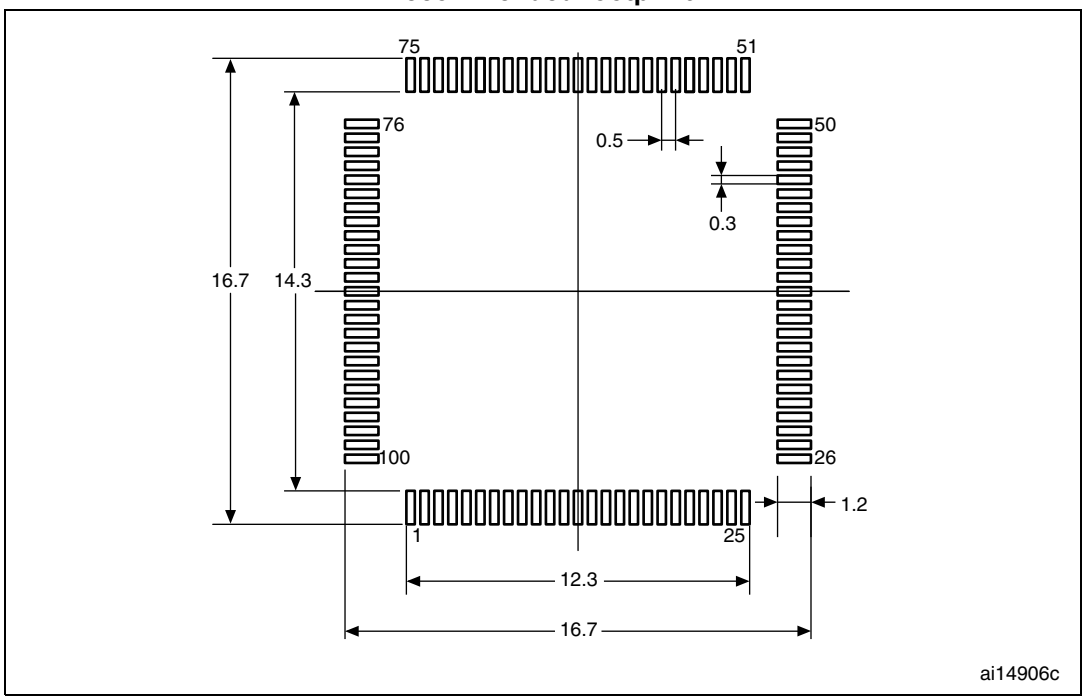
Figures *63* through *66* represent synchronous waveforms and *Table 96* through *Table 99* provide the corresponding timings. The results shown in these tables are obtained with the following FMC configuration:

- BurstAccessMode = FMC_BurstAccessMode_Enable;
- MemoryType = FMC_MemoryType_CRAM;
- WriteBurst = FMC_WriteBurst_Enable;
- CLKDivision = 1;
- DataLatency = 1 for NOR Flash; DataLatency = 0 for PSRAM
- C_L = 30 pF on data and address lines. C_L = 10 pF on FMC_CLK unless otherwise specified.

In all timing tables, the T_{HCLK} is the HCLK clock period:

- For 2.7 V≤ V_{DD}≤ 3.6 V, maximum FMC_CLK = 90 MHz at C_L = 30 pF (on FMC_CLK).
- For 1.71 V≤ V_{DD}<1.9 V, maximum FMC_CLK = 60 MHz at C_L = 10 pF (on FMC_CLK).

Figure 81. LQFP100 - 100-pin, 14 x 14 mm low-profile quad flat recommended footprint

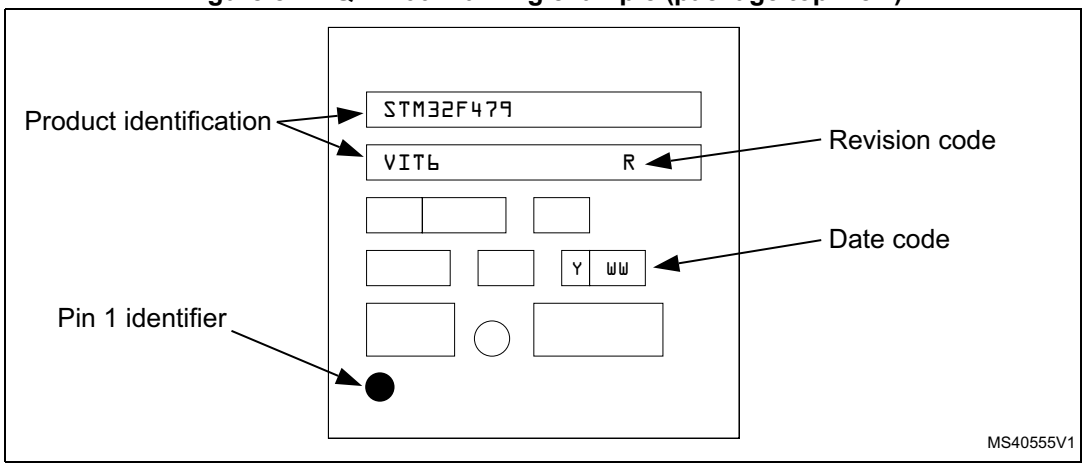


1. Dimensions are expressed in millimeters.

Device Marking for LQFP100

The following figure gives an example of topside marking orientation versus pin 1 identifier location. Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

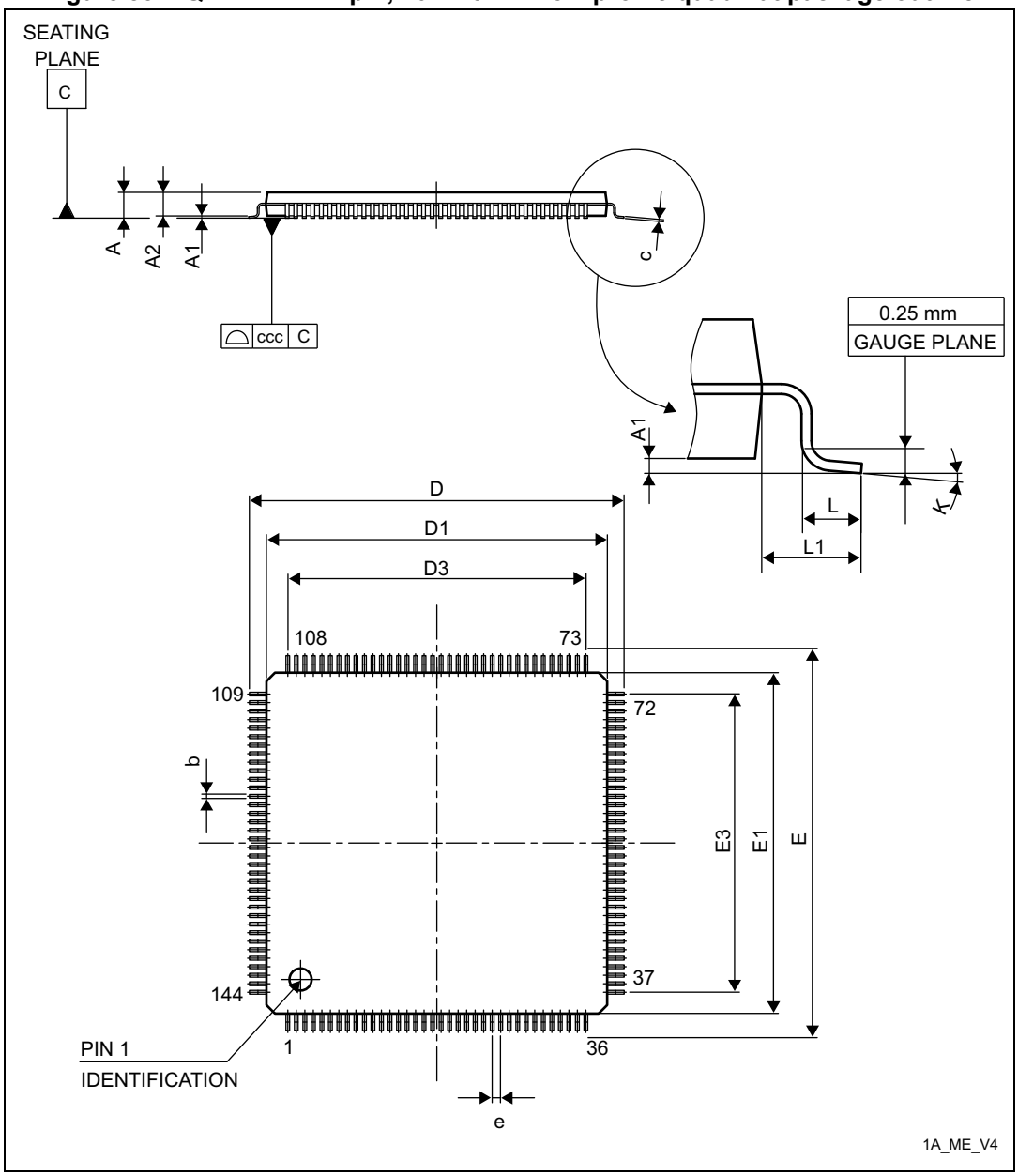
Figure 82. LQFP100 marking example (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

6.2 LQFP144 package information

Figure 83. LQFP144 - 144-pin, 20 x 20 mm low-profile quad flat package outline



1. Drawing is not to scale.

Table 117. LQFP176, 24 x 24 mm, 176-pin low-profile quad flat package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
e	-	0.500	-	-	0.0197	-
HD	25.900	-	26.100	1.0200	-	1.0276
HE	25.900	-	26.100	1.0200	-	1.0276
L	0.450	-	0.750	0.0177	-	0.0295
L1	-	1.000	-	-	0.0394	-
ZD	-	1.250	-	-	0.0492	-
ZE	-	1.250	-	-	0.0492	-
ccc	-	-	0.080	-	-	0.0031
k	0 °	-	7 °	0 °	-	7 °

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 93. UFBGA176+25 - 201-ball, 10 x 10 mm, 0.65 mm pitch, ultra fine pitch ball grid array package recommended footprint

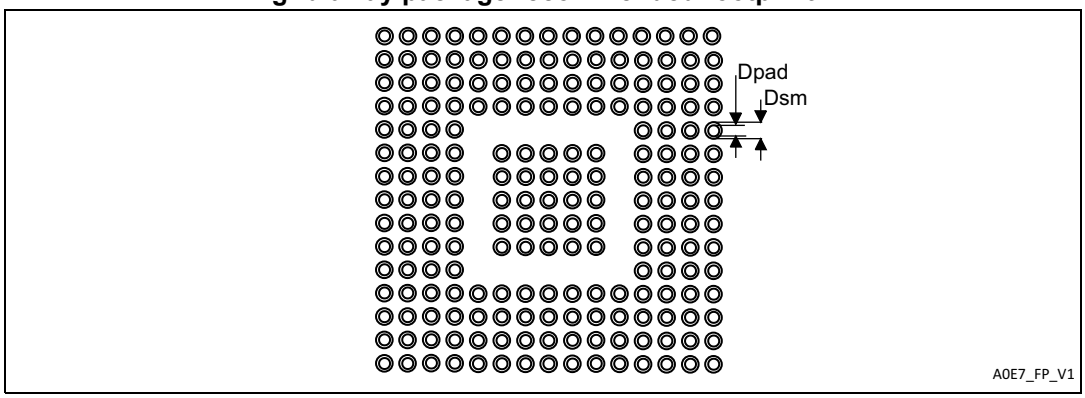


Table 119. UFBGA176+25 recommended PCB design rules (0.65 mm pitch BGA)

Dimension	Recommended values
Pitch	0.65 mm
Dpad	0.300 mm
Dsm	0.400 mm typ. (depends on the soldermask registration tolerance)
Stencil opening	0.300 mm
Stencil thickness	Between 0.100 mm and 0.125 mm
Pad trace width	0.100 mm

7 Part numbering

Table 123. Ordering information scheme

Example: STM32 F 479 V I T 6 xxx

Device family

STM32 = ARM-based 32-bit microcontroller

Product type

F = general-purpose

Device subfamily

479= STM32F479xx, USB OTG FS/HS, camera interface, Ethernet, LCD-TFT, DSIHost, cryptographic acceleration, Quad-SPI, Chrom-ART graphical accelerator.

Pin count

V = 100 pins

Z = 144 pins

A = 168 and 169 pins

I = 176 pins

B = 208 pins

N = 216 pins

Flash memory size

G = 1024 Kbytes of Flash memory

I = 2048 Kbytes of Flash memory

Package

T = LQFP

H = BGA

Y = WLCSP

Temperature range

6 = Industrial temperature range, –40 to 85 °C.

7 = Industrial temperature range, –40 to 105 °C.

Options

xxx = programmed parts

TR = tape and reel

For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest ST sales office.