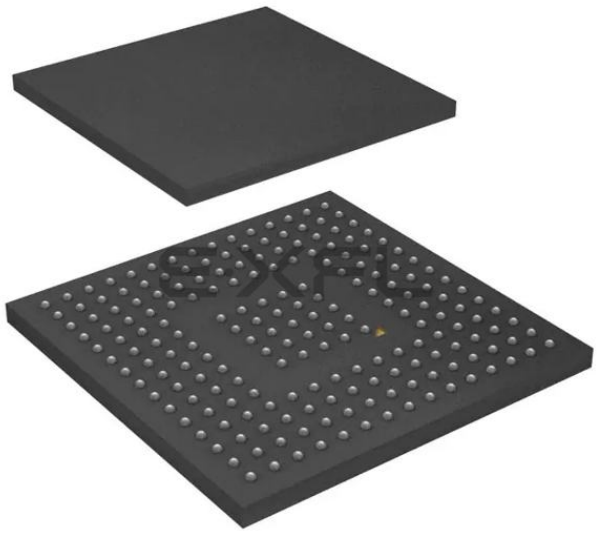

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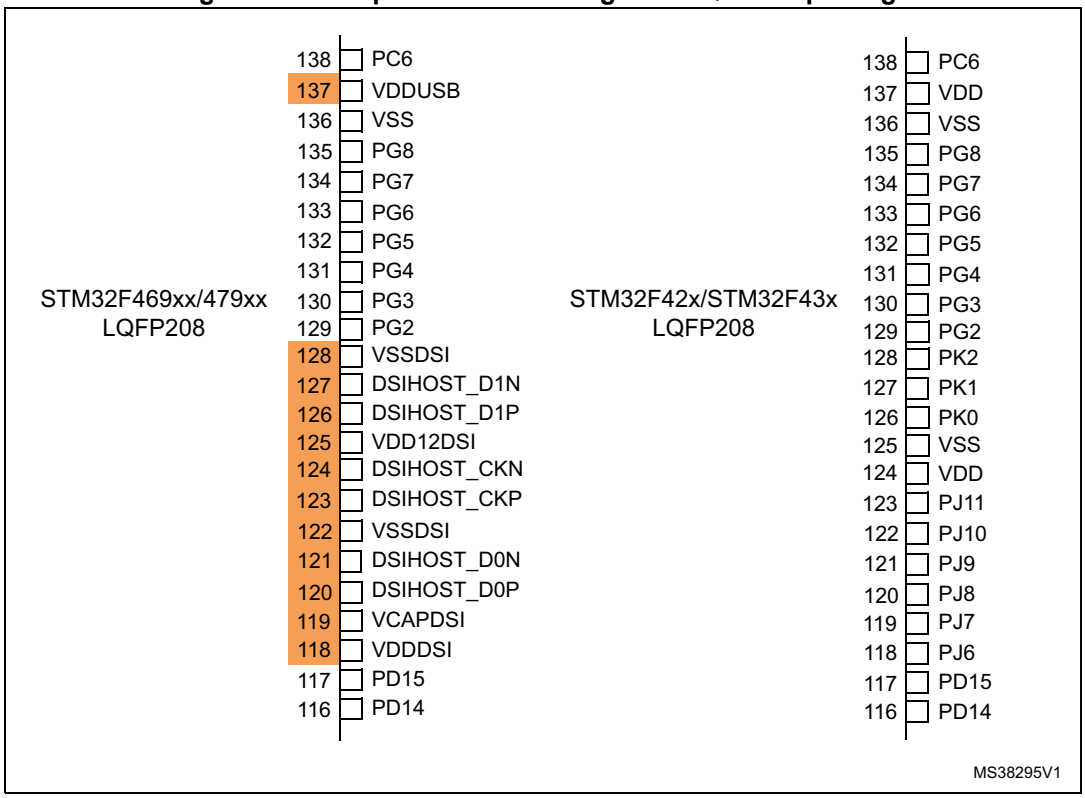
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	180MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, LINbus, SAI, SDIO, SPI, UART/USART, USB, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	131
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	384K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	201-UFBGA
Supplier Device Package	176+25UFBGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f479igh6

Contents

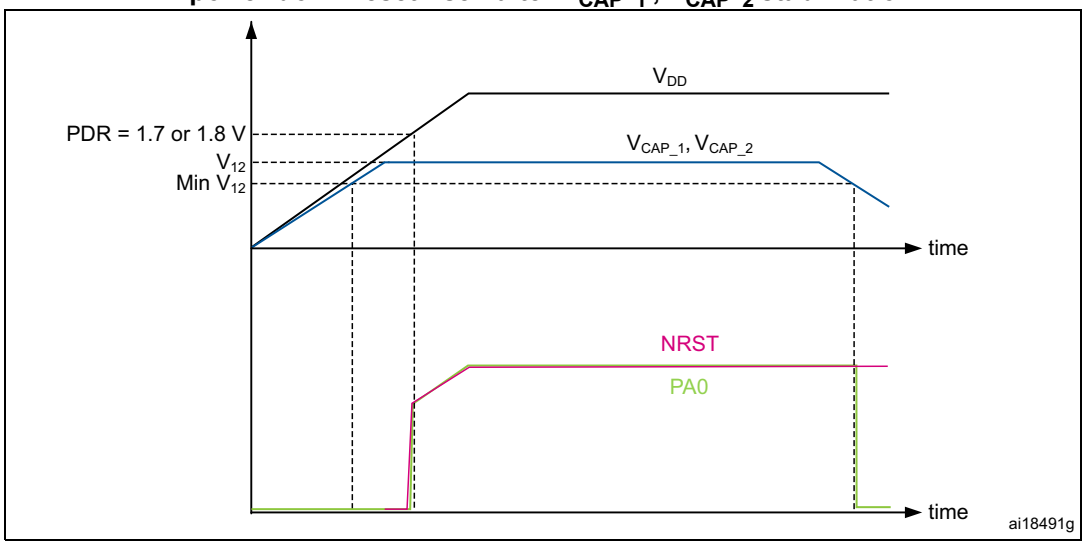
1.1.2 LQFP208 package

Figure 2. Incompatible board design for LQFP208 package



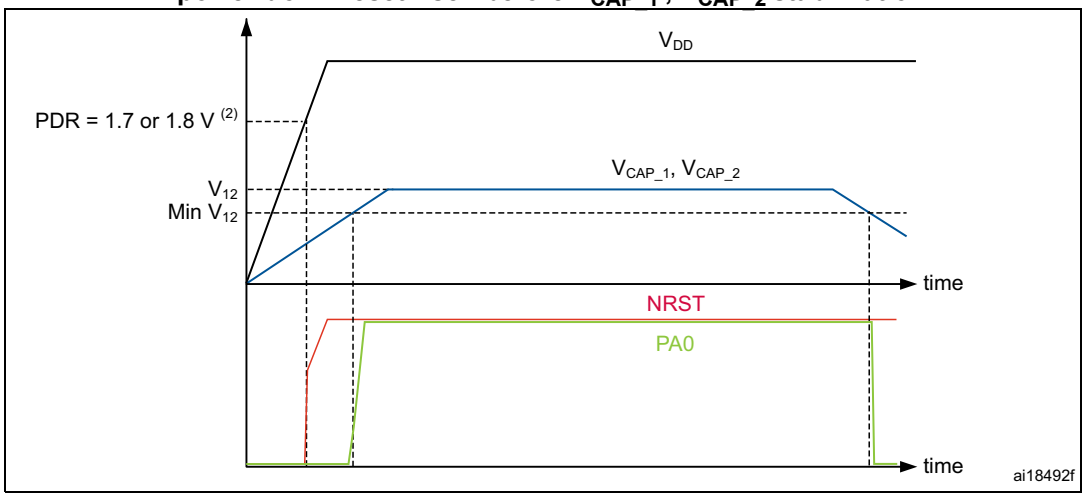
1. Pins from 118 to 128 and pin 137 are not compatible

Figure 11. Startup in regulator OFF: slow V_{DD} slope - power-down reset risen after V_{CAP_1}, V_{CAP_2} stabilization



1. This figure is valid whatever the internal reset mode (ON or OFF).

Figure 12. Startup in regulator OFF mode: fast V_{DD} slope - power-down reset risen before V_{CAP_1}, V_{CAP_2} stabilization



1. This figure is valid whatever the internal reset mode (ON or OFF).

2.20.3 Regulator ON/OFF and internal reset ON/OFF availability

Table 4. Regulator ON/OFF and internal reset ON/OFF availability

Package	Regulator ON	Regulator OFF	Internal reset ON	Internal reset OFF
WLCSP168 UFBGA169 LQFP208	Yes	No	Yes PDR_ON set to V_{DD}	Yes PDR_ON set to V_{SS}
LQFP176 UFBGA176 TFBGA216	Yes BYPASS_REG set to V_{SS}	Yes BYPASS_REG set to V_{DD}		

Table 12. Alternate function (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2	TIM3/4/5	TIM8/9/10/11	I2C1/2/3	SPI1/2/3/4/5/6	SPI2/3/SAI1	SPI2/3/USART1/2/3	USART6/UART4/5/7/8	CAN1/2/TIM12/13/14/QUADSPI/LCD	QUADSPI/OTG2_HS/OTG1_FS	ETH	FMC/SDIO/OTG2_FS	DCMI/DSI HOST	LCD	SYS
Port D	PD0	-	-	-	-	-	-	-	-	-	CAN1_RX	-	-	FMC_D2	-	-	EVENTOUT
	PD1	-	-	-	-	-	-	-	-	-	CAN1_TX	-	-	FMC_D3	-	-	EVENTOUT
	PD2	TRACED2	-	TIM3_ETR	-	-	-	-	-	UART5_RX	-	-	-	SDIO_CMD	DCMI_D11	-	EVENTOUT
	PD3	-	-	-	-	-	SPI2_SCK/I2S2_CK	-	USART2_CTS	-	-	-	-	FMC_CLK	DCMI_D5	LCD_G7	EVENTOUT
	PD4	-	-	-	-	-	-	-	USART2_RTS	-	-	-	-	FMC_NOE	-	-	EVENTOUT
	PD5	-	-	-	-	-	-	-	USART2_TX	-	-	-	-	FMC_NWE	-	-	EVENTOUT
	PD6	-	-	-	-	-	SPI3_MOSI/I2S3_SD	SAI1_SD_A	USART2_RX	-	-	-	-	FMC_NWAIT	DCMI_D10	LCD_B2	EVENTOUT
	PD7	-	-	-	-	-	-	-	USART2_CK	-	-	-	-	FMC_NE1	-	-	EVENTOUT
	PD8	-	-	-	-	-	-	-	USART3_TX	-	-	-	-	FMC_D13	-	-	EVENTOUT
	PD9	-	-	-	-	-	-	-	USART3_RX	-	-	-	-	FMC_D14	-	-	EVENTOUT
	PD10	-	-	-	-	-	-	-	USART3_CK	-	-	-	-	FMC_D15	-	LCD_B3	EVENTOUT
	PD11	-	-	-	-	-	-	-	USART3_CTS	-	QUADSPI_BK1_IO0	-	-	FMC_A16/FMC_CLE	-	-	EVENTOUT
	PD12	-	-	TIM4_CH1	-	-	-	-	USART3_RTS	-	QUADSPI_BK1_IO1	-	-	FMC_A17/FMC_ALE	-	-	EVENTOUT
	PD13	-	-	TIM4_CH2	-	-	-	-	-	-	QUADSPI_BK1_IO3	-	-	FMC_A18	-	-	EVENTOUT
	PD14	-	-	TIM4_CH3	-	-	-	-	-	-	-	-	-	FMC_D0	-	-	EVENTOUT
	PD15	-	-	TIM4_CH4	-	-	-	-	-	-	-	-	-	FMC_D1	-	-	EVENT‘OUT

Table 13. STM32F479xx register boundary addresses(1)

Bus	Boundary address	Peripheral
-	0xE00F FFFF - 0xFFFF FFFF	Reserved
Cortex®-M4	0xE000 0000 - 0xE00F FFFF	Cortex®-M4 internal peripherals
AHB3	0xD000 0000 - 0xDFFF FFFF	FMC bank 6
	0xC000 0000 - 0xCFFF FFFF	FMC bank 5
	0xA000 1000 - 0xA0001FFF	Quad-SPI control register
	0xA000 2000 - 0xBFFF FFFF	Reserved
	0xA000 0000- 0xA000 0FFF	FMC control register
	0x9000 0000 - 0x9FFF FFFF	Quad-SPI bank
	0x8000 0000 - 0x8FFF FFFF	FMC bank 3
	0x7000 0000 - 0x7FFF FFFF	FMC bank 2 (reserved)
	0x6000 0000 - 0x6FFF FFFF	FMC bank 1
-	0x5006 0C00- 0x5FFF FFFF	Reserved
AHB2	0x5006 0800 - 0x5006 0BFF	RNG
	0x5006 0400 - 0x5006 07FF	HASH
	0x5006 0000 - 0x5006 03FF	CRYP
	0x5005 0400 - 0x5005 FFFF	Reserved
	0x5005 0000 - 0x5005 03FF	DCMI
	0x5004 0000- 0x5004 FFFF	Reserved
	0x5000 0000 - 0x5003 FFFF	USB OTG FS

Table 13. STM32F479xx register boundary addresses[1] (continued)

Bus	Boundary address	Peripheral
-	0x4008 0000- 0x4FFF FFFF	Reserved
AHB1	0x4004 0000 - 0x4007 FFFF	USB OTG HS
	0x4002 BC00- 0x4003 FFFF	Reserved
	0x4002 B000 - 0x4002 BBFF	Chrom (DMA2D)
	0x4002 9400 - 0x4002 AFFF	Reserved
	0x4002 9000 - 0x4002 93FF	ETHERNET MAC
	0x4002 8C00 - 0x4002 8FFF	
	0x4002 8800 - 0x4002 8BFF	
	0x4002 8400 - 0x4002 87FF	
	0x4002 8000 - 0x4002 83FF	
	0x4002 6800 - 0x4002 7FFF	Reserved
	0x4002 6400 - 0x4002 67FF	DMA2
	0x4002 6000 - 0x4002 63FF	DMA1
	0x4002 5000 - 0x4002 5FFF	Reserved
	0x4002 4000 - 0x4002 4FFF	BKPSRAM
	0x4002 3C00 - 0x4002 3FFF	Flash interface register
	0x4002 3800 - 0x4002 3BFF	RCC
	0x4002 3400 - 0x4002 37FF	Reserved
	0x4002 3000 - 0x4002 33FF	CRC
	0x4002 2C00 - 0x4002 2FFF	Reserved
	0x4002 2800 - 0x4002 2BFF	GPIOK
	0x4002 2400 - 0x4002 27FF	GPIOJ
	0x4002 2000 - 0x4002 23FF	GPIOI
	0x4002 1C00 - 0x4002 1FFF	GPIOH
	0x4002 1800 - 0x4002 1BFF	GPIOG
	0x4002 1400 - 0x4002 17FF	GPIOF
	0x4002 1000 - 0x4002 13FF	GPIOE
	0x4002 0C00 - 0x4002 0FFF	GPIOD
	0x4002 0800 - 0x4002 0BFF	GPIOC
	0x4002 0400 - 0x4002 07FF	GPIOB
	0x4002 0000 - 0x4002 03FF	GPIOA

7. To sustain a voltage higher than VDD+0.3, the internal Pull-up and Pull-Down resistors must be disabled
8. If T_A is lower, higher P_D values are allowed as long as T_J does not exceed T_{Jmax}.
9. In low power dissipation state, T_A can be extended to this range as long as T_J does not exceed T_{Jmax}.

Table 18. Limitations depending on the operating power supply range

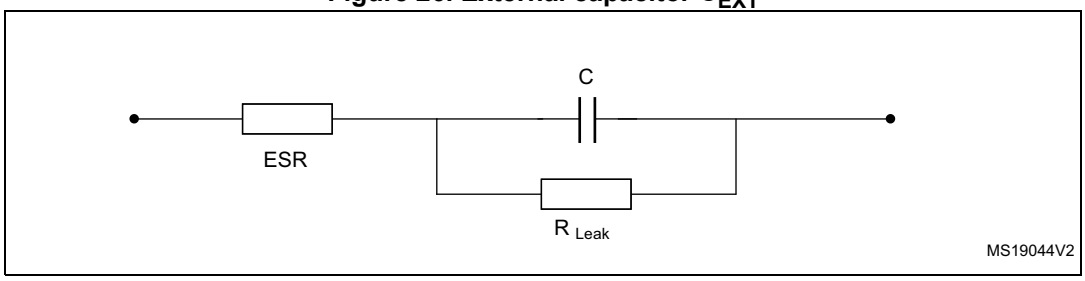
Operating power supply range	ADC operation	Maximum Flash memory access frequency with no wait states ($f_{Flashmax}$)	Maximum HCLK frequency vs. Flash memory wait states (1)(2)	I/O operation	Possible Flash memory operations
V_{DD} = 1.7 to 2.1 V(3)	Conversion time up to 1.2 Msps	20 MHz(4)	168 MHz with 8 wait states and over-drive OFF	No I/O compensation	8-bit erase and program operations only
V_{DD} = 2.1 to 2.4 V		22 MHz	180 MHz with 8 wait states and over-drive ON		16-bit erase and program operations
V_{DD} = 2.4 to 2.7 V	Conversion time up to 2.4 Msps	24 MHz	180 MHz with 7 wait states and over-drive ON	I/O compensation works	16-bit erase and program operations
V_{DD} = 2.7 to 3.6 V(5)		30 MHz	180 MHz with 5 wait states and over-drive ON		32-bit erase and program operations

1. Applicable only when the code is executed from Flash memory. When the code is executed from RAM, no wait state is required.
2. Thanks to the ART accelerator and the 128-bit Flash memory, the number of wait states given here does not impact the execution speed from Flash memory since the ART accelerator allows to achieve a performance equivalent to 0 wait state program execution.
3. V_{DD}/V_{DDA} minimum value of 1.7 V is obtained with the use of an external power supply supervisor (refer to *Section 2.19.2*).
4. Prefetch is not available.
5. When V_{DDUSB} is connected to V_{DD}, the voltage range for USB full speed PHYs can drop down to 2.7 V. However the electrical characteristics of D- and D+ pins will be degraded between 2.7 and 3 V.

5.3.2 VCAP1/VCAP2 external capacitor

Stabilization for the main regulator is achieved by connecting an external capacitor C_{EXT} to the VCAP1/VCAP2 pins. C_{EXT} is specified in *Table 19*.

Figure 26. External capacitor C_{EXT}



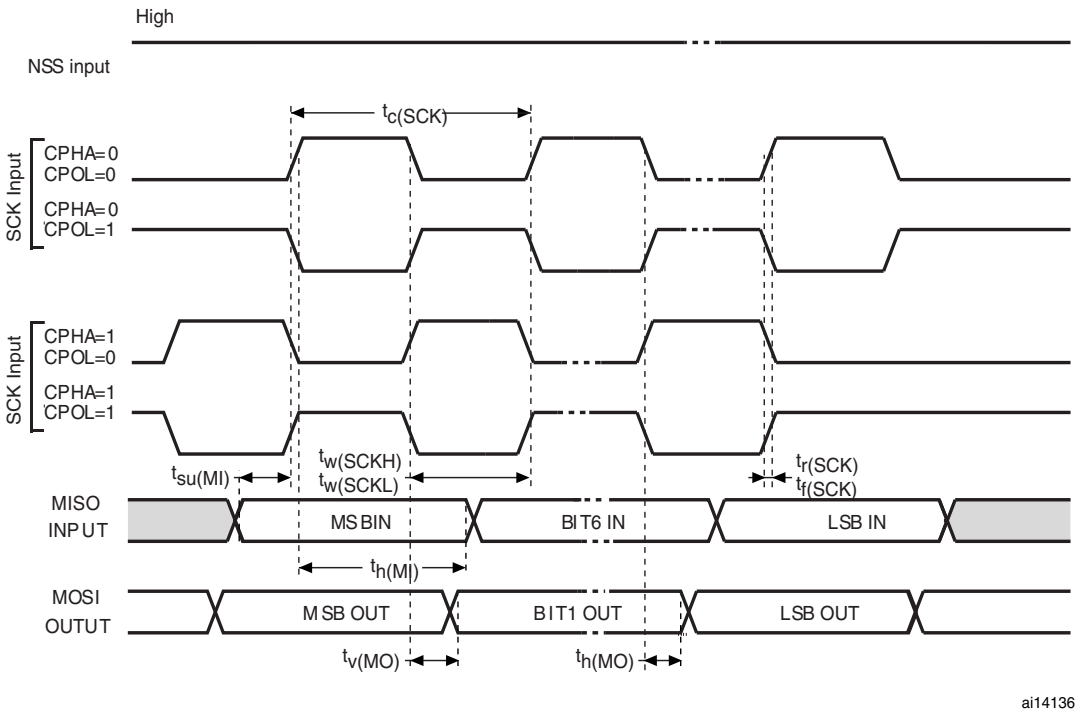
1. Legend: ESR is the equivalent series resistance.

Table 28. Typical and maximum current consumption in Sleep mode, regulator OFF

Symbol	Parameter	Conditions	f_{HCLK} (MHz)	Typ		Max(1)						Unit
				I_{DD12}	I_{DD}	T_A = 25 °C		T_A = 85 °C		T_A = 105 °C		
						I_{DD12}	I_{DD}	I_{DD12}	I_{DD}	I_{DD12}	I_{DD}	
I_{DD12} / I_{DD}	Supply current in RUN mode from V_{12} and V_{DD} supply	All Peripherals enabled	168	70	1	75	1	100	1	126	1	mA
			150	63	1	70	1	93	1	118	1	
			144	57	1	61	1	84	1	108	1	
			120	42	1	45	1	64	1	84	1	
			90	32	1	36	1	53	1	73	1	
			60	22	1	24	1	43	1	63	1	
			30	12	1	14	1	33	1	53	1	
			25	10	1	12	1	31	1	51	1	
		All Peripherals disabled	168	20	1	24	1	49	1	75	1	
			150	18	1	22	1	47	1	73	1	
			144	16	1	19	1	42	1	66	1	
			120	12	1	14	1	33	1	53	1	
			90	10	1	12	1	30	1	50	1	
			60	7	1	9	1	27	1	47	1	
			30	4	1	6	1	24	1	44	1	
			25	4	1	6	1	24	1	44	1	

1. Guaranteed based on test during characterization.

Figure 44. SPI timing diagram - master mode(1)



I²S interface characteristics

Unless otherwise specified, the parameters given in *Table 65* for the I²S interface are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in *Table 17*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: 0.5 V_{DD}

Refer to *Section 5.3.20* for more details on the input/output alternate function characteristics (CK, SD, WS).

Table 65. I²S dynamic characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
f_{MCK}	I2S Main clock output	-	256x8K	256xFs(2)	MHz
f_{CK}	I2S clock frequency	Master data	-	64xFs	
		Slave data	-	64xFs	
D_{CK}	I2S clock frequency duty cycle	Slave receiver	30	70	%
$t_{v(WS)}$	WS valid time	Master mode	0	5	ns
$t_{h(WS)}$	WS hold time	Master mode	0	-	
$t_{su(WS)}$	WS setup time	Slave mode	3.5	-	
		Slave mode PCM short pulse mode(3)	3.5	-	
$t_{h(WS)}$	WS hold time	Slave mode	0.5	-	
		Slave mode PCM short pulse mode(3)	1	-	
$t_{su(SD\_MR)}$	Data input setup time	Master receiver	5	-	
$t_{su(SD\_SR)}$		Slave receiver	1.5	-	
$t_{h(SD\_MR)}$	Data input hold time	Master receiver	5	-	
$t_{h(SD\_SR)}$		Slave receiver	1.5	-	
$t_{v(SD\_ST)}$	Data output valid time	Slave transmitter (after enable edge)	-	19	
$t_{v(SD\_MT)}$		Master transmitter (after enable edge)	-	2.50	
$t_{h(SD\_ST)}$	Data output hold time	Slave transmitter (after enable edge)	5	-	
$t_{h(SD\_MT)}$		Master transmitter (after enable edge)	0	-	

1. Guaranteed based on test during characterization.
2. 128xFs maximum is 24.756 MHz (APB1 Maximum frequency).
3. Measurement done with respect to I2S_CK rising edge.

Note: Refer to the I2S section of RM0386 reference manual for more details on the sampling frequency (F_S).

f_{MCK}, f_{CK}, and D_{CK} values reflect only the digital peripheral behavior, source clock precision might slightly change the values. The values of these parameters might be slightly impacted by the source clock precision. D_{CK} depends mainly on the value of ODD bit. The digital

SAI characteristics

Unless otherwise specified, the parameters given in *Table 66* for SAI are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and VDD supply voltage conditions summarized in *Table 17*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C=30 pF
- Measurement points are performed at CMOS levels: 0.5 V_{DD}

Refer to *Section 5.3.20* for more details on the input/output alternate function characteristics (SCK,SD,WS).

Table 66. SAI characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
f_{MCKL}	SAI Main clock output	-	256 x 8K	256xFs	MHz
f_{CK}	SAI clock frequency(2)	Master data: 32 bits	-	128xFs(3)	
		Slave data: 32 bits	-	128xFs	
$t_{v(FS)}$	FS valid time	Master mode, 2.7V ≤ V_{DD} ≤ 3.6V	-	17	ns
		Master mode, 1.71V ≤ V_{DD} ≤ 3.6V	-	23	
$t_{su(FS)}$	FS setup time	Slave mode	10	-	
$t_{h(FS)}$	FS hold time	Slave mode	0	-	
$t_{su(SD\_MR)}$	Data input setup time	Master receiver	1	-	
$t_{su(SD\_SR)}$		Slave receiver	2	-	
$t_{h(SD\_MR)}$	Data input hold time	Master receiver	6	-	
$t_{h(SD\_SR)}$		Slave receiver	1	-	
$t_{h(SD\_B\_ST)}$	Data output valid time	Slave transmitter (after enable edge), 2.7V ≤ V_{DD} ≤ 3.6V	-	14	
		Slave transmitter (after enable edge), 1.71V ≤ V_{DD} ≤ 3.6V	-	23	
$t_{h(SD\_B\_ST)}$	Data output hold time	Slave transmitter (after enable edge)	9	-	
$t_{v(SD\_A\_MT)}$	Data output valid time	Master transmitter (after enable edge), 2.7V ≤ V_{DD} ≤ 3.6V	-	20	
		Master transmitter (after enable edge), 1.71V ≤ V_{DD} ≤ 3.6V	-	26	
$t_{h(SD\_A\_MT)}$	Data output hold time	Master transmitter (after enable edge)	10	-	

1. Guaranteed based on test during characterization.
2. APB clock frequency must be at least twice SAI clock frequency.
3. With Fs = 192 kHz.

Figure 49. USB OTG full speed timings: definition of data signal rise and fall time

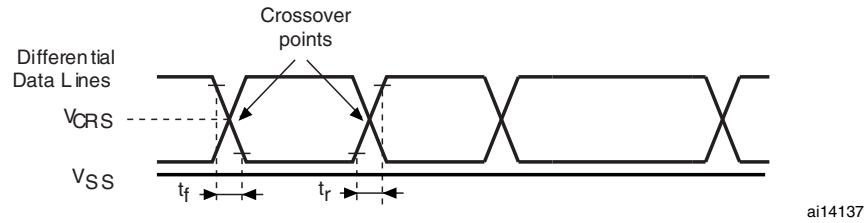


Table 69. USB OTG full speed electrical characteristics(1)

Driver characteristics					
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Unit**
t_r	Rise time(2)	C_L = 50 pF	4	20	ns
t_f	Fall time(2)	C_L = 50 pF	4	20	
t_{rfm}	Rise/ fall time matching	t_r/t_f	90	110	%
V_{CRS}	Output signal crossover voltage	-	1.3	2.0	V
Z_{DRV}	Output driver impedance(3)	Driving high or low	28	44	Ω

1. Guaranteed by design.
2. Measured from 10% to 90% of the data signal. For more detailed informations, please refer to USB Specification - Chapter 7 (version 2.0).
3. No external termination series resistors are required on DP (D+) and DM (D-) pins since the matching impedance is included in the embedded driver.

USB high speed (HS) characteristics

Unless otherwise specified, the parameters given in *Table 72* for ULPI are derived from tests performed under the ambient temperature, f_{HCLK} frequency summarized in *Table 71* and V_{DD} supply voltage conditions summarized in *Table 70*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11, unless otherwise specified
- Capacitive load C = 20 pF / 15 pF, unless otherwise specified
- Measurement points are done at CMOS levels: 0.5 V_{DD}.

Refer to *Section 5.3.20* for more details on the input/output characteristics.

Table 70. USB HS DC electrical characteristics

Symbol		Parameter	Min.(1)	Max.(1)	Unit
Input level	V_{DD}	USB OTG HS operating voltage	1.7	3.6	V

1. All the voltages are measured from the local ground potential.

5.3.25 Temperature sensor characteristics

Table 82. Temperature sensor characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L (1)	V_{SENSE} linearity with temperature	-	±1	±2	°C
Avg_Slope(1)	Average slope	-	2.5	-	mV/°C
V_{25} (1)	Voltage at 25 °C	-	0.76	-	V
t_{START} (2)	Startup time	-	6	10	µs
T_{S_temp} (2)	ADC sampling time when reading the temperature (1 °C accuracy)	10	-	-	

1. Based on test during characterization.
2. Guaranteed by design.

Table 83. Temperature sensor calibration values

Symbol	Parameter	Memory address
TS_CAL1	TS ADC raw data acquired at temperature of 30 °C, V_{DDA}= 3.3 V	0x1FFF 7A2C - 0x1FFF 7A2D
TS_CAL2	TS ADC raw data acquired at temperature of 110 °C, V_{DDA}= 3.3 V	0x1FFF 7A2E - 0x1FFF 7A2F

5.3.26 V_{BAT} monitoring characteristics

Table 84. V_{BAT} monitoring characteristics

Symbol	Parameter	Min	Typ	Max	Unit
R	Resistor bridge for V_{BAT}	-	50	-	KΩ
Q	Ratio on V_{BAT} measurement	-	4	-	
Er(1)	Error on Q	–1	-	+1	%
T_{S_vbat} (2)(2)	ADC sampling time when reading the V_{BAT} 1 mV accuracy	5	-	-	µs

1. Guaranteed by design.
2. Shortest sampling time can be determined in the application by multiple iterations.

5.3.27 Reference voltage

The parameters given in *Table 85* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 17*.

Table 85. internal reference voltage

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltage	–40 °C < T_A < +105 °C	1.18	1.21	1.24	V
$T_{S\_vrefint}$ (1)	ADC sampling time when reading the internal reference voltage		10	-	-	µs
V_{RERINT_s} (2)	Internal reference voltage spread over the temperature range	V_{DD} = 3V ± 10mV	-	3	5	mV

Table 85. internal reference voltage (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{Coeff}(2)	Temperature coefficient		-	30	50	ppm/°C
t_{START}(2)	Startup time		-	6	10	µs

1. Shortest sampling time can be determined in the application by multiple iterations.
2. Guaranteed by design

Table 86. Internal reference voltage calibration values

Symbol	Parameter	Memory address
V_{REFIN_CAL}	Raw data acquired at temperature of 30 °C V_{DDA} = 3.3 V	0x1FFF 7A2A - 0x1FFF 7A2B

5.3.28 DAC electrical characteristics

Table 87. DAC characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Comments
V_{DDA}	Analog supply voltage	1.7(1)	-	3.6	V	-
V_{REF+}	Reference supply voltage	1.7(1)	-	3.6	V	$V_{REF+} \leq V_{DDA}$
V_{SSA}	Ground	0	-	0	V	-
R_{LOAD}(2)	Resistive load with buffer ON	5	-	-	kΩ	-
R_O(2)	Impedance output with buffer OFF	-	-	15	kΩ	When the buffer is OFF, the Minimum resistive load between DAC_OUT and V_{SS} to have a 1% accuracy is 1.5 MΩ
C_{LOAD}(2)	Capacitive load	-	-	50	pF	Maximum capacitive load at DAC_OUT pin (when the buffer is ON).
DAC_OUT min(2)	Lower DAC_OUT voltage with buffer ON	0.2	-	-	V	It gives the maximum output excursion of the DAC. It corresponds to 12-bit input code (0x0E0) to (0xF1C) at V_{REF+} = 3.6 V and (0x1C7) to (0xE38) at V_{REF+} = 1.7 V
DAC_OUT max(2)	Higher DAC_OUT voltage with buffer ON	-	-	V_{DDA} – 0.2	V	
DAC_OUT min(2)	Lower DAC_OUT voltage with buffer OFF	-	0.5	-	mV	It gives the maximum output excursion of the DAC.
DAC_OUT max(2)	Higher DAC_OUT voltage with buffer OFF	-	-	V_{REF+} – 1LSB	V	
I_{VREF+}(4)	DAC DC V_{REF} current consumption in quiescent mode (Standby mode)	-	170	240	µA	With no load, worst code (0x800) at V_{REF+} = 3.6 V in terms of DC consumption on the inputs
		-	50	75		With no load, worst code (0xF1C) at V_{REF+} = 3.6 V in terms of DC consumption on the inputs

Figure 62. Asynchronous multiplexed PSRAM/NOR write waveforms

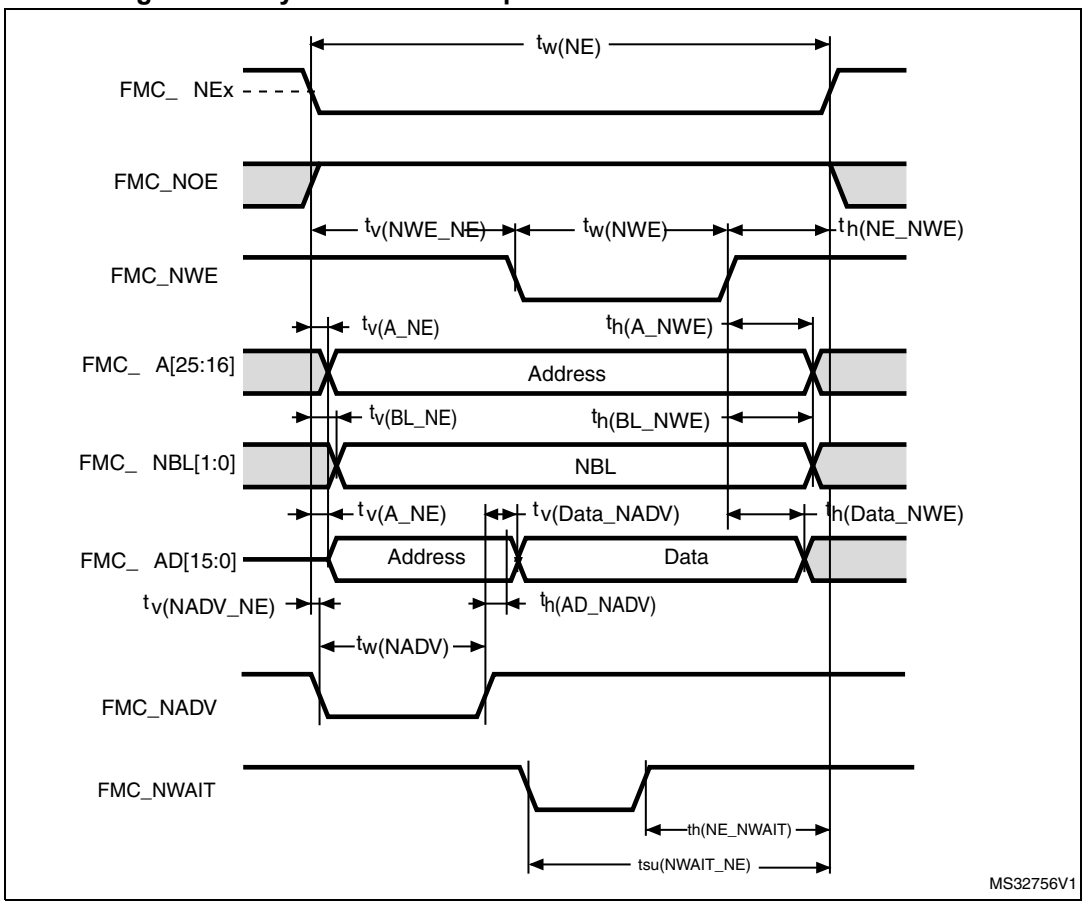


Table 94. Asynchronous multiplexed PSRAM/NOR write timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$4T_{HCLK}$	$4T_{HCLK}+0.5$	ns
$t_{v(NWE\_NE)}$	FMC_NEx low to FMC_NWE low	$T_{HCLK} - 1$	$T_{HCLK}+0.5$	
$t_{w(NWE)}$	FMC_NWE low time	$2T_{HCLK}$	$2T_{HCLK}+0.5$	
$t_{h(NE\_NWE)}$	FMC_NWE high to FMC_NE high hold time	T_{HCLK}	-	
$t_{v(A\_NE)}$	FMC_NEx low to FMC_A valid	-	0	
$t_{v(NADV\_NE)}$	FMC_NEx low to FMC_NADV low	0.5	1	
$t_{w(NADV)}$	FMC_NADV low time	$T_{HCLK} - 0.5$	$T_{HCLK}+ 0.5$	
$t_{h(AD\_NADV)}$	FMC_AD (address) valid hold time after FMC_NADV high	$T_{HCLK} - 2$	-	
$t_{h(A\_NWE)}$	Address hold time after FMC_NWE high	T_{HCLK}	-	
$t_{h(BL\_NWE)}$	FMC_BL hold time after FMC_NWE high	$T_{HCLK} - 2$	-	
$t_{v(BL\_NE)}$	FMC_NEx low to FMC_BL valid	-	2	
$t_{v(Data\_NADV)}$	FMC_NADV high to Data valid	-	$T_{HCLK}+1.5$	
$t_{h(Data\_NWE)}$	Data hold time after FMC_NWE high	$T_{HCLK}+0.5$	-	

1. Based on test during characterization.

Figure 64. Synchronous multiplexed PSRAM write timings

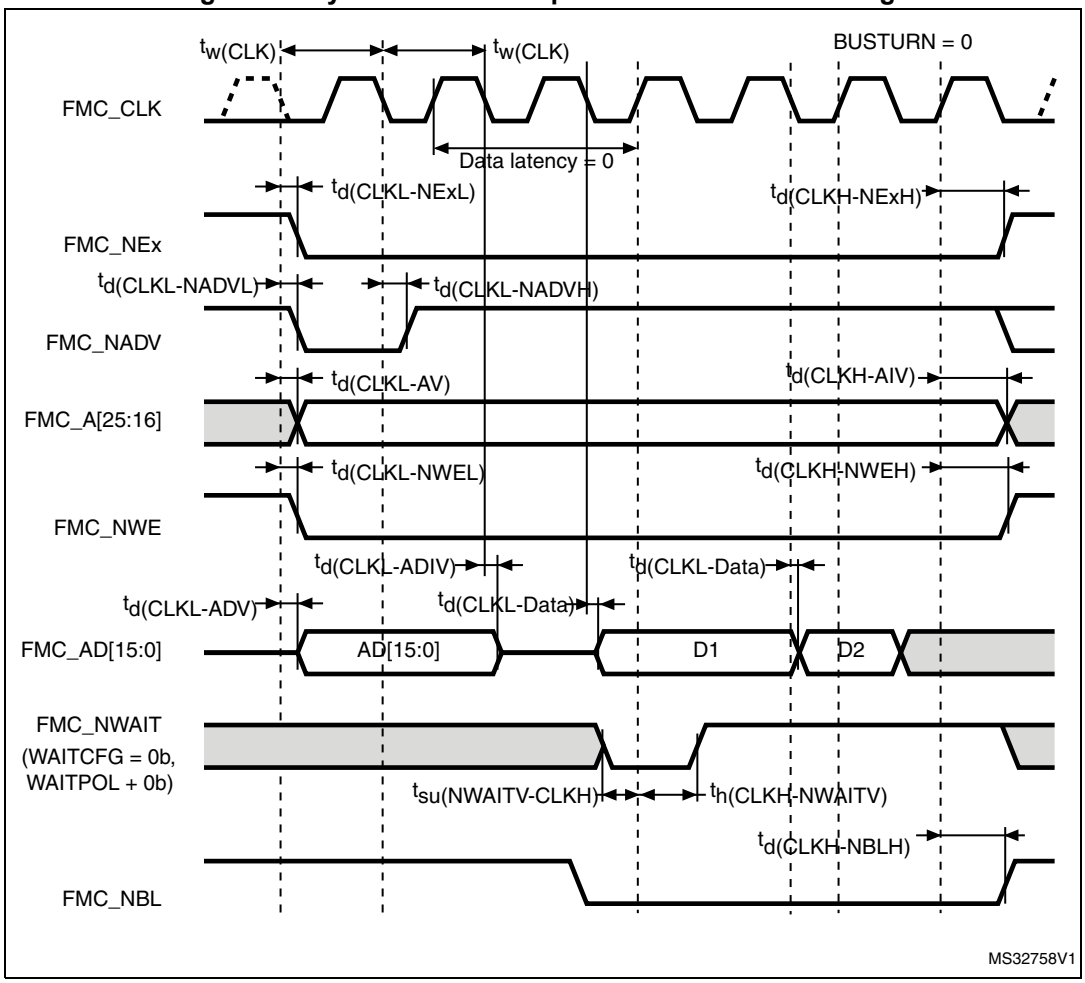


Figure 68. NAND controller waveforms for write access

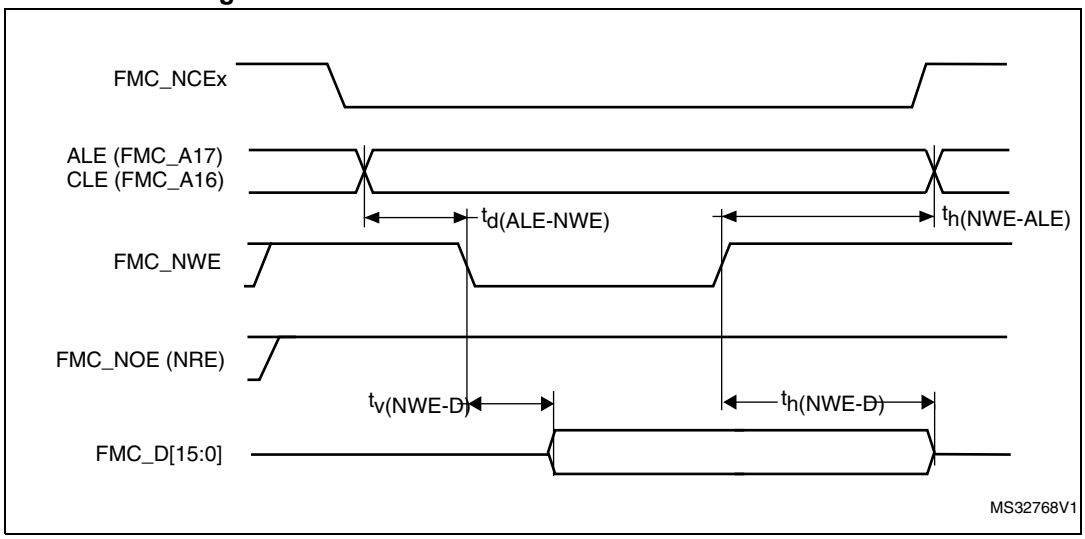


Figure 69. NAND controller waveforms for common memory read access

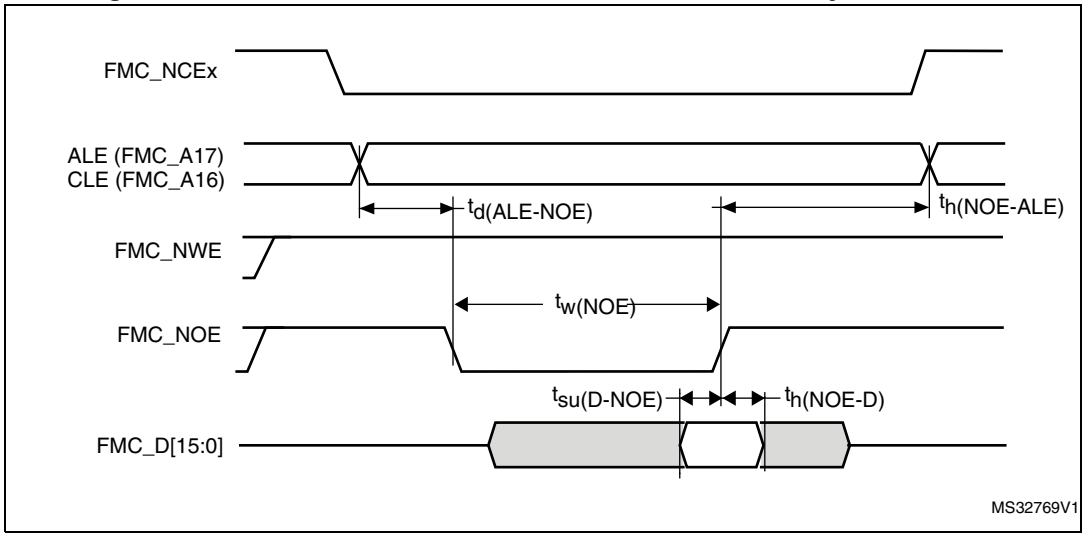
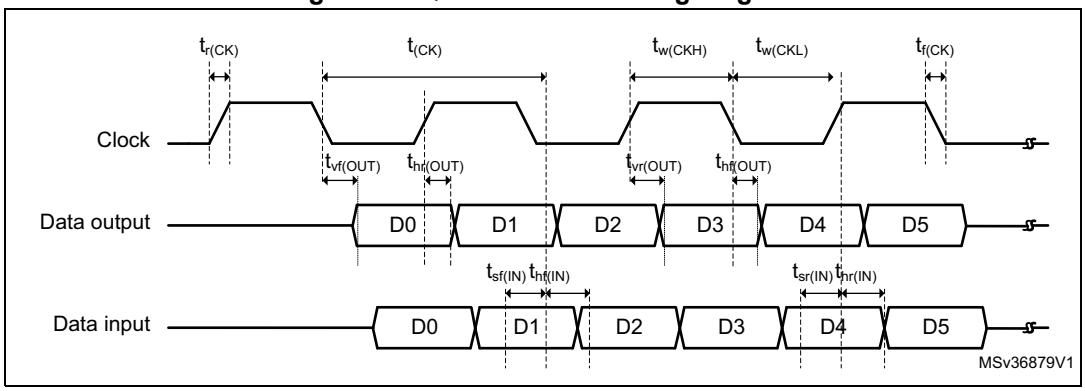


Table 107. Quad-SPI characteristics in DDR mode(1)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
F_{ck} $1/t_{(CK)}$	Quad-SPI clock frequency	2.7 V ≤ V_{DD} ≤ 3.6 V, C_L = 20 pF	-	-	80	MHz
		1.71 V ≤ V_{DD} ≤ 3.6 V, C_L = 15 pF	-	-	70	
$t_{w(CKH)}$	Quad-SPI clock high time	-	$t_{(CK)}$/2-1	-	$t_{(CK)}$/2	ns
$t_{w(CKL)}$	Quad-SPI clock low time	-	$t_{(CK)}$/2	-	$t_{(CK)}$/2+1	
$t_{sr(IN)}$ $t_{sf(IN)}$	Data input set-up time	2.7 V ≤ V_{DD} ≤ 3.6 V	2	-	-	
		1.71 V ≤ V_{DD} ≤ 3.6 V	0.5	-	-	
$t_{hr(IN)}$ $t_{hf(IN)}$	Data input hold time	2.7 V ≤ V_{DD} ≤ 3.6 V	3	-	-	
		1.71 V ≤ V_{DD} ≤ 3.6 V	4.5	-	-	
$t_{vr(OUT)}$ $t_{vf(OUT)}$	Data output valid time	DHHC=0	-	8	10.5	
		DHHC=1 Pres=1,2…	-	T_{hclk}/2+2	T_{hclk}/2+2.5	
$t_{h(OUT)}$ $t_{f(OUT)}$	Data output hold time	DHHC=0	7	-	-	
		DHHC=1 Pres=1,2…	T_{hclk}/2+0.5	-	-	

1. Guaranteed based on test during characterization.

Figure 74. Quad-SPI DDR timing diagram



5.3.31 Camera interface (DCMI) timing specifications

Unless otherwise specified, the parameters given in *Table 108* for DCMI are derived from tests performed under the ambient temperature, f_{HCLK} frequency and V_{DD} supply voltage summarized in *Table 17*, with the following configuration:

- DCMI_PIXCLK polarity: falling
- DCMI_VSYNC and DCMI_HSYNC polarity: high
- Data formats: 14 bits
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: 0.5 V_{DD}

Table 114. LQFP144 - 144-pin, 20 x 20 mm low-profile quad flat package mechanical data

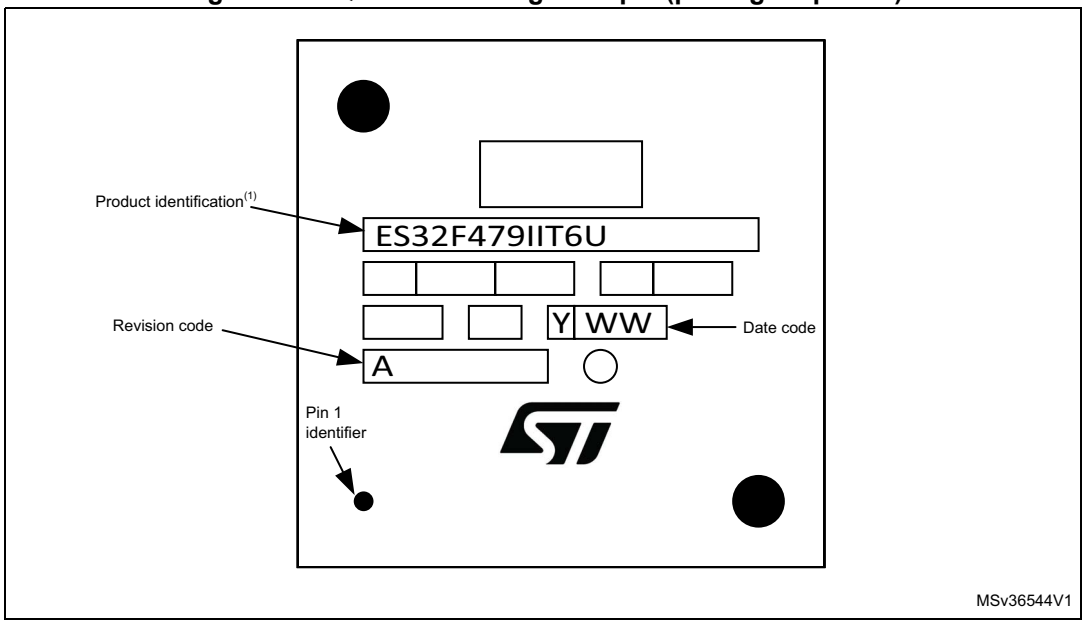
Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	21.800	22.000	22.200	0.8583	0.8661	0.8740
D1	19.800	20.000	20.200	0.7795	0.7874	0.7953
D3	-	17.500	-	-	0.6890	-
E	21.800	22.000	22.200	0.8583	0.8661	0.8740
E1	19.800	20.000	20.200	0.7795	0.7874	0.7953
E3	-	17.500	-	-	0.6890	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Device Marking for LQFP176

The following figure gives an example of topside marking orientation versus pin 1 identifier location. Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 91. LQFP176 marking example (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.