STMicroelectronics - STM32F479VGT6 Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	180MHz
Connectivity	CANbus, EBI/EMI, I²C, IrDA, LINbus, SAI, SDIO, SPI, UART/USART, USB, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	71
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	384K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	A/D 14x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f479vgt6

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2.10 Quad-SPI memory interface (QUADSPI)

All STM32F479xx devices embeds a Quad-SPI memory interface, which is a specialized communication interface targeting Single, Dual, Quad or Dual-flash SPI memories. It can work in direct mode through registers, external flash status register polling mode and memory mapped mode. Up to 256 Mbytes external Flash memory are mapped, supporting 8, 16 and 32-bit access. Code execution is supported.

The opcode and the frame format are fully programmable. Communication can be either in Single Data Rate or Dual Data Rate.

2.11 LCD-TFT controller

The LCD-TFT display controller provides a 24-bit parallel digital RGB (Red, Green, Blue) and delivers all signals to interface directly to a broad range of LCD and TFT panels up to XGA (1024x768) resolution with the following features:

- 2 displays layers with dedicated FIFO (64x32-bit)
- Color Look-Up table (CLUT) up to 256 colors (256x24-bit) per layer
- Up to 8 Input color formats selectable per layer
- Flexible blending between two layers using alpha value (per pixel or constant)
- Flexible programmable parameters for each layer
- Color keying (transparency color)
- Up to 4 programmable interrupt events.

2.12 DSI Host (DSIHOST)

The DSI Host is a dedicated peripheral for interfacing with MIPI® DSI compliant displays. It includes a dedicated video interface internally connected to the LTDC and a generic APB interface that can be used to transmit information to the display.

These interfaces are as follows:

- LTDC interface:
  - Used to transmit information in Video Mode, in which the transfers from the host processor to the peripheral take the form of a real-time pixel stream (DPI).
  - Through a customized for mode, this interface can be used to transmit information in full bandwidth in the Adapted Command Mode (DBI).
- APB slave interface:
  - Allows the transmission of generic information in Command mode, and follows a proprietary register interface.
  - Can operate concurrently with either LTDC interface in either Video Mode or Adapted Command Mode.
- Video mode pattern generator:
  - Allows the transmission of horizontal/vertical color bar and D-PHY BER testing pattern without any kind of stimuli.

2.28 Inter-integrated sound (I^2S)

Two standard I^2S interfaces (multiplexed with SPI2 and SPI3) are available. They can be operated in master or slave mode, in full duplex and simplex communication modes, and can be configured to operate with a 16-/32-bit resolution as an input or output channel. Audio sampling frequencies from 8 kHz up to 192 kHz are supported. When either or both of the I^2S interfaces is/are configured in master mode, the master clock can be output to the external DAC/CODEC at 256 times the sampling frequency.

All I2Sx can be served by the DMA controller.

Note: For I2S2 *full-duplex mode, I2S2_CK and I2S2_WS signals can be used only on GPIO Port B and GPIO Port D.*

2.29 Serial Audio interface (SAI1)

The serial audio interface (SAI1) is based on two independent audio sub-blocks which can operate as transmitter or receiver with their FIFO. Many audio protocols are supported by each block: I2S standards, LSB or MSB-justified, PCM/DSP, TDM, AC'97 and SPDIF output, supporting audio sampling frequencies from 8 kHz up to 192 kHz. Both sub-blocks can be configured in master or in slave mode.

In master mode, the master clock can be output to the external DAC/CODEC at 256 times of the sampling frequency.

The two sub-blocks can be configured in synchronous mode when full-duplex mode is required.

SAI1 can be served by the DMA controller.

2.30 Audio PLL (PLLI2S)

The devices feature an additional dedicated PLL for audio I^2S and SAI applications. It allows to achieve error-free I^2S sampling clock accuracy without compromising on the CPU performance, while using USB peripherals.

The PLLI2S configuration can be modified to manage an I^2S/SAI sample rate change without disabling the main PLL (PLL) used for CPU, USB and Ethernet interfaces.

The audio PLL can be programmed with very low error to obtain sampling rates ranging from 8 KHz to 192 KHz.

In addition to the audio PLL, a master clock input pin can be used to synchronize the I^2S/SAI flow with an external PLL (or Codec output).

2.31 Audio and LCD PLL(PLLSAI)

An additional PLL dedicated to audio and LCD-TFT is used for SAI1 peripheral in case the PLLI2S is programmed to achieve another audio sampling frequency (49.152 MHz or 11.2896 MHz) and the audio application requires both sampling frequencies simultaneously.

The PLLSAI is also used to generate the LCD-TFT clock.

2.32 Secure digital input/output interface (SDIO)

An SD/SDIO/MMC host interface is available, that supports MultiMediaCard System Specification Version 4.2 in three different databus modes: 1-bit (default), 4-bit and 8-bit.

The interface allows data transfer at up to 48 MHz, and is compliant with the SD Memory Card Specification Version 2.0.

The SDIO Card Specification Version 2.0 is also supported with two different databus modes: 1-bit (default) and 4-bit.

The current version supports only one SD/SDIO/MMC4.2 card at any one time and a stack of MMC4.1 or previous.

In addition to SD/SDIO/MMC, this interface is fully compliant with the CE-ATA digital protocol Rev1.1.

2.33 Ethernet MAC interface with dedicated DMA and IEEE 1588 support

The devices provide an IEEE-802.3-2002-compliant media access controller (MAC) for ethernet LAN communications through an industry-standard medium-independent interface (MII) or a reduced medium-independent interface (RMII). The microcontroller requires an external physical interface device (PHY) to connect to the physical LAN bus (twisted-pair, fiber, etc.). The PHY is connected to the device MII port using 17 signals for MII or 9 signals for RMII, and can be clocked using the 25 MHz (MII) from the microcontroller.

The devices include the following features:

- Supports 10 and 100 Mbit/s rates
- Dedicated DMA controller allowing high-speed transfers between the dedicated SRAM and the descriptors (see the STM32F4xx reference manual for details)
- Tagged MAC frame support (VLAN support)
- Half-duplex (CSMA/CD) and full-duplex operation
- MAC control sublayer (control frames) support
- 32-bit CRC generation and removal
- Several address filtering modes for physical and multicast address (multicast and group addresses)
- 32-bit status code for each transmitted or received frame
- Internal FIFOs to buffer transmit and receive frames. The transmit FIFO and the receive FIFO are both 2 Kbytes.
- Supports hardware PTP (precision time protocol) in accordance with IEEE 1588 2008 (PTP V2) with the time stamp comparator connected to the TIM2 input
- Triggers interrupt when system time becomes greater than target time

2.34 Controller area network (bxCAN)

The two CANs are compliant with the 2.0A and B (active) specifications with a bitrate up to 1 Mbit/s. They can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers. Each CAN has three transmit mailboxes, two receive

Table 10. STM32F479xx pin and ball definitions (continued)

Pin number								Pin name (function after reset)(1)	Pin types	I/O structures	Notes	Alternate functions	Additional functions
LQFP100	LQFP144	UFBGA169	WLCSP168	UFBGA176	LQFP176	LQFP208	TFBGA216						
13	22	N1	L12	M3	33	36	M3	PC1	I/O	FT	(5)	TRACED0, SPI2_MOSI/I2S2_SD, SAI1_SD_A, ETH_MDC, EVENTOUT	ADC123_ IN11
14	23	-	-	M4	34	37	M4	PC2	I/O	FT	(5)	SPI2_MISO, I2S2ext_SD, OTG_HS_ULPI_DIR, ETH_MII_TXD2, FMC_SDNE0, EVENTOUT	ADC123_ IN12
15	24	-	-	M5	35	38	L4	PC3	I/O	FT	(5)	SPI2_MOSI/I2S2_SD, OTG_HS_ULPI_NXT, ETH_MII_TX_CLK, FMC_SDCKE0, EVENTOUT	ADC123_ IN13
-	25	-	-	-	36	39	J5	VDD	S	-	-	-	-
-	-	-	-	-	-	-	J6	VSS	S	-	-	-	-
16	26	J2	L11	M1	37	40	M1	VSSA	S	-	-	-	-
-	-	-	-	N1	-	-	N1	VREF-	S	-	-	-	-
17	27	-	-	P1	38	41	P1	VREF+	S	-	-	-	-
18	28	J3	M12	R1	39	42	R1	VDDA	S	-	-	-	-
19	29	J5	L10	N3	40	43	N3	PA0-WKUP(PA0)	I/O	FT	(6)	TIM2_CH1/TIM2_ETR, TIM5_CH1, TIM8_ETR, USART2_CTS, UART4_TX, ETH_MII_CRS, EVENTOUT	ADC123_IN0, WKUP
20	30	K1	K9	N2	41	44	N2	PA1	I/O	FT	(5)	TIM2_CH2, TIM5_CH2, USART2_RTS, UART4_RX, QUADSPI_BK1_IO3, ETH_MII_RX_CLK/ETH_R MII_REF_CLK, LCD_R2, EVENTOUT	ADC123_IN1
21	31	K2	L9	P2	42	45	P2	PA2	I/O	FT	(5)	TIM2_CH3, TIM5_CH3, TIM9_CH1, USART2_TX, ETH_MDIO, LCD_R1, EVENTOUT	ADC123_IN2
-	-	L2	M11	F4	43	46	K4	PH2	I/O	FT	-	QUADSPI_BK2_IO0, ETH_MII_CRS, FMC_SDCKE0, LCD_R0, EVENTOUT	-
-	-	L1	N12	G4	44	47	J4	PH3	I/O	FT	-	QUADSPI_BK2_IO1, ETH_MII_COL, FMC_SDNE0, LCD_R1, EVENTOUT	-
-	-	M2	M10	H4	45	48	H4	PH4	I/O	FT	-	I2C2_SCL, LCD_G5, OTG_HS_ULPI_NXT, LCD_G4, EVENTOUT	-

Table 10. STM32F479xx pin and ball definitions (continued)

Pin number								Pin name (function after reset)(1)	Pin types	I/O structures	Notes	Alternate functions	Additional functions
LQFP100	LQFP144	UFBGA169	WLCSP168	UFBGA176	LQFP176	LQFP208	TFBGA216						
-	-	J9	M4	-	-	100	P15	PH10	I/O	FT	-	TIM5_CH1, FMC_D18, DCMI_D1, LCD_R4, EVENTOUT	-
-	-	K9	N3	-	-	101	N15	PH11	I/O	FT	-	TIM5_CH2, FMC_D19, DCMI_D2, LCD_R5, EVENTOUT	-
-	-	H10	P2	-	-	102	M15	PH12	I/O	FT	-	TIM5_CH3, FMC_D20, DCMI_D3, LCD_R6, EVENTOUT	-
-	-	-	H7	-	-	-	K10	VSS	S	-	-	-	-
-	66	-	-	-	-	103	K11	VDD	S	-	-	-	-
46	67	N10	H5	P12	85	104	L13	PB12	I/O	FT	-	TIM1_BKIN, I2C2_SMBA, SPI2_NSS/I2S2_WS, USART3_CK, CAN2_RX, OTG_HS_ULPI_D5, ETH_MII_TXD0/ETH_RMII_TXD0, OTG_HS_ID, EVENTOUT	-
47	68	N11	K4	P13	86	105	K14	PB13	I/O	FT	-	TIM1_CH1N, SPI2_SCK/I2S2_CK, USART3_CTS, CAN2_TX, OTG_HS_ULPI_D6, ETH_MII_TXD1/ETH_RMII_TXD1, EVENTOUT	OTG_HS_VBUS
48	69	N12	P1	R14	87	106	R14	PB14	I/O	FT	-	TIM1_CH2N, TIM8_CH2N, SPI2_MISO, I2S2ext_SD, USART3_RTS, TIM12_CH1, OTG_HS_DM, EVENTOUT	-
49	70	N13	N2	R15	88	107	R15	PB15	I/O	FT	-	RTC_REFIN, TIM1_CH3N, TIM8_CH3N, SPI2_MOSI/I2S2_SD, TIM12_CH2, OTG_HS_DP, EVENTOUT	-
50	71	L10	L4	P15	89	108	L15	PD8	I/O	FT	-	USART3_TX, FMC_D13, EVENTOUT	-
51	72	M10	N1	P14	90	109	L14	PD9	I/O	FT	-	USART3_RX, FMC_D14, EVENTOUT	-
52	73	L11	M3	N15	91	110	K15	PD10	I/O	FT	-	USART3_CK, FMC_D15, LCD_B3, EVENTOUT	-
-	74	M11	J4	N14	92	111	N10	PD11	I/O	FT	-	USART3_CTS, QUADSPI_BK1_IO0, FMC_A16/FMC_CLE, EVENTOUT	-

4 Memory mapping

The memory map is shown in *Figure 21*.

Figure 21. Memory map

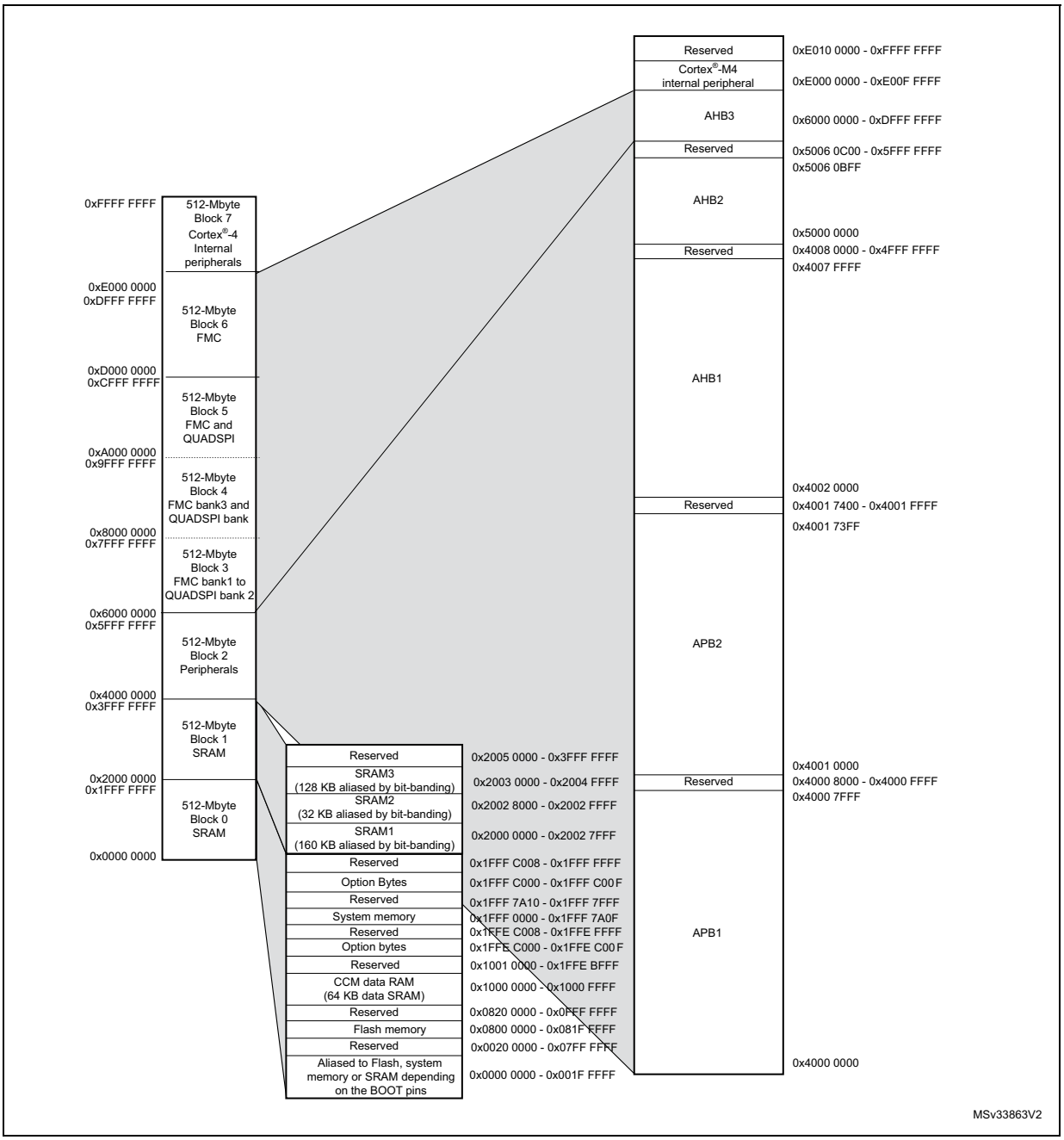


Table 27. Typical and maximum current consumption in Sleep mode, regulator ON

Symbol	Parameter	Conditions	f_{HCLK} (MHz)	Typ	Max(1)(2)(3)			Unit
					T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply current in Sleep mode	All Peripherals enabled	180	78	88(4)	118	151(4)	mA
			168	71	76	101	127	
			150	64	71	94	119	
			144	58	62	85	109	
			120	43	46	65	85	
			90	33	37	54	74	
			60	23	25	44	63	
			30	13	15	34	53	
			25	11	13	32	52	
			16	5	8	27	47	
			8	4	7	25	45	
			4	3	5	24	44	
			2	2	5	23	43	
		All Peripherals disabled	180	23	29(4)	63	96(4)	
			168	21	25	50	76	
			150	19	23	48	74	
			144	17	31	43	67	
			120	13	16	34	54	
			90	10	13	31	51	
			60	7	10	28	48	
			30	5	7	25	45	
			25	4	7	25	45	
			16	2	5	23	43	
			8	2	5	23	43	
			4	2	5	23	43	
			2	2	4	23	42	

1. Guaranteed based on test during characterization.
2. When analog peripheral blocks such as ADCs, DACs, HSE, LSE, HSI, or LSI are ON, an additional power consumption should be considered.
3. When the ADC is ON (ADON bit set in the ADC_CR2 register), add an additional power consumption of 1.6 mA per ADC for the analog part.
4. Guaranteed by test in production.

Table 30. Typical and maximum current consumption in Standby mode

Symbol	Parameter	Conditions	Typ(1)			Max(2)			Unit
			T_A = 25 °C			T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
			V_{DD} = 1.7 V	V_{DD}= 2.4 V	V_{DD} = 3.3 V	V_{DD} = 3.3 V			
I_{DD_STBY}	Supply current in Standby mode	Backup SRAM ON, RTC and LSE oscillator OFF	1.7	2.5	2.9	6(3)	18	35(3)	µA
		Backup SRAM OFF, RTC and LSE oscillator OFF	1.0	1.8	2.20	5(3)	15	30(3)	
		Backup SRAM OFF, RTC ON and LSE oscillator in Power Drive mode	1.7	2.7	3.2	7	20	39	
		Backup SRAM ON, RTC ON and LSE oscillator in Power Drive mode	2.4	3.4	4.0	8	25	48	
		Backup SRAM ON, RTC ON and LSE oscillator in High Drive mode	3.2	4.2	4.8	10	29	57	
		Backup SRAM OFF, RTC ON and LSE oscillator in High Drive mode	2.5	3.5	4.1	8	25	48	

1. PDR is off for V_{DD}=1.7 V. When the PDR is OFF (internal reset OFF), the typical current consumption is reduced by additional 1.2 µA
2. Based on characterization, not tested in production unless otherwise specified.
3. Based on characterization, tested in production.

Figure 35 and *Figure 36* show the main PLL output clock waveforms in center spread and down spread modes, where:

F0 is f_{PLL_OUT} nominal.

T_{mode} is the modulation period.

md is the modulation depth.

Figure 35. PLL output clock waveforms in center spread mode

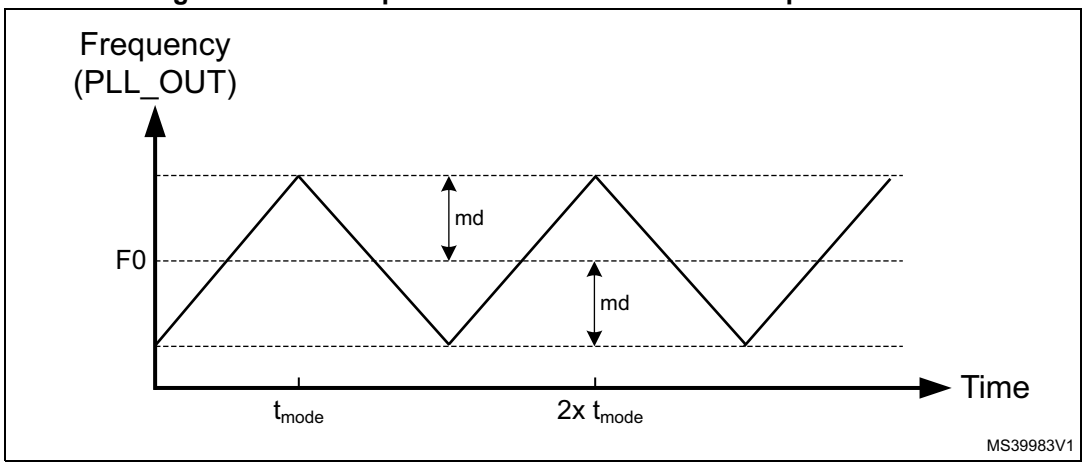
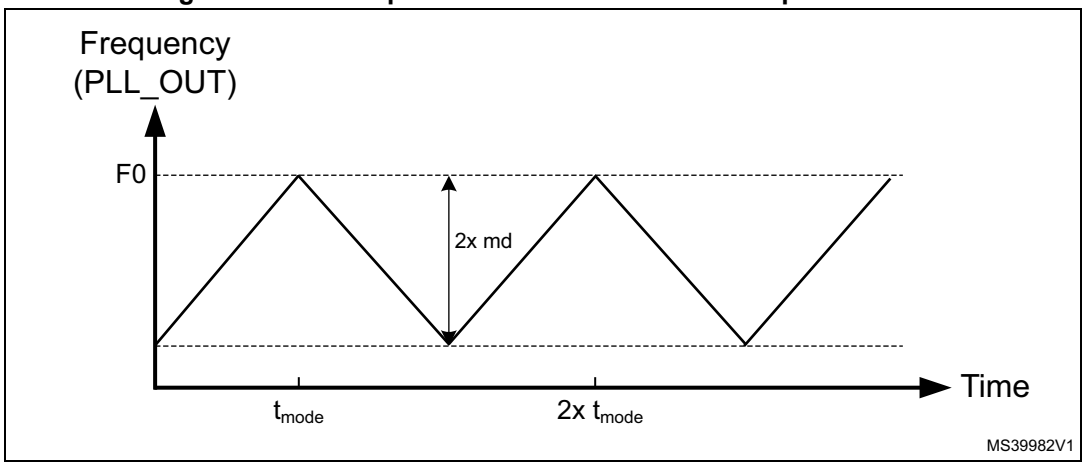


Figure 36. PLL output clock waveforms in down spread mode



5.3.13 MIPI D-PHY characteristics

The parameters given in *Table 45* and *Table 46* are derived from tests performed under temperature and V_{DD} supply voltage conditions summarized in *Table 17*.

Table 45. MIPI D-PHY characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Hi-Speed Input/Output Characteristics						
U_{INST}	UI instantaneous	-	2	-	12.5	ns

Figure 37. MIPI D-PHY HS/LP clock lane transition timing diagram

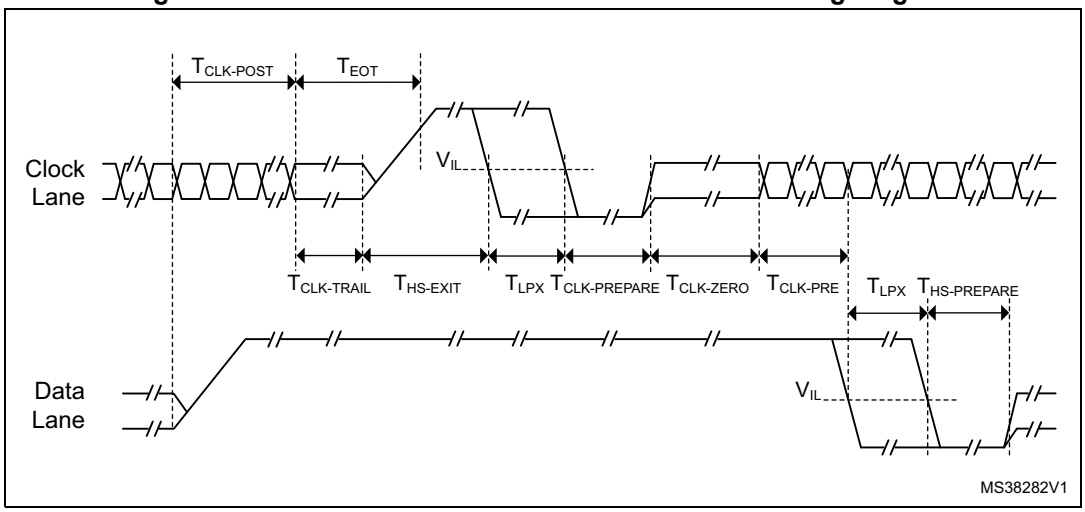
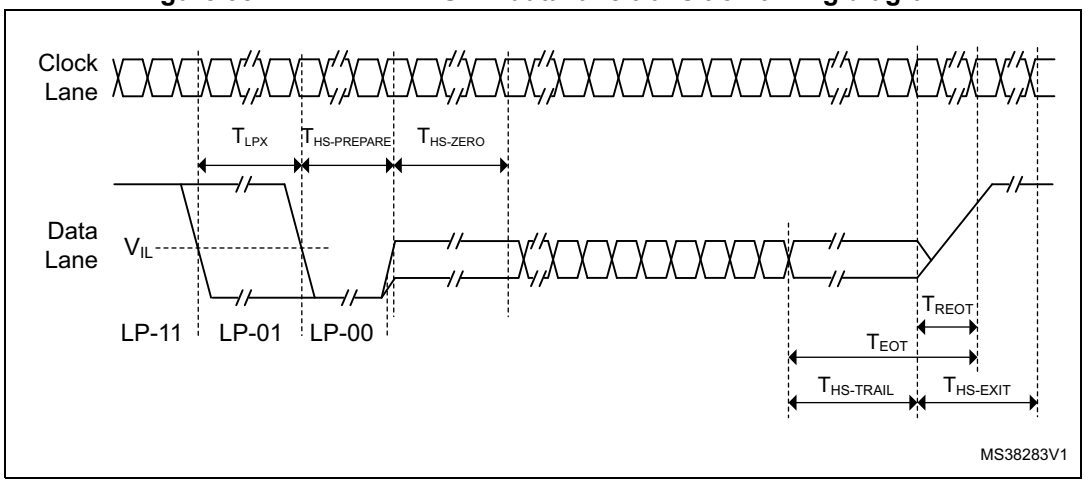


Figure 38. MIPI D-PHY HS/LP data lane transition timing diagram



5.3.14 MIPI D-PHY PLL characteristics

The parameters given in *Table 47* are derived from tests performed under temperature and V_{DD} supply voltage conditions summarized in *Table 17*.

Table 47. DSI-PLL characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PLL_IN}	PLL input clock	-	4	-	100	MHz
f_{PLL_INFIN}	PFD input clock	-	4	-	25	
f_{PLL_OUT}	PLL multiplier output clock	-	31.25	-	500	
f_{VCO_OUT}	PLL VCO output	-	500	-	1000	
t_{LOCK}	PLL lock time	-	-	-	200	µs

Output voltage levels

Unless otherwise specified, the parameters given in *Table 59* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 17*. All I/Os are CMOS and TTL compliant.

Table 59. Output voltage characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}(1)	Output low level voltage for an I/O pin	CMOS port(2) I_{IO} = +8 mA 2.7 V ≤V_{DD} ≤3.6 V	-	0.4	V
V_{OH}(3)	Output high level voltage for an I/O pin		V_{DD} − 0.4	-	
V_{OL} (1)	Output low level voltage for an I/O pin	TTL port(2) I_{IO} =+ 8mA 2.7 V ≤V_{DD} ≤3.6 V	-	0.4	
V_{OH} (3)	Output high level voltage for an I/O pin		2.4	-	
V_{OL}(1)	Output low level voltage for an I/O pin	I_{IO} = +20 mA 2.7 V ≤V_{DD} ≤3.6 V	-	1.3(4)	
V_{OH}(3)	Output high level voltage for an I/O pin		V_{DD}−1.3(4)	-	
V_{OL}(1)	Output low level voltage for an I/O pin	I_{IO} = +6 mA 1.8 V ≤V_{DD} ≤3.6 V	-	0.4(4)	
V_{OH}(3)	Output high level voltage for an I/O pin		V_{DD}−0.4(4)	-	
V_{OL}(1)	Output low level voltage for an I/O pin	I_{IO} = +4 mA 1.7 V ≤V_{DD} ≤3.6V	-	0.4(5)	
V_{OH}(3)	Output high level voltage for an I/O pin		V_{DD}−0.4(5)	-	

1. The I_{IO} current sunk by the device must always respect the absolute maximum rating specified in *Table 15*. and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS}.
2. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.
3. The I_{IO} current sourced by the device must always respect the absolute maximum rating specified in *Table 15* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VDD}.
4. Based on characterization data.
5. Guaranteed by design.

Input/output AC characteristics

The definition and values of input/output AC characteristics are given in *Figure 40* and *Table 60*, respectively.

Unless otherwise specified, the parameters given in *Table 60* are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in *Table 17*.

Table 60. I/O AC characteristics(1)(2)

OSPEEDRy [1:0] bit value(1)	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
00	$f_{max(IO)out}$	Maximum frequency(3)	C_L = 50 pF, $V_{DD} \geq$ 2.7 V	-	-	4	MHz
			C_L = 50 pF, $V_{DD} \geq$ 1.7 V	-	-	2	
			C_L = 10 pF, $V_{DD} \geq$ 2.7 V	-	-	8	
			C_L = 10 pF, $V_{DD} \geq$ 1.8 V	-	-	4	
			C_L = 10 pF, $V_{DD} \geq$ 1.7 V	-	-	3	
	$t_{f(IO)out}$/ $t_{r(IO)out}$	Output high to low level fall time and output low to high level rise time	C_L = 50 pF, V_{DD} = 1.7 V to 3.6 V	-	-	100	ns
01	$f_{max(IO)out}$	Maximum frequency(3)	C_L = 50 pF, $V_{DD} \geq$ 2.7 V	-	-	25	MHz
			C_L = 50 pF, $V_{DD} \geq$ 1.8 V	-	-	12.5	
			C_L = 50 pF, $V_{DD} \geq$ 1.7 V	-	-	10	
			C_L = 10 pF, $V_{DD} \geq$ 2.7 V	-	-	50	
			C_L = 10 pF, $V_{DD} \geq$ 1.8 V	-	-	20	
			C_L = 10 pF, $V_{DD} \geq$ 1.7 V	-	-	12.5	
	$t_{f(IO)out}$/ $t_{r(IO)out}$	Output high to low level fall time and output low to high level rise time	C_L = 50 pF, $V_{DD} \geq$ 2.7 V	-	-	10	ns
			C_L = 10 pF, $V_{DD} \geq$ 2.7 V	-	-	6	
			C_L = 50 pF, $V_{DD} \geq$ 1.7 V	-	-	20	
			C_L = 10 pF, $V_{DD} \geq$ 1.7 V	-	-	10	
10	$f_{max(IO)out}$	Maximum frequency(3)	C_L = 40 pF, $V_{DD} \geq$ 2.7 V	-	-	50(4)	MHz
			C_L = 10 pF, $V_{DD} \geq$ 2.7 V	-	-	100(4)	
			C_L = 40 pF, $V_{DD} \geq$ 1.7 V	-	-	25	
			C_L = 10 pF, $V_{DD} \geq$ 1.8 V	-	-	50	
			C_L = 10 pF, $V_{DD} \geq$ 1.7 V	-	-	42.5	
	$t_{f(IO)out}$/ $t_{r(IO)out}$	Output high to low level fall time and output low to high level rise time	C_L = 40 pF, $V_{DD} \geq$2.7 V	-	-	6	ns
			C_L = 10 pF, $V_{DD} \geq$ 2.7 V	-	-	4	
			C_L = 40 pF, $V_{DD} \geq$ 1.7 V	-	-	10	
			C_L = 10 pF, $V_{DD} \geq$ 1.7 V	-	-	6	

1. Guaranteed based on test during characterization.
2. Spikes with widths below $t_{AF(min)}$ are filtered.
3. Spikes with widths above $t_{AF(max)}$ are not filtered

SPI interface characteristics

Unless otherwise specified, the parameters given in *Table 64* for the SPI interface are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in *Table 17*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: 0.5 V_{DD}

Refer to *Section 5.3.20* for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO for SPI).

Table 64. SPI dynamic characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode, 2.7 V≤V_{DD}≤3.6 V, SPI1,4,5,6,	-	-	45	MHz
		Master mode, 1.71 V≤V_{DD}≤3.6 V, SPI1,4,5,6	-	-	22.5(2)	
		Master transmitter mode, 1.7 V≤V_{DD}≤3.6 V, SPI1,4,5,6	-	-	45	
		Slave full duplex mode, 2.7 V≤V_{DD}≤3.6 V, SPI1,4,5,6	-	-	22.5	
		Slave transmitter mode, 1.71 V≤V_{DD}≤3.6 V, SPI1,4,5,6	-	-	33	
		Slave transmitter mode, 2.7 V≤V_{DD}≤3.6 V, SPI1,4,5,6	-	-	45	
		Slave mode, 1.71 V≤V_{DD}≤3.6 V, SPI2,3	-	-	22.5	
Duty(SCK)	Duty cycle of SPI clock frequency	Slave mode	30	50	70	%

Figure 44. SPI timing diagram - master mode(1)

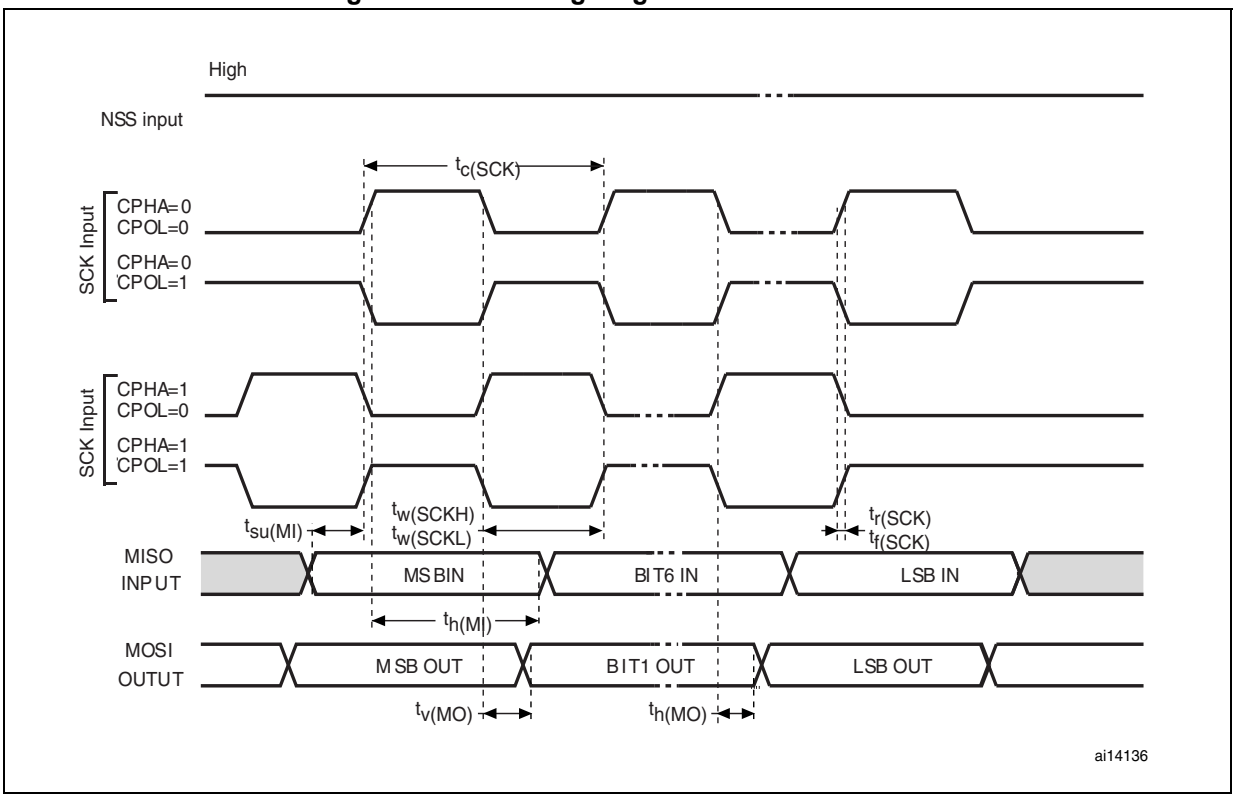
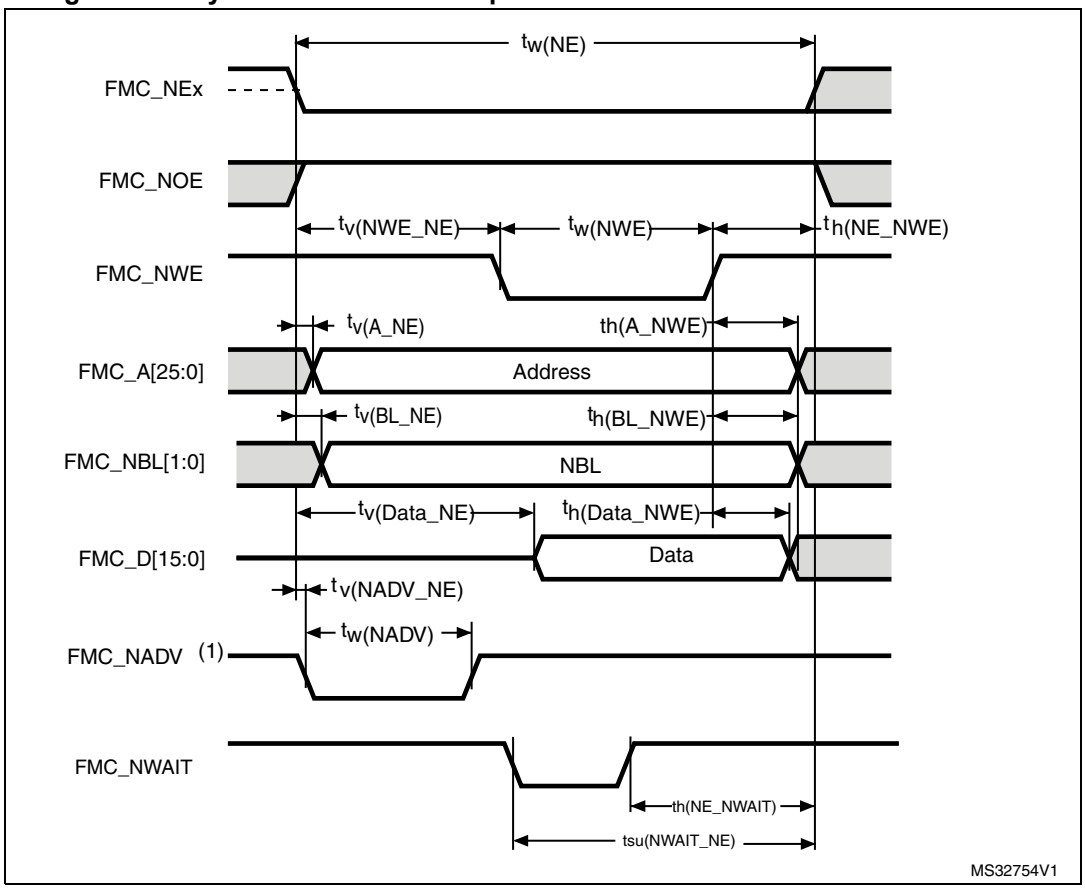


Figure 60. Asynchronous non-multiplexed SRAM/PSRAM/NOR write waveforms



1. Mode 2/B, C and D only. In Mode 1, FMC_NADV is not used.

Table 90. Asynchronous non-multiplexed SRAM/PSRAM/NOR write timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$3T_{HCLK}$	$3T_{HCLK}+1$	ns
$t_{v(NWE_NE)}$	FMC_NEx low to FMC_NWE low	$T_{HCLK} - 0.5$	$T_{HCLK}+ 0.5$	
$t_{w(NWE)}$	FMC_NWE low time	T_{HCLK}	$T_{HCLK}+ 0.5$	
$t_{h(NE_NWE)}$	FMC_NWE high to FMC_NE high hold time	$T_{HCLK} +1.5$	-	
$t_{v(A_NE)}$	FMC_NEx low to FMC_A valid	-	0	
$t_{h(A_NWE)}$	Address hold time after FMC_NWE high	$T_{HCLK}+0.5$	-	
$t_{v(BL_NE)}$	FMC_NEx low to FMC_BL valid	-	1.5	
$t_{h(BL_NWE)}$	FMC_BL hold time after FMC_NWE high	$T_{HCLK}+0.5$	-	
$t_{v(Data_NE)}$	Data to FMC_NEx low to Data valid	-	$T_{HCLK}+ 2$	
$t_{h(Data_NWE)}$	Data hold time after FMC_NWE high	$T_{HCLK}+0.5$	-	
$t_{v(NADV_NE)}$	FMC_NEx low to FMC_NADV low	-	0.5	
$t_{w(NADV)}$	FMC_NADV low time	-	$T_{HCLK}+ 0.5$	

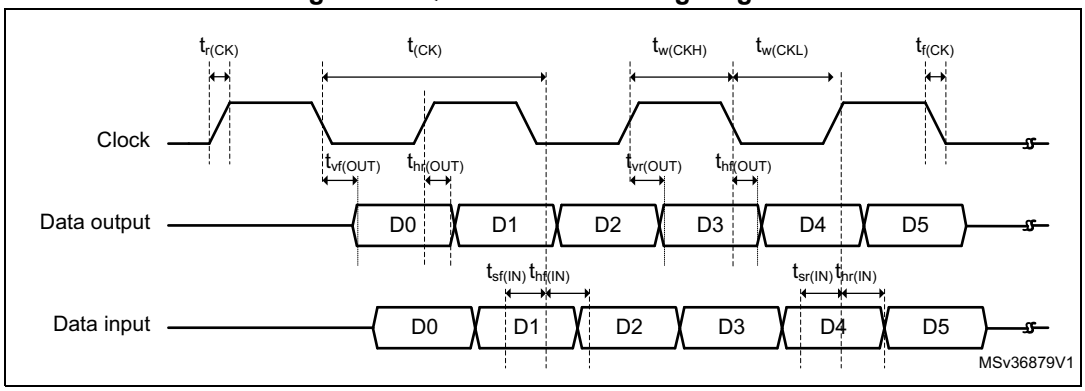
1. Based on test during characterization.

Table 107. Quad-SPI characteristics in DDR mode(1)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
F_{ck} $1/t_{(CK)}$	Quad-SPI clock frequency	2.7 V ≤ V_{DD} ≤ 3.6 V, C_L = 20 pF	-	-	80	MHz
		1.71 V ≤ V_{DD} ≤ 3.6 V, C_L = 15 pF	-	-	70	
$t_{w(CKH)}$	Quad-SPI clock high time	-	$t_{(CK)}/2-1$	-	$t_{(CK)}/2$	ns
$t_{w(CKL)}$	Quad-SPI clock low time	-	$t_{(CK)}/2$	-	$t_{(CK)}/2+1$	
$t_{sr(IN)}$ $t_{sf(IN)}$	Data input set-up time	2.7 V ≤ V_{DD} ≤ 3.6 V	2	-	-	
		1.71 V ≤ V_{DD} ≤ 3.6 V	0.5	-	-	
$t_{hr(IN)}$ $t_{hf(IN)}$	Data input hold time	2.7 V ≤ V_{DD} ≤ 3.6 V	3	-	-	
		1.71 V ≤ V_{DD} ≤ 3.6 V	4.5	-	-	
$t_{vr(OUT)}$ $t_{vf(OUT)}$	Data output valid time	DHHC=0	-	8	10.5	
		DHHC=1 Pres=1,2…	-	$T_{hclk}/2+2$	$T_{hclk}/2+2.5$	
$t_{h(OUT)}$ $t_{f(OUT)}$	Data output hold time	DHHC=0	7	-	-	
		DHHC=1 Pres=1,2…	$T_{hclk}/2+0.5$	-	-	

1. Guaranteed based on test during characterization.

Figure 74. Quad-SPI DDR timing diagram



5.3.31 Camera interface (DCMI) timing specifications

Unless otherwise specified, the parameters given in *Table 108* for DCMI are derived from tests performed under the ambient temperature, f_{HCLK} frequency and V_{DD} supply voltage summarized in *Table 17*, with the following configuration:

- DCMI_PIXCLK polarity: falling
- DCMI_VSYNC and DCMI_HSYNC polarity: high
- Data formats: 14 bits
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: 0.5 V_{DD}

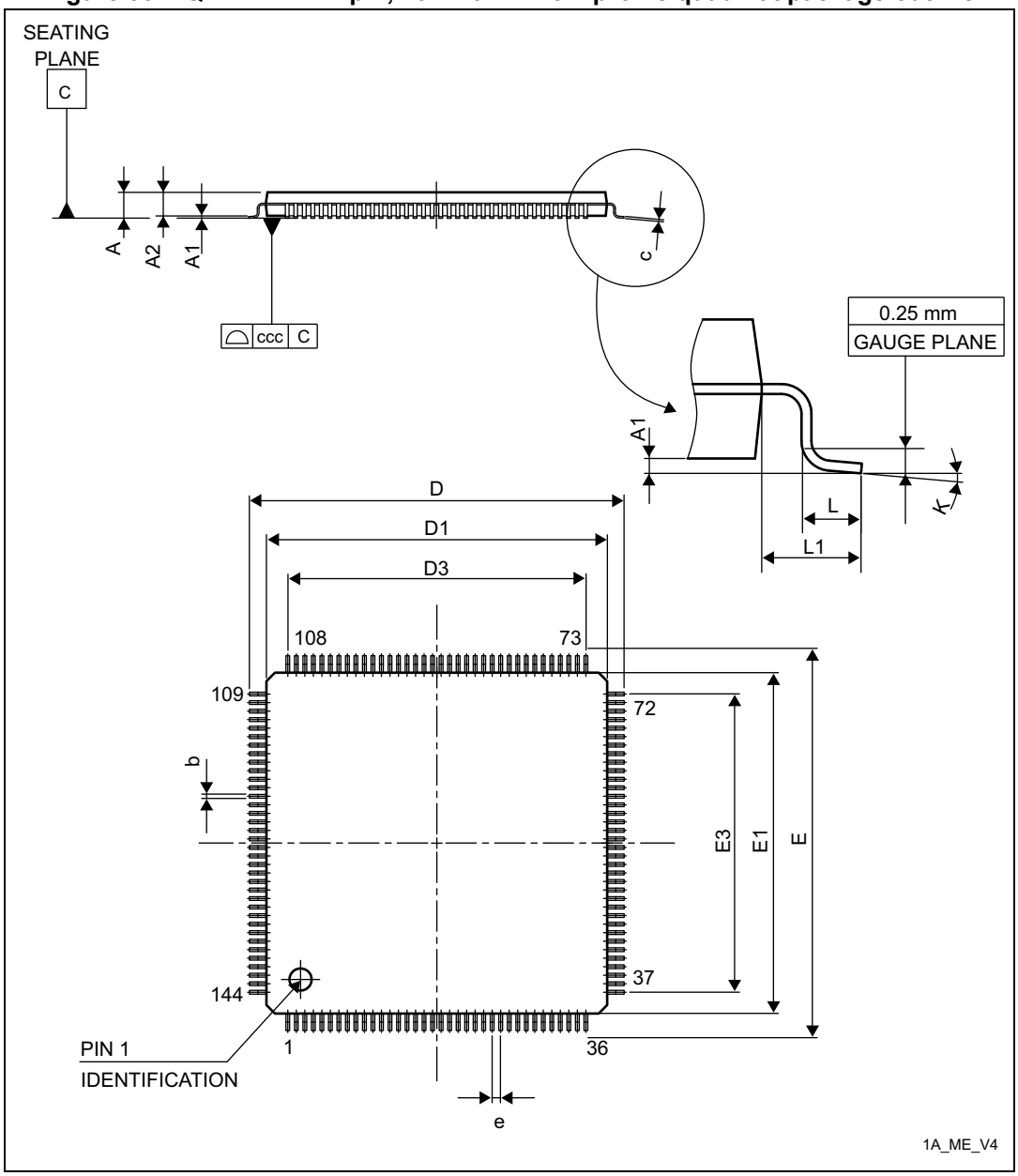
Table 113. LQPF100 - 100-pin, 14 x 14 mm low-profile quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	15.800	16.000	16.200	0.6220	0.6299	0.6378
D1	13.800	14.000	14.200	0.5433	0.5512	0.5591
D3	-	12.000	-	-	0.4724	-
E	15.800	16.000	16.200	0.6220	0.6299	0.6378
E1	13.800	14.000	14.200	0.5433	0.5512	0.5591
E3	-	12.000	-	-	0.4724	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0.0°	3.5°	7.0°	0.0°	3.5°	7.0°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

6.2 LQFP144 package information

Figure 83. LQFP144 - 144-pin, 20 x 20 mm low-profile quad flat package outline



1. Drawing is not to scale.

Table 115. WLCSP168 - 168-pin, 4.891 x 5.692 mm, 0.4 mm pitch wafer level chip scale package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.525	0.555	0.585	0.0207	0.0219	0.0230
A1	-	0.170	-	-	0.0067	-
A2	-	0.380	-	-	0.0150	-
A3[2]	-	0.025	-	-	0.0010	-
b[3]	0.220	0.250	0.280	0.0087	0.0098	0.0110
D	4.856	4.891	4.926	0.1912	0.1926	0.1939
E	5.657	5.692	5.727	0.2227	0.2241	0.2255
e	-	0.400	-	-	0.0157	-
e1	-	4.400	-	-	0.1732	-
e2	-	5.200	-	-	0.2047	-
F	-	0.2455	-	-	0.0097	-
G	-	0.246	-	-	0.0097	-
aaa	-	-	0.100	-	-	0.0039
bbb	-	-	0.100	-	-	0.0039
ccc	-	-	0.100	-	-	0.0039
ddd	-	-	0.050	-	-	0.0020
eee	-	-	0.050	-	-	0.0020

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. Back side coating.
3. Dimension is measured at the maximum bump diameter parallel to primary datum Z.