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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	EBI/EMI, I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I²S, LVD, POR, PS2, PWM, WDT
Number of I/O	49
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 5.5V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/nuc100rd3an

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2 FEATURES

The equipped features are dependent on the product line and their sub products.

2.1 NuMicro™ NUC100 Features – Advanced Line

- Core
  - ARM® Cortex™-M0 core runs up to 50 MHz
  - One 24-bit system timer
  - Supports low power sleep mode
  - Single-cycle 32-bit hardware multiplier
  - NVIC for the 32 interrupt inputs, each with 4-levels of priority
  - Serial Wire Debug supports with 2 watchpoints/4 breakpoints
- Build-in LDO for wide operating voltage ranges from 2.5 V to 5.5 V
- Flash Memory
  - 32K/64K/128K bytes Flash for program code (128KB only support in NuMicro™ NUC100/NUC120 Medium Density)
  - 4KB flash for ISP loader
  - Support In-system program (ISP) application code update
  - 512 byte page erase for flash
  - Configurable data flash address and size for 128KB system, fixed 4KB data flash for the 32KB and 64KB system
  - Support 2 wire ICP update through SWD/ICE interface
  - Support fast parallel programming mode by external programmer
- SRAM Memory
  - 4K/8K/16K bytes embedded SRAM (16KB only support in NuMicro™ NUC100/NUC120 Medium Density)
  - Support PDMA mode
- PDMA (Peripheral DMA)
  - Support 9 channels PDMA for automatic data transfer between SRAM and peripherals (Only support 1 channel in NuMicro™ NUC100/NUC120 Low Density)
- Clock Control
  - Flexible selection for different applications
  - Built-in 22.1184 MHz high speed OSC for system operation
    - Trimmed to ± 1 % at +25 ℃ and V_{DD} = 5 V
    - Trimmed to ± 3 % at -40 ℃ ~ +85 ℃ and V_{DD} = 2.5 V ~ 5.5 V
  - Built-in 10 kHz low speed OSC for Watchdog Timer and Wake-up operation
  - Support one PLL, up to 50 MHz, for high performance system operation
  - External 4~24 MHz high speed crystal input for precise timing operation
  - External 32.768 kHz low speed crystal input for RTC function and low power system operation
- GPIO
  - Four I/O modes:
    - Quasi bi-direction
    - Push-Pull output
    - Open-Drain output
    - Input only with high impendence

3.2.1.2 NuMicro™ NUC100 Medium Density LQFP 64 pin

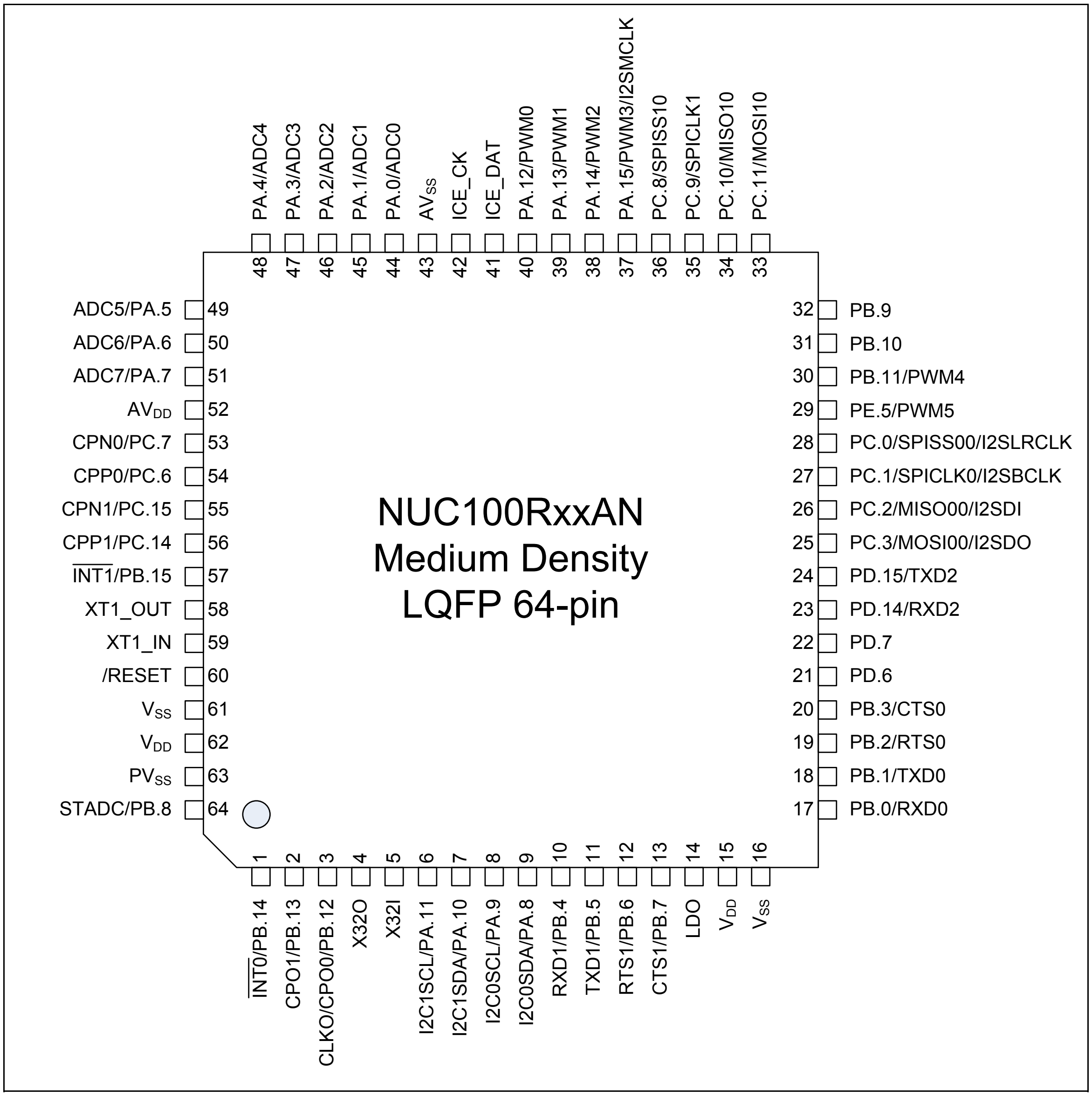


Figure 3-2 NuMicro™ NUC100 Medium Density LQFP 64-pin Pin Diagram

3.2.1.3 NuMicro™ NUC100 Medium Density LQFP 48 pin

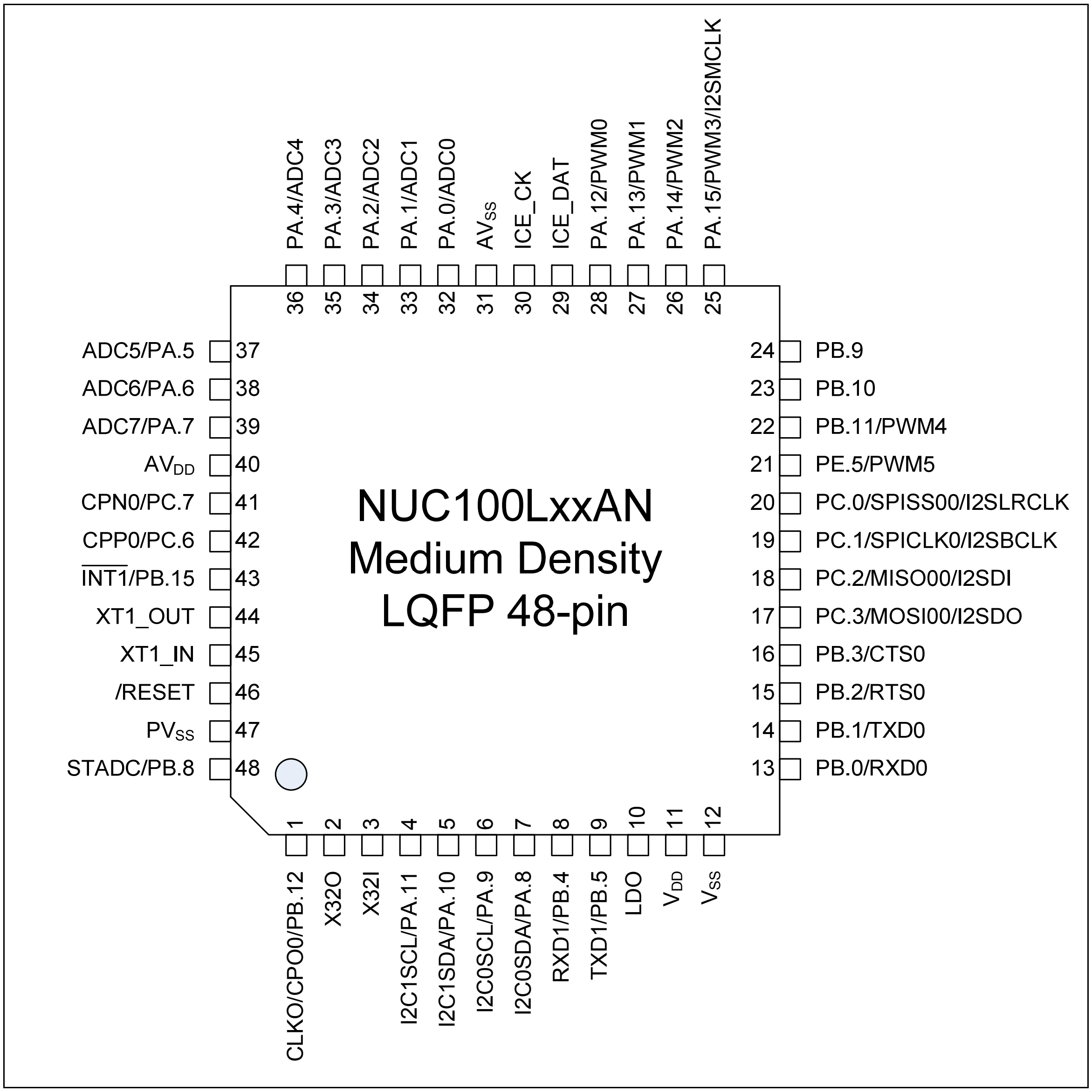


Figure 3-3 NuMicro™ NUC100 Medium Density LQFP 48-pin Pin Diagram

5.2.4 System Memory Map

NuMicro™ NUC100 Series provides 4G-byte addressing space. The memory locations assigned to each on-chip controllers are shown in the following table. The detailed register definition, memory space, and programming detailed will be described in the following sections for each on-chip peripherals. NuMicro™ NUC100 Series only supports little-endian data format.

Address Space	Token	Controllers
Flash and SRAM Memory Space		
0x0000_0000 – 0x0001_FFFF	FLASH_BA	FLASH Memory Space (128KB)
0x2000_0000 – 0x2000_3FFF	SRAM_BA	SRAM Memory Space (16KB)
0x6000_0000 – 0x6001_FFFF	EXTMEM_BA	External Memory Space (128KB) (NuMicro™ NUC100/NUC120 Low Density 64-pin Only)
AHB Controllers Space (0x5000_0000 – 0x501F_FFFF)		
0x5000_0000 – 0x5000_01FF	GCR_BA	System Global Control Registers
0x5000_0200 – 0x5000_02FF	CLK_BA	Clock Control Registers
0x5000_0300 – 0x5000_03FF	INT_BA	Interrupt Multiplexer Control Registers
0x5000_4000 – 0x5000_7FFF	GPIO_BA	GPIO Control Registers
0x5000_8000 – 0x5000_BFFF	PDMA_BA	Peripheral DMA Control Registers
0x5000_C000 – 0x5000_FFFF	FMC_BA	Flash Memory Control Registers
0x5001_0000 – 0x5001_03FF	EBI_BA	External Bus Interface Control Registers (NuMicro™ NUC100/NUC120 Low Density 64-pin Only)
APB1 Controllers Space (0x4000_0000 ~ 0x400F_FFFF)		
0x4000_4000 – 0x4000_7FFF	WDT_BA	Watchdog Timer Control Registers
0x4000_8000 – 0x4000_BFFF	RTC_BA	Real Time Clock (RTC) Control Register
0x4001_0000 – 0x4001_3FFF	TMR01_BA	Timer0/Timer1 Control Registers
0x4002_0000 – 0x4002_3FFF	I2C0_BA	I^2C0 Interface Control Registers
0x4003_0000 – 0x4003_3FFF	SPI0_BA	SPI0 with master/slave function Control Registers
0x4003_4000 – 0x4003_7FFF	SPI1_BA	SPI1 with master/slave function Control Registers
0x4004_0000 – 0x4004_3FFF	PWMA_BA	PWM0/1/2/3 Control Registers
0x4005_0000 – 0x4005_3FFF	UART0_BA	UART0 Control Registers
0x4006_0000 – 0x4006_3FFF	USBD_BA	USB 2.0 FS device Controller Registers
0x400D_0000 – 0x400D_3FFF	ACMP_BA	Analog Comparator Control Registers

Address Space	Token	Controllers
0x400E_0000 – 0x400E_FFFF	ADC_BA	Analog-Digital-Converter (ADC) Control Registers
APB2 Controllers Space (0x4010_0000 ~ 0x401F_FFFF)		
0x4010_0000 – 0x4010_3FFF	PS2_BA	PS/2 Interface Control Registers
0x4011_0000 – 0x4011_3FFF	TMR23_BA	Timer2/Timer3 Control Registers
0x4012_0000 – 0x4012_3FFF	I2C1_BA	I^2C1 Interface Control Registers
0x4013_0000 – 0x4013_3FFF	SPI2_BA	SPI2 with master/slave function Control Registers (NuMicro™ NUC100/NUC120 Medium Density Only)
0x4013_4000 – 0x4013_7FFF	SPI3_BA	SPI3 with master/slave function Control Registers (NuMicro™ NUC100/NUC120 Medium Density Only)
0x4014_0000 – 0x4014_3FFF	PWMB_BA	PWM4/5/6/7 Control Registers (NuMicro™ NUC100/NUC120 Medium Density Only)
0x4015_0000 – 0x4015_3FFF	UART1_BA	UART1 Control Registers
0x4015_4000 – 0x4015_7FFF	UART2_BA	UART2 Control Registers (NuMicro™ NUC100/NUC120 Medium Density Only)
0x401A_0000 – 0x401A_3FFF	I2S_BA	I^2S Interface Control Registers
System Controllers Space (0xE000_E000 ~ 0xE000_EFFF)		
0xE000_E010 – 0xE000_E0FF	SCS_BA	System Timer Control Registers
0xE000_E100 – 0xE000_ECFF	SCS_BA	External Interrupt Controller Control Registers
0xE000_ED00 – 0xE000_ED8F	SCS_BA	System Control Registers

Table 5-1 Address Space Assignments for On-Chip Controllers

5.2.5 System Timer (SysTick)

The Cortex-M0 includes an integrated system timer, SysTick. SysTick provides a simple, 24-bit clear-on-write, decrementing, wrap-on-zero counter with a flexible control mechanism. The counter can be used as a Real Time Operating System (RTOS) tick timer or as a simple counter.

When system timer is enabled, it will count down from the value in the SysTick Current Value Register (SYST_CVR) to zero, and reload (wrap) to the value in the SysTick Reload Value Register (SYST_RVR) on the next clock cycle, then decrement on subsequent clocks. When the counter transitions to zero, the COUNTFLAG status bit is set. The COUNTFLAG bit clears on reads.

The SYST_CVR value is UNKNOWN on reset. Software should write to the register to clear it to zero before enabling the feature. This ensures the timer will count from the SYST_RVR value rather than an arbitrary value when it is enabled.

If the SYST_RVR is zero, the timer will be maintained with a current value of zero after it is reloaded with this value. This mechanism can be used to disable the feature independently from the timer enable bit.

For more detailed information, please refer to the documents "ARM® Cortex™-M0 Technical Reference Manual" and "ARM® v6-M Architecture Reference Manual".

5.2.6.2 *Vector Table*

When any interrupts is accepted, the processor will automatically fetch the starting address of the interrupt service routine (ISR) from a vector table in memory. For ARMv6-M, the vector table base address is fixed at 0x00000000. The vector table contains the initialization value for the stack pointer on reset, and the entry point addresses for all exception handlers. The vector number on previous page defines the order of entries in the vector table associated with exception handler entry as illustrated in previous section.

Vector Table Word Offset	Description
0	SP_main – The Main stack pointer
Vector Number	Exception Entry Pointer using that Vector Number

Table 5-4 Vector Table Format

5.2.6.3 *Operation Description*

NVIC interrupts can be enabled and disabled by writing to their corresponding Interrupt Set-Enable or Interrupt Clear-Enable register bit-field. The registers use a write-1-to-enable and write-1-to-clear policy, both registers reading back the current enabled state of the corresponding interrupts. When an interrupt is disabled, interrupt assertion will cause the interrupt to become Pending, however, the interrupt will not activate. If an interrupt is Active when it is disabled, it remains in its Active state until cleared by reset or an exception return. Clearing the enable bit prevents new activations of the associated interrupt.

NVIC interrupts can be pended/un-pended using a complementary pair of registers to those used to enable/disable the interrupts, named the Set-Pending Register and Clear-Pending Register respectively. The registers use a write-1-to-enable and write-1-to-clear policy, both registers reading back the current pended state of the corresponding interrupts. The Clear-Pending Register has no effect on the execution status of an Active interrupt.

NVIC interrupts are prioritized by updating an 8-bit field within a 32-bit register (each register supporting four interrupts).

The general registers associated with the NVIC are all accessible from a block of memory in the System Control Space and will be described in next section.

5.3 Clock Controller

5.3.1 Overview

The clock controller generates the clocks for the whole chip, including system clocks and all peripheral clocks. The clock controller also implements the power control function with the individually clock ON/OFF control, clock source selection and a clock divider. The chip will not enter power down mode until CPU sets the power down enable bit (PWR_DOWN_EN) and Cortex-M0 core executes the WFI instruction. After that, chip enter power down mode and wait for wake-up interrupt source triggered to leave power down mode. In the power down mode, the clock controller turns off the external 4~24 MHz high speed crystal and internal 22.1184 MHz high speed oscillator to reduce the overall system power consumption.

the PWM counter 0/1/2/3 will be reload at this moment.

The maximum captured frequency that PWM can capture is confined by the capture interrupt latency. When capture interrupt occurred, software will do at least three steps, they are: Read PIIR to get interrupt source and Read CRLRx/CFLRx(x=0~3) to get capture value and finally write 1 to clear PIIR to zero. If interrupt latency will take time T0 to finish, the capture signal mustn't transition during this interval (T0). In this case, the maximum capture frequency will be 1/T0. For example:

HCLK = 50 MHz, PWM_CLK = 25 MHz, Interrupt latency is 900 ns

So the maximum capture frequency will is 1/900ns ≈ 1000 kHz

5.6.2 Features

5.6.2.1 PWM function features:

- PWM group has two PWM generators. Each PWM generator supports one 8-bit prescaler, one clock divider, two PWM-timers (down counter), one dead-zone generator and two PWM outputs.
- Up to 16-bit resolution
- PWM Interrupt request synchronized with PWM period
- One-shot or Auto-reload mode PWM
- Up to 2 PWM group (PWMA/PWMB) to support 8 PWM channels or 4 PWM paired channels (only 1 PWM group support for NuMicro™ NUC100/NUC120 Low Density)

5.6.2.2 Capture Function Features:

- Timing control logic shared with PWM Generators
- Support 8 Capture input channels shared with 8 PWM output channels (NuMicro™ NUC100/NUC120 Low Density only support 4 Capture input channels shared with 4 PWM output channels)
- Each channel supports one rising latch register (CRLR), one falling latch register (CFLR) and Capture interrupt flag (CAPIFx)

5.10.2 Features

- 18-bit free running counter to avoid chip from Watchdog timer reset before the delay time expires.
- Selectable time-out interval (2^4 ~ 2^{18}) and the time out interval is 104 ms ~ 26.3168 s (if WDT_CLK = 10 kHz).
- Reset period = (1 / 10 kHz) * 63, if WDT_CLK = 10 kHz.

5.11 UART Interface Controller (UART)

NuMicro™ NUC100/NUC120 Medium Density provides up to three channels of Universal Asynchronous Receiver/Transmitters (UART). UART0 supports High Speed UART and UART1~2 perform Normal Speed UART, besides, only UART0 and UART1 support flow control function. NuMicro™ NUC100/NUC120 Low Density only supports UART0 and UART1.

5.11.1 Overview

The Universal Asynchronous Receiver/Transmitter (UART) performs a serial-to-parallel conversion on data received from the peripheral, and a parallel-to-serial conversion on data transmitted from the CPU. The UART controller also supports IrDA SIR Function and RS-485 mode functions. Each UART channel supports seven types of interrupts including transmitter FIFO empty interrupt (INT_THRE), receiver threshold level reaching interrupt (INT_RDA), line status interrupt (parity error or framing error or break interrupt) (INT_RLS), receiver buffer time out interrupt (INT_TOUT), MODEM/Wake-up status interrupt (INT_MODEM) and Buffer error interrupt (INT_BUF_ERR). Interrupts of UART0 and UART2 share the interrupt number 12 (vector number is 28); Interrupt number 13 (vector number is 29) only supports UART1 interrupt. Refer to Nested Vectored Interrupt Controller chapter for System Interrupt Map.

The UART0 is built-in with a 64-byte transmitter FIFO (TX_FIFO) and a 64-byte receiver FIFO (RX_FIFO) that reduces the number of interrupts presented to the CPU and the UART1~2 are equipped 16-byte transmitter FIFO (TX_FIFO) and 16-byte receiver FIFO (RX_FIFO). The CPU can read the status of the UART at any time during the operation. The reported status information includes the type and condition of the transfer operations being performed by the UART, as well as 4 error conditions (parity error, framing error, break interrupt and buffer error) probably occur while receiving data. The UART includes a programmable baud rate generator that is capable of dividing clock input by divisors to produce the serial clock that transmitter and receiver need. The baud rate equation is Baud Rate = UART_CLK / M * [BRD + 2], where M and BRD are defined in Baud Rate Divider Register (UA_BAUD). Table 5-6 lists the equations in the various conditions and Table 5-7 list the UART baud rate setting table.

Mode	DIV_X_EN	DIV_X_ONE	Divider X	BRD	Baud rate equation
0	0	0	B	A	UART_CLK / [16 * (A+2)]
1	1	0	B	A	UART_CLK / [(B+1) * (A+2)] , B must >= 8
2	1	1	Don’t care	A	UART_CLK / (A+2), A must >=3

Table 5-6 UART Baud Rate Equation

5.14 Analog-to-Digital Converter (ADC)

5.14.1 Overview

NuMicro™ NUC100 Series contains one 12-bit successive approximation analog-to-digital converters (SAR A/D converter) with 8 input channels. The A/D converter supports three operation modes: single, single-cycle scan and continuous scan mode. The A/D converters can be started by software and external STADC pin.

5.14.2 Features

- Analog input voltage range: 0~V_{REF}
- 12-bit resolution and 10-bit accuracy is guaranteed
- Up to 8 single-end analog input channels or 4 differential analog input channels
- Maximum ADC clock frequency is 16 MHz
- Up to 600K SPS conversion rate
- Three operating modes
  - Single mode: A/D conversion is performed one time on a specified channel
  - Single-cycle scan mode: A/D conversion is performed one cycle on all specified channels with the sequence from the lowest numbered channel to the highest numbered channel
  - Continuous scan mode: A/D converter continuously performs Single-cycle scan mode until software stops A/D conversion
- An A/D conversion can be started by
  - Software write 1 to ADST bit
  - External pin STADC
- Conversion results are held in data registers for each channel with valid and overrun indicators
- Conversion result can be compared with specify value and user can select whether to generate an interrupt when conversion result is equal to the compare register setting
- Channel 7 supports 3 input sources: external analog voltage, internal bandgap voltage, and internal temperature sensor output
- Support Self-calibration to minimize conversion error

7.2 DC Electrical Characteristics

7.2.1 NuMicro™ NUC100/NUC120 Medium Density DC Electrical Characteristics

(V_{DD}-V_{SS}=3.3 V, TA = 25°C, FOSC = 50 MHz unless otherwise specified.)

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Operation voltage	V_{DD}	2.5		5.5	V	V_{DD} =2.5 V ~ 5.5 V up to 50 MHz
Power Ground	V_{SS} AV_{SS}	-0.3			V	
LDO Output Voltage	V_{LDO}	-10%	2.5	+10%	V	V_{DD} > 2.7 V
Analog Operating Voltage	AV_{DD}	0		V_{DD}	V	
Analog Reference Voltage	Vref	0		AV_{DD}	V	
Operating Current Normal Run Mode @ 50 MHz	I_{DD1}		54		mA	V_{DD} = 5.5 V@50 MHz, enable all IP and PLL, XTAL=12 MHz
	I_{DD2}		31		mA	V_{DD} = 5.5 V@ 50 MHz, disable all IP and enable PLL, XTAL=12 MHz
	I_{DD3}		51		mA	V_{DD} = 3 V@50 MHz, enable all IP and PLL, XTAL=12 MHz
	I_{DD4}		28		mA	V_{DD} = 3 V@50 MHz, disable all IP and enable PLL, XTAL=12 MHz
Operating Current Normal Run Mode @ 12 MHz	I_{DD5}		22		mA	V_{DD} = 5.5 V@12 MHz, enable all IP and disable PLL, XTAL=12 MHz
	I_{DD6}		14		mA	V_{DD} = 5.5 V@12 MHz, disable all IP and disable PLL, XTAL=12 MHz
	I_{DD7}		20		mA	V_{DD} = 3 V@12MHz, enable all IP and disable PLL, XTAL=12 MHz

Note:

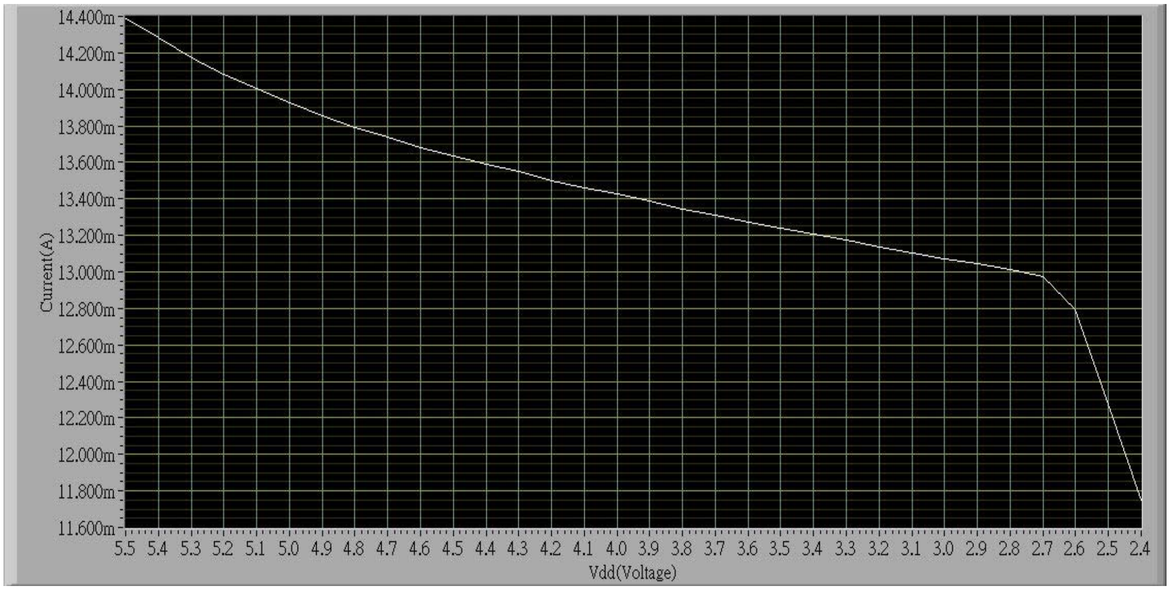
1. /RESET pin is a Schmitt trigger input.

2. Crystal Input is a CMOS input.

3. Pins of PA, PB, PC, PD and PE can source a transition current when they are being externally driven from 1 to 0. In the condition of V_{DD}=5.5 V, 5he transition current reaches its maximum value when V_{IN} approximates to 2 V.

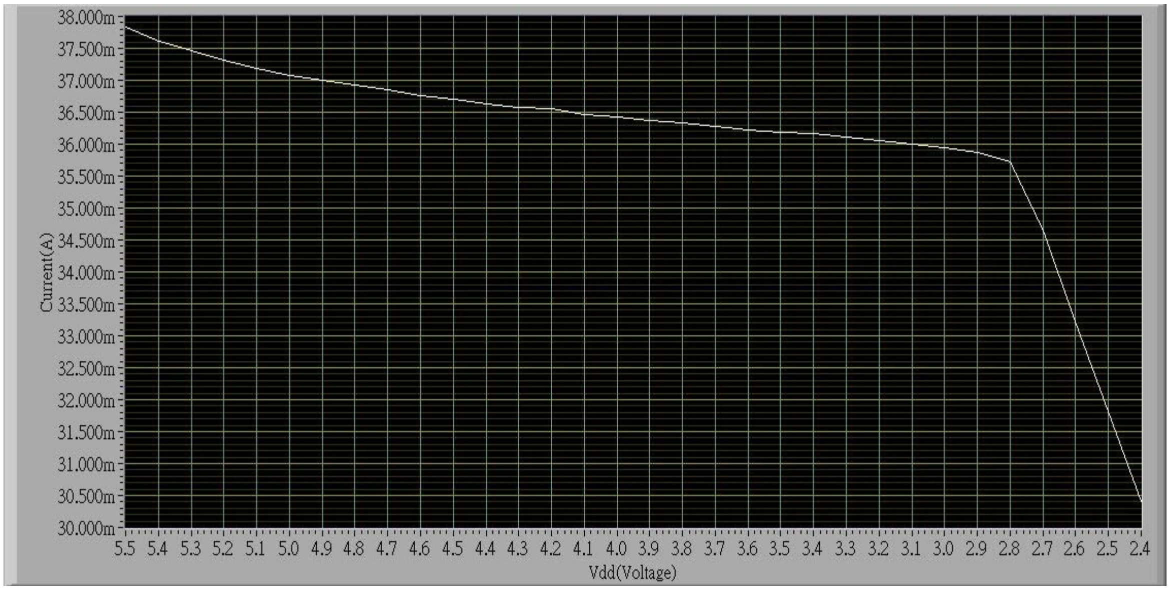
3. XTAL clock = 12 MHz, PLL enable, all-IP disable

Unit: mA



4. XTAL clock = 12 MHz, PLL enable, all-IP enable

Unit: mA



7.4.2 Specification of LDO and Power management

PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTE
Input Voltage	2.7	5	5.5	V	V_{DD} input voltage
Output Voltage	-10%	2.5	+10%	V	V_{DD} > 2.7 V
Temperature	-40	25	85	℃	
Cbp	-	1	-	uF	Resr=1ohm

Note:

1. It is recommended that a 10uF or higher capacitor and a 100nF bypass capacitor are connected between V_{DD} and the closest V_{SS} pin of the device.

2. For ensuring power stability, a 1uF or higher capacitor must be connected between LDO pin and the closest V_{SS} pin of the device.

7.4.3 Specification of Low Voltage Reset

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Operation voltage	-	1.7	-	5.5	V
Quiescent current	V_{DD}=5.5 V	-	-	5	uA
Temperature	-	-40	25	85	℃
Threshold voltage	Temperature=25℃	1.7	2.0	2.3	V
	Temperature=-40℃	-	2.4	-	V
	Temperature=85℃	-	1.6	-	V
Hysteresis	-	0	0	0	V

7.4.4 Specification of Brown-Out Detector

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Operation voltage	-	2.5	-	5.5	V
Quiescent current	AV_{DD}=5.5 V	-	-	125	μA
Temperature	-	-40	25	85	℃
Brown-Out voltage	BOV_VL[1:0]=11	4.3	4.5	4.7	V
	BOV_VL [1:0]=10	3.6	3.8	4.0	V
	BOV_VL [1:0]=01	2.6	2.7	2.8	V
	BOV_VL [1:0]=00	2.1	2.2	2.3	V
Hysteresis	-	30	-	150	mV

7.4.5 Specification of Power-On Reset (5 V)

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Temperature	-	-40	25	85	℃
Reset voltage	V+	-	2	-	V
Quiescent current	Vin>reset voltage	-	1	-	nA

9 REVISION HISTORY

VERSION	DATE	PAGE/ CHAP.	DESCRIPTION
V1.00	March 1, 2010	-	Preliminary version initial issued
V1.01	April 9, 2010	Ch4	Modify the block diagram
V1.02	May 31, 2010	7.2	Add operation current of DC characteristics
V1.03	Aug. 23, 2010	7.2	Modify operation current of DC characteristics
V2.00	Nov. 11, 2010	-	Update low density and selection table
V2.01	May 6, 2011	-	Remove NUC130/NUC140 Add SPI Dynamic Characteristics Remove TM0~3 of medium density Remove word “MICROWIRE” in all document
V2.02	June 20, 2011	-	Modify temperature sensor spec Revise Pin description position for multi-function T2EX, T3EX, nRD, nWR Update title of SPI Dynamic Characteristics Update BOD spec
V2.03	Jan. 2, 2012	-	1. Remove feature “Dynamic priority changing” for NVIC 2. Modify ADC analog characteristic spec 3. Revise the number of UART for NUC100 medium density selection table.

Important Notice

Nuvoton Products are neither intended nor warranted for usage in systems or equipment, any malfunction or failure of which may cause loss of human life, bodily injury or severe property damage. Such applications are deemed, "Insecure Usage".

Insecure usage includes, but is not limited to: equipment for surgical implementation, atomic energy control instruments, airplane or spaceship instruments, the control or operation of dynamic, brake or safety systems designed for vehicular use, traffic signal instruments, all types of safety devices, and other applications intended to support or sustain life.

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