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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	SAM8RC
Core Size	8-Bit
Speed	12MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	LCD, LVD, LVR, PWM, WDT
Number of I/O	26
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-SOIC (0.450", 11.40mm Width)
Supplier Device Package	32-SOP
Purchase URL	https://www.e-xfl.com/product-detail/zilog/s3f8s39xzz-so99

1.3.13 Oscillation Sources

- Main clock frequency: 0.4 MHz-12.0 MHz
- External RC for main clock
- Internal RC: 8 MHz (typ.), 4 MHz (typ.), 1 MHz (typ.), 0.5 MHz (typ.)
- On-chip free running Ring oscillator with 32 kHz frequency for 16-bit Timer 1.

1.3.14 Instruction Execution Time

- 333 ns at fx = 12 MHz (minimum, main clock)

1.3.15 Built-In Reset Circuit (LVR)

- Low-Voltage check to reset system
- V_{LVR} = 1.9/2.3/3.0/3.9 V (by the Smart Option)

1.3.16 Low Voltage Detect Circuit (LVD)

- Flag or Interrupt for voltage drop detection
- Programmable detect voltage: 2.1/2.5/3.2/4.1 V
- Enable/Disable software selectable

1.3.17 Operating Voltage Range

- 1.8 V to 5.5 V at 4 MHz (main clock)
- 2.7 V to 5.5 V at 12 MHz (main clock)

1.3.18 Package Type

- 32-pin SDIP
- 32-pin SOP
- 32-pin QFN
  32-pin LQFP

1.3.19 Operating Temperature Range

- –40°C to +85°C

1.3.20 Smart Option

- ISP-related option selectable (ROM address 3EH)
- Oscillator selection, LVR selection (ROM address 3FH)

1.6 Pin Descriptions

Table 1-1 describes the pin descriptions of 32-pin SOP (32-pin SDIP).

Table 1-1 Pin Descriptions of 32-SOP (32-SDIP)

Pin Names	Pin Type	Pin Description	Circuit Type	Pin No.	Shared Functions
P0.0 P0.1-P0.3	I/O	I/O port with bit-programmable pins Input or push-pull output and software assignable pull-ups.	E-1	8 (28) 9-11 (29-31)	ADC0/BUZ ADC1-ADC3
P0.4-P0.7				12-15 (32,1-3)	ADC4 -ADC7
P1.0	I/O	I/O port with bit-programmable pins Input or push-pull output and software assignable pull-ups.	E-1	6 (26)	ADC8
P1.1				5 (25)	ADC9
P2.0	I/O	Input or push-pull, open-drain output and software assignable pull-up. I/O port with bit-programmable pins	D-6 E-2	24 (12)	T0OUT/INT0
P2.1				25 (13)	TBOUT/INT1
P2.2				26 (14)	TACLK/INT2
P2.3		–		27 (15)	TAOUT/TACAP/INT3
P2.4		–		28 (16)	TXD1
P2.5		–		29 (17)	RXD1
P2.6		–		30 (18)	TXD0
P2.7		–		31 (19)	RXD0
P3.0	I/O	I/O port with bit-programmable pins Schmitt trigger input or push-pull, open-drain output and software assignable pull-ups.	E D-5 D-6	16 (4)	ADC10/MISO
P3.1				17 (5)	ADC11/MOSI
P3.2				18 (6)	ADC12/ SCK
P3.3				19 (7)	ADC13/NSS
P3.4				20 (8)	INT4/T2OUT/ T2CAP/ADC14
P3.5				21 (9)	INT5/T2CLK/ T1OUT/ADC15
P3.6				22 (10)	INT6/SCL/T1CLK
P3.7				23 (11)	INT7/T1CAP/ SDA

NOTE: Parentheses indicate pin number for 32-QFN package.

2.15.3 Stack Pointers (SPL, SPH)

Register locations D8H and D9H contain the 16-bit SP that is used for system stack operations. The most significant byte of the SP address, SP15–SP8, is stored in the SPH register (D8H), and the least significant byte, SP7–SP0, is stored in the SPL register (D9H). After a reset, the SP value is undetermined.

Because it only implements internal memory space in the S3F8S39/S3F8S35 microcontroller, it should initialize to an 8-bit value in the range 00H–FFH. The SPH register is not required and it can use it as a general-purpose register, if necessary.

When the SPL register contains only SP value (that is, when it points to a system stack in the register file), you can use the SPH register as a general-purpose data register.

However, if an overflow or underflow condition occurs as a result of increasing or decreasing the stack address value in the SPL register during normal stack operations, the value in the SPL register overflows (or underflows) to the SPH register. This occurs by overwriting any other data that is currently stored there. To avoid overwriting data in the SPH register, initialize the SPL value to "FFH" instead of "00H".

Example 2-4 shows how to perform stack operations in the internal register file by using PUSH and POP instructions:

Example 2-4 Standard Stack Operations Using PUSH and POP

```
LD      SPL, #0FFH      ; SPL ← FFH
                        ; (Normally, the SPL is set to 0FFH by the initialization routine)
•
•
•
PUSH    PP              ; Stack address 0FEH ← PP
PUSH    RP0             ; Stack address 0FDH ← RP0
PUSH    RP1             ; Stack address 0FCH ← RP1
PUSH    R3              ; Stack address 0FBH ← R3
•
•
•
POP     R3              ; R3 ← Stack address 0FBH
POP     RP1             ; RP1 ← Stack address 0FCH
POP     RP0             ; RP0 ← Stack address 0FDH
POP     PP              ; PP ← Stack address 0FEH
```

4.1.2 BTCON-Basic Timer Control Register (D3H, SET1)

Bit Identifier	.7	.6	. 5	.4	.3	.2	.1	.0
nRESET Value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Addressing Mode	Register addressing mode only							

.7– .4	**Watchdog Timer Function Disable Code (For System Reset)**				
	1	0	1	0	Disable watchdog timer function
	Other values				Enable watchdog timer function
.3– .2	**Basic Timer Clock Selection Bits**				
	0	0	fxx/4096		
	0	1	fxx/1024		
	1	0	fxx/128		
	1	1	Invalid selection		
.1	**Basic Timer Counter Clear Bit**				
	0	No effect			
	1	Clears the basic timer counter value (Automatically cleared to "0" after being cleared basic timer counter)			
.0	**Clock Frequency Divider Clear Bit for Basic Timer and Timer Counters**				
	0	No effect			
	1	Clear clock frequency dividers (Automatically cleared to "0" after being cleared clock frequency dividers)			

NOTE: When you write a "1" to BTCON.0 (or BTCON.1), it clears the basic timer divider (or basic timer counter). The bit is then cleared automatically to "0".

4.1.15 IRQ-Interrupt Request Register (DCH, SET1)

Bit Identifier	.7	.6	.5	.4	.3	.2	.1	.0
Reset Value	0	0	0	0	0	0	0	0
Read/Write	R	R	R	R	R	R	R	R

.7	**Level 7 (IRQ7) Request Pending Bit;**	
	0	Not pending
	1	Pending
.6	**Level 6 (IRQ6) Request Pending Bit;**	
	0	Not pending
	1	Pending
.5	**Level 5 (IRQ5) Request Pending Bit;**	
	0	Not pending
	1	Pending
.4	**Level 4 (IRQ4) Request Pending Bit;**	
	0	Not pending
	1	Pending
.3	**Level 3 (IRQ3) Request Pending Bit;**	
	0	Not pending
	1	Pending
.2	**Level 2 (IRQ2) Request Pending Bit;**	
	0	Not pending
	1	Pending
.1	**Level 1 (IRQ1) Request Pending Bit;**	
	0	Not pending
	1	Pending
.0	**Level 0 (IRQ0) Request Pending Bit;**	
	0	Not pending
	1	Pending

4.1.49 T0PS-T0 PreScalar (EDH, BANK0)

Bit Identifier	.7	.6	.5	.4	.3	.2	.1	.0
RESET Value	–	–	–	–	0	0	0	0
Read/Write	–	–	–	–	R/W	R/W	R/W	R/W
.7– .5	Not used							
.3– .0	Timer 0 Prescaler Bits							
	T0PS = T0 clock/($2^{T0PS[3-0]}$) Prescaler values above 12 are invalid							

6.6.9 BOR-Bit OR

BOR dst, src.b

BOR dst.b,src

Operation: dst (0) ← dst (0) OR src (b)

or

dst (b) ← dst (b) OR src (0)

The specified bit of the source (or the destination) is logically ORed with bit zero (LSB) of the destination (or the source). The resulting bit value is stored in the specified bit of the destination. No other bits of the destination are affected. The source is unaffected.

Flags:

C: Does not affect.

Z: Sets if the result is "0"; otherwise it clears.

S: Clears to "0".

V: Does not affect.

D: Does not affect.

H: Does not affect.

Format:

						Bytes	Cycles	Opcode (Hex)	Addr Mode dst	src
	opc	dst | b | 0	src			3	6	07	r0	Rb
	opc	src | b | 1	dst			3	6	07	Rb	r0

NOTE: In the second byte of the 3 byte instruction formats, the destination (or source) address is 4 bits, the bit address "b" is 3 bits, and the LSB address value is 1 bit.

Examples: Given: R1 = 07H and register 01H = 03H:

```
BOR     R1, 01H.1 → R1 = 07H, register 01H = 03H
BOR     01H.2, R1 → Register 01H = 07H, R1 = 07H
```

In the first example, destination working register R1 contains the value 07H (00000111B) and source register 01H the value 03H (00000011B). The statement "BOR R1, 01H.1" logically ORs bit 1 of register 01H (source) with bit 0 of R1 (destination). This leaves the same value (07H) in working register R1.

In the second example, destination register 01H contains the value 03H (00000011B) and the source working register R1 the value 07H (00000111B). The statement "BOR 01H.2, R1" logically ORs bit 2 of register 01H (destination) with bit 0 of R1 (source). This leaves the value 07H in register 01H.

6.6.20 DA-Decimal Adjust

DA dst

Operation: dst ← DA dst

The destination operand is adjusted to form two 4-bit BCD digits after an addition or subtraction operation. For addition (ADD, ADC) or subtraction (SUB, SBC). the following table indicates the operation that it performs (The operation is undefined if the destination operand was not the result of a valid addition or subtraction of BCD digits):

Instruction	Carry Before DA	Bits 4–7 Value (Hex)	H Flag Before DA	Bits 0–3 Value (Hex)	Number Added to Byte	Carry After DA
–	0	0–9	0	0–9	00	0
–	0	0–8	0	A–F	06	0
–	0	0–9	1	0–3	06	0
ADD	0	A–F	0	0–9	60	1
ADC	0	9–F	0	A–F	66	1
–	0	A–F	1	0–3	66	1
–	1	0–2	0	0–9	60	1
–	1	0–2	0	A–F	66	1
–	1	0–3	1	0–3	66	1
–	0	0–9	0	0–9	00 = – 00	0
SUB	0	0–8	1	6–F	FA = – 06	0
SBC	1	7–F	0	0–9	A0 = – 60	1
–	1	6–F	1	6–F	9A = – 66	1

Flags:

C: Sets if there was a carry from the most significant bit; otherwise it clears (see table).

Z: Sets if result is "0"; otherwise it clears.

S: Sets if result bit 7 is set; otherwise it clears.

V: Does not define.

D: Does not affect.

H: Does not affect.

Format:

						Bytes	Cycles	Opcode (Hex)	Addr Mode dst
	opc	dst				2	4	40	R
							4	41	IR

6.6.68 STOP-Stop Operation

STOP

Operation:

The STOP instruction stops both the CPU and system clock and causes the microcontroller to enter Stop Mode. During Stop Mode, the contents of on-chip CPU registers, peripheral registers, and I/O port control and data registers are retained. An external reset operation or external interrupts release the Stop Mode. For the reset operation, the RESET pin must be held to Low level until the required oscillation stabilization interval has elapsed.

Flags: Does not affect any flags.

Format:

						Bytes	Cycles	Opcode (Hex)	Addr Mode dst	src
	opc					1	4	7F	–	–

Example: The statement

STOP

Halts all microcontroller operations.

7 Clock Circuit

7.1 Overview

By Smart Option (0x3FH.2 in ROM), you can select internal RC oscillator, external RC oscillator, or external oscillator. An internal RC oscillator source provides 8 MHz, 4 MHz, 1 MHz, or 0.5 MHz depending on Smart Option.

An external RC oscillation source provides 4 MHz clock for S3F8S39/S3F8S35. An internal capacitor supports the RC oscillator circuit. An external crystal or ceramic oscillation source provides a maximum 12 MHz clock. The X_{IN} and X_{OUT} pin connect the oscillation source to the on-chip clock circuit.

Figure 7-1 illustrates the simplified external RC oscillator.

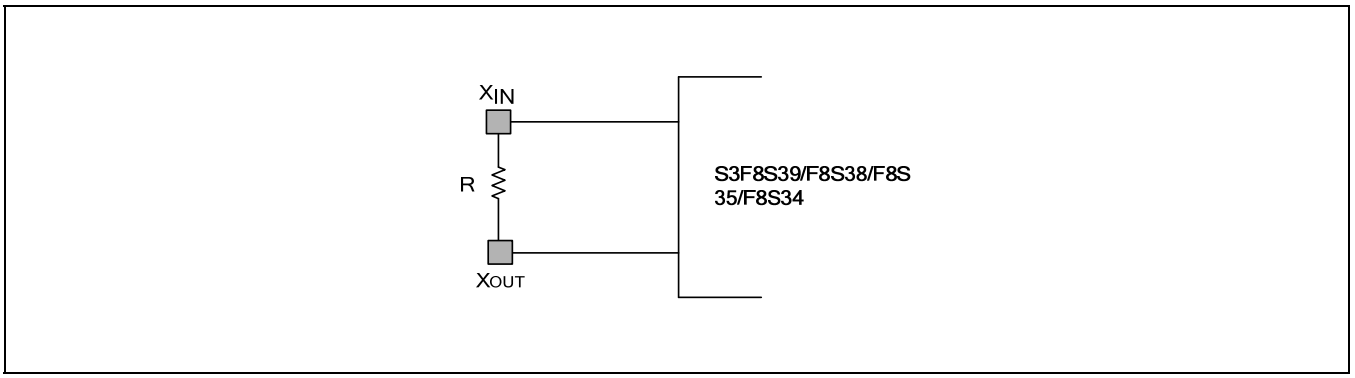

Figure 7-1 Main Oscillator Circuit (RC Oscillator with Internal Capacitor)

Figure 7-2 illustrates the simplified crystal/ceramic oscillator circuits.

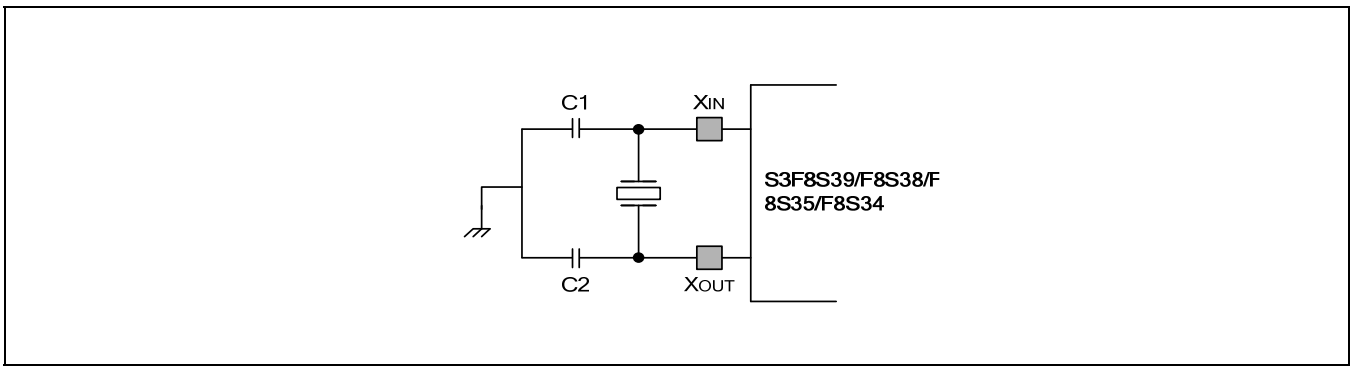

Figure 7-2 Main Oscillator Circuit (Crystal/Ceramic Oscillator)

8 RESET and Power-Down

8.1 Overview

By Smart Option (3FH.7 in ROM), you can select internal reset (LVR) or external RESET.

You can reset S3F8S39/S3F8S35 in four ways. They are:

- By external power-on-reset
- By the external nRESET input pin pulled low
- By digital basic timer timing out
- By Low Voltage Reset (LVR)

During an external power-on reset, the voltage at V_{DD} is High level and the nRESET pin is forced to Low level. The nRESET signal is an input through a schmitt trigger circuit where it is then synchronized to CPU clock. This brings the S3F8S39/S3F8S35 into a known operating status. To ensure correct start-up, you should take care that it does not release nRESET signal before the V_{DD} level is sufficient to allow MCU operation at the chosen frequency.

The nRESET pin must be held as low level for a minimum time interval after the power supply comes within tolerance to allow time for internal CPU clock oscillation to stabilize.

When a reset occurs during normal operation (with both V_{DD} and nRESET at High level), it forces the signal at the nRESET pin to low and the reset operation starts. Next, it sets all system and peripheral control registers to their default hardware reset values (Refer to *Table 8-1* for more information.)

The MCU provides a watchdog timer function to ensure graceful recovery from software malfunction. If watchdog timer is not refreshed before an end-of-counter condition (overflow) is reached, the internal reset will be activated.

The on-chip Low Voltage Reset features static reset when supply voltage is below a reference value (Typical 1.9, 2.3, 3.0, 3.9 V). With this feature, you can remove the external reset circuit while keeping the application safety. As long as the supply voltage is below the reference value, there is an internal and static reset. The MCU can start only when the supply voltage rises over the reference value.

When you calculate power consumption, remember that you should add a static current of LVR circuit a CPU operating current in any operating modes such as STOP, IDLE, and normal RUN mode.

Figure 12-5 illustrates the Timer 1 prescaler register.

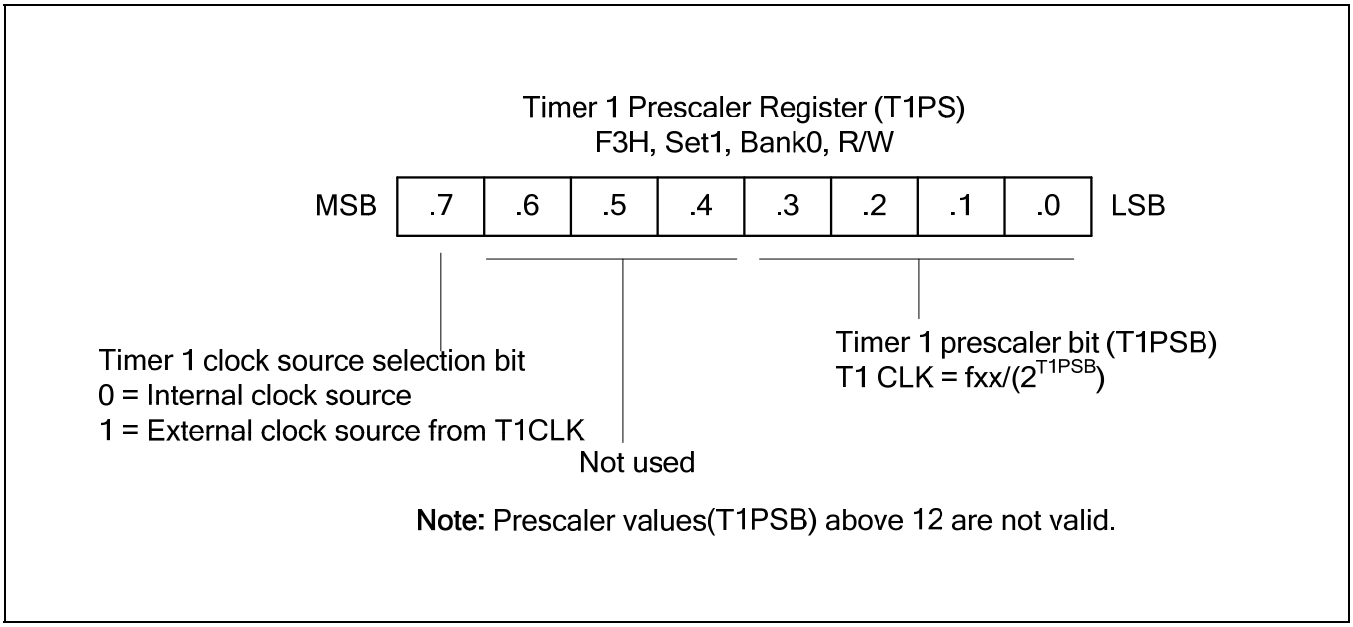

Figure 12-5 Timer 1 Prescaler Register (T1PS)

14.1.1 Watch Timer Control Register

You use the watch timer control register (WTCON) to:

- Select the watch timer interrupt time and Buzzer signal,
- Enable or disable the watch timer function.

WTCON is located in set 1, bank 1 at address FEH, and is read/write addressable using register addressing mode.

A reset clears WTCON to "00H". This disables the watch timer.

Therefore, if you want to use the watch timer, you should write appropriate value to WTCON.

Figure 14-1 illustrates the watch timer control register.

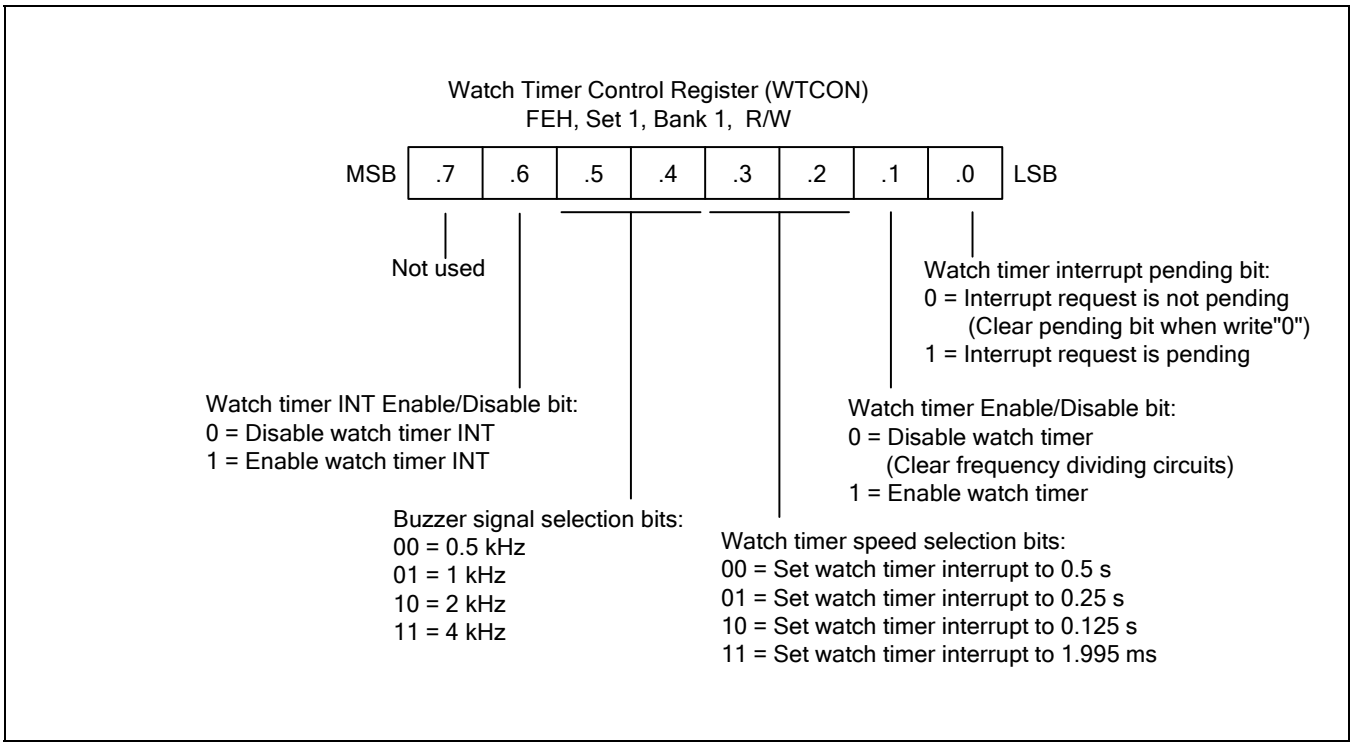

Figure 14-1 Watch Timer Control Register (WTCON)

18.1.3 Multi-Master IIC-Bus Transmit/Receive Data Shift Register

The IIC-bus data shift register, IDSR, is located at address F5H. In a transmit operation, data that is written to the IDSR is transmitted serially and MSB first. (For receive operations, the input data is written into the IDSR register LSB first.)

The ICSR.4 setting enables or disables serial transmit/receive operations. When ICSR.4 = "1", data can be written to the shift register. However, you can read the IIC-bus shift register at any time, irrespective of the current ICSR.4 setting.

Figure 18-3 illustrates the multi-master IIC-bus Tx/Rx data shift register.

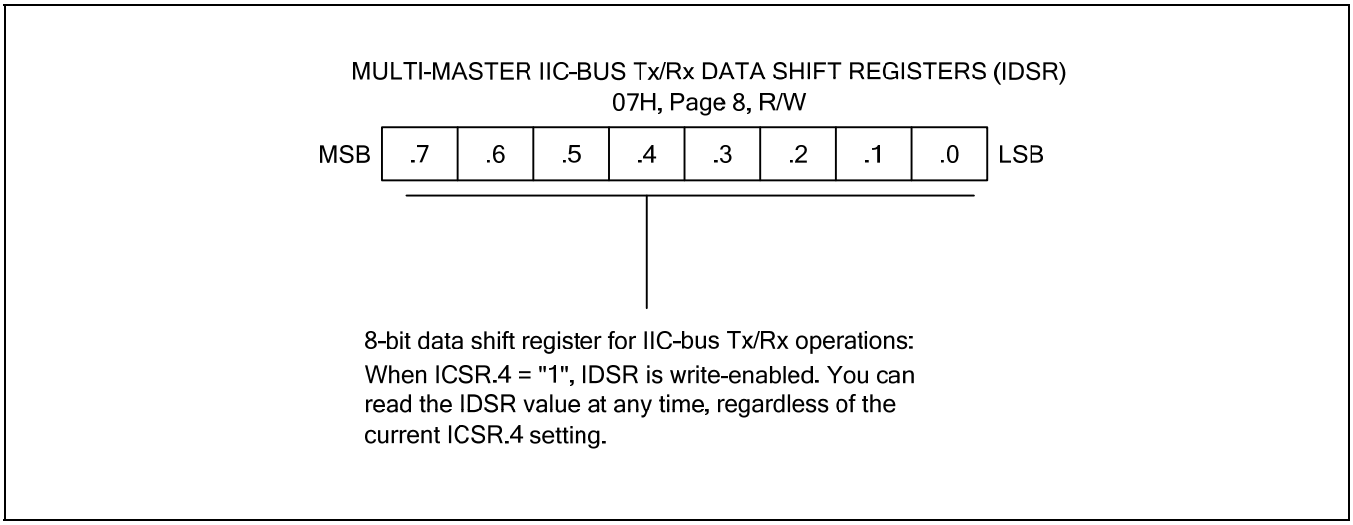

Figure 18-3 Multi-Master IIC-Bus Tx/Rx Data Shift Register (IDSR)

Figure 18-7 illustrates the input data protocol.

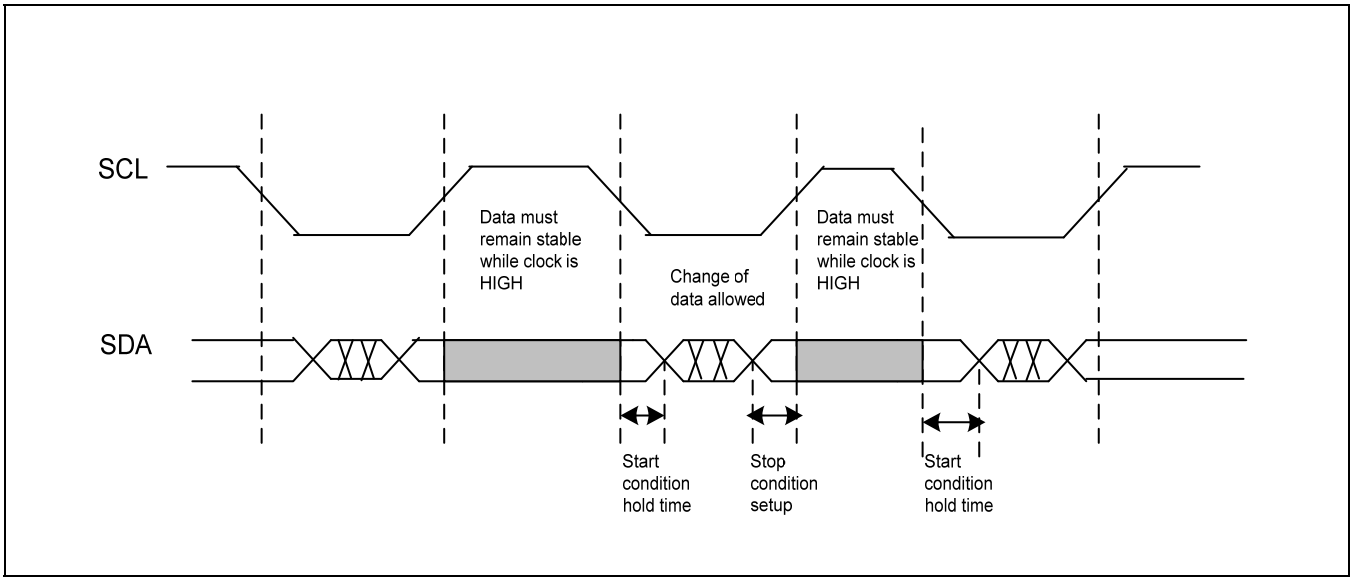

Figure 18-7 Input Data Protocol

Figure 18-8 illustrates the interrupt pending information.

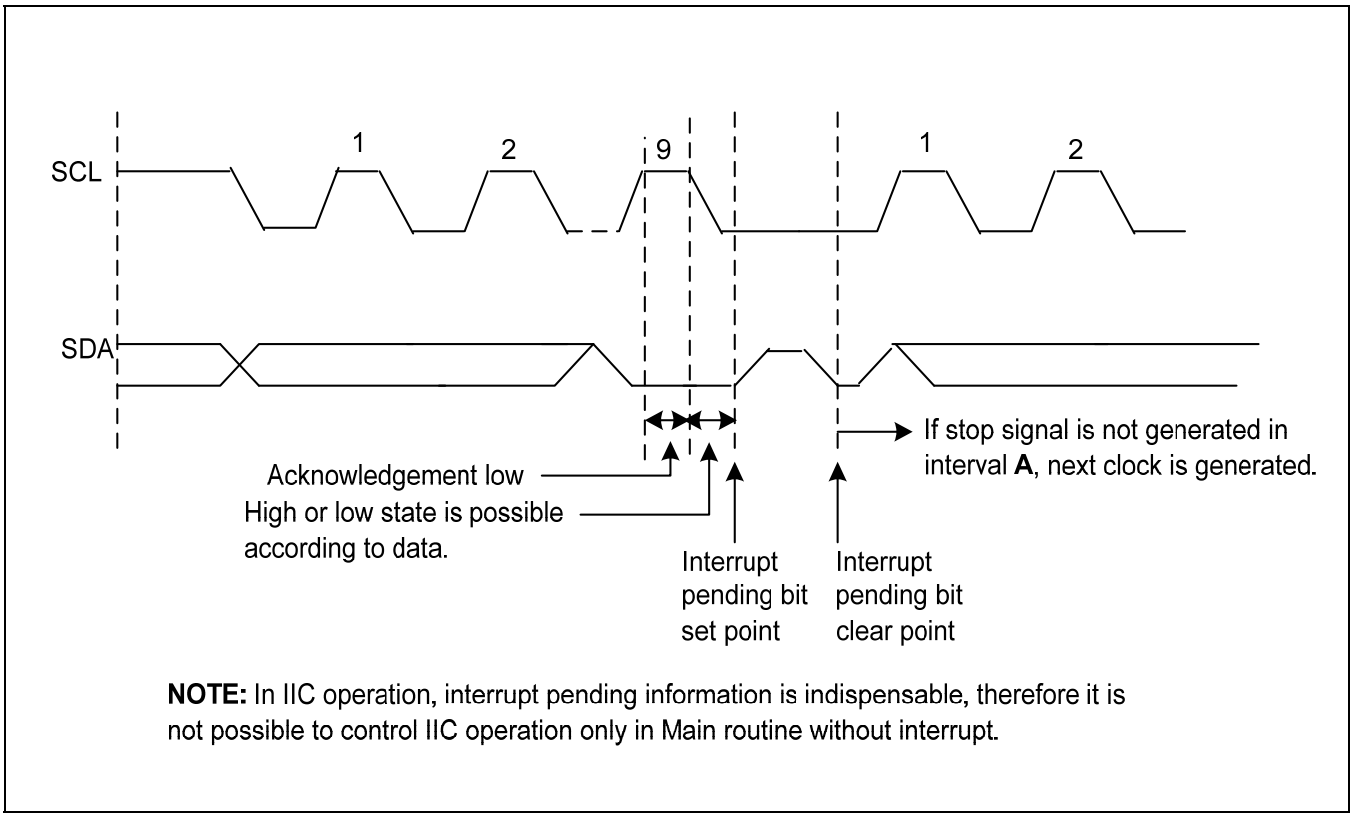

Figure 18-8 Interrupt Pending Information

19.2.3 UART 0 Interrupt Pending Bits

In mode 0, the receive interrupt pending bit UART0CONH.0 is set to "1" when the 8th receive data bit has been shifted. In mode 1, the UART0CONH.0 bit is set to "1" at the halfway point of the shift time of stop bit. In mode 2, or 3, the UART0CONH.0 bit is set to "1" at the halfway point of the shift time of RB8 bit. When the CPU acknowledges the receive interrupt pending condition, the UART0CONH.0 bit must then be cleared by software in the interrupt service routine.

In mode 0, the transmit interrupt pending bit UART0CONL.0 is set to "1" when the 8th transmit data bit has been shifted. In mode 1, 2, or 3, the UART0CONL.0 bit is set at the start of the stop bit. When the CPU acknowledges the transmit interrupt pending condition, the UART0CONL.0 bit must then be cleared by software in the interrupt service routine.

19.2.4 UART 0 Data Register

Figure 19-3 illustrates the UART 0 data register.

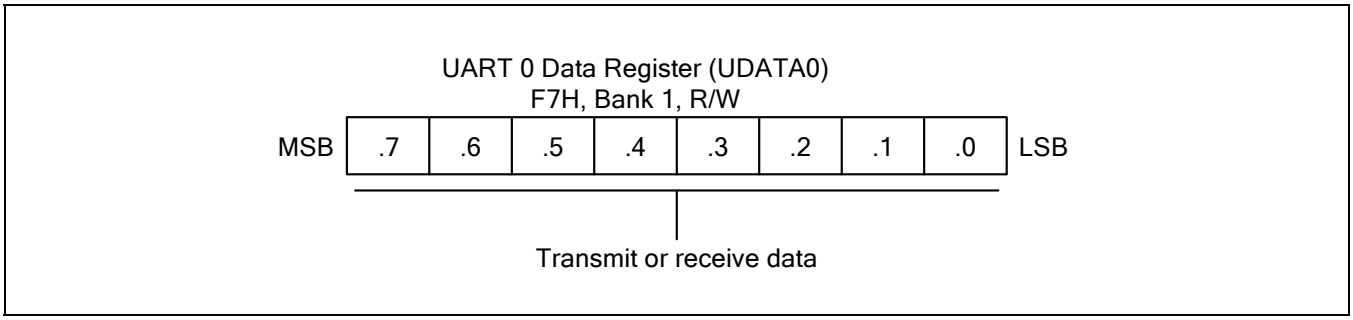

Figure 19-3 UART 0 Data Register (UDATA0)

19.2.5 UART 0 Baud Rate Data Register

The value stored in the UART 0 baud rate register (BRDATA0), enables you to determine the UART 0 clock rate (baud rate).

Figure 19-4 illustrates the UART 0 baud rate data register.

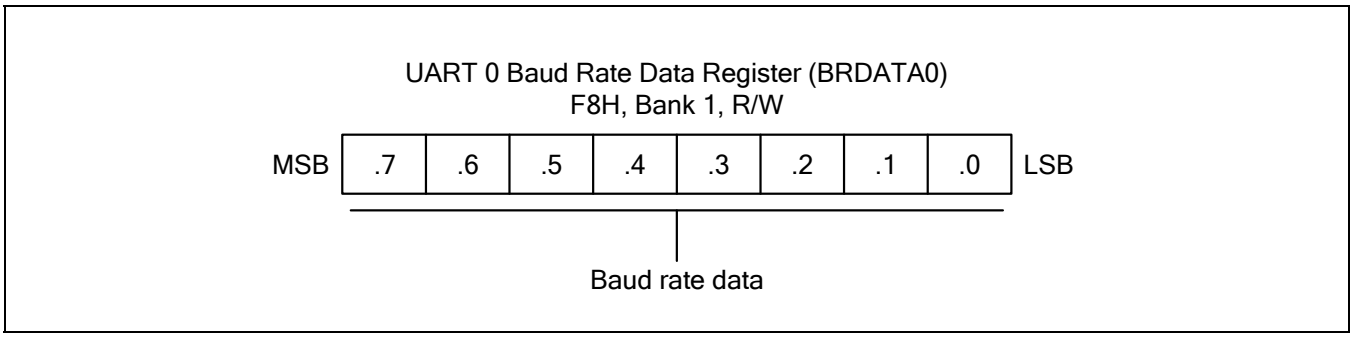

Figure 19-4 UART 0 Baud Rate Data Register (BRDATA0)

Figure 19-9 illustrates the timing diagram for serial port Mode 3 operation.

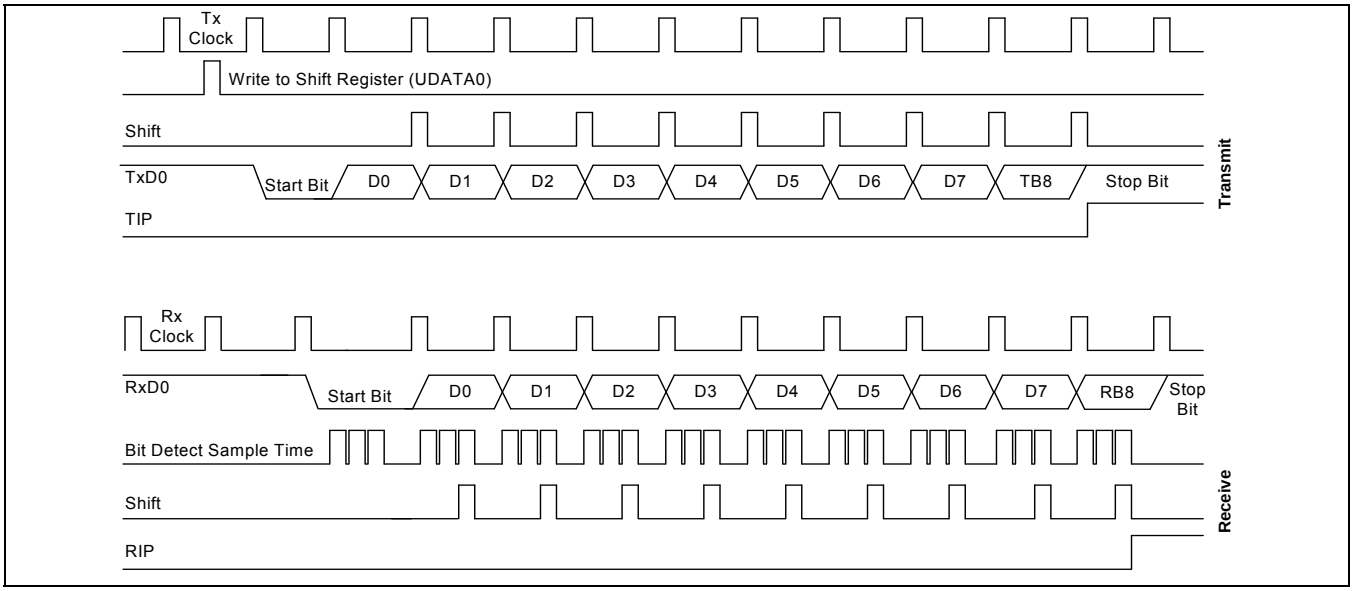

Figure 19-9 Timing Diagram for Serial Port Mode 3 Operation

20.8 Serial Port Mode 3 Function Description

In mode 3, 11 bits are transmitted (through the TxD1 (P2.4) pin) or received (through the RxD1 (P2.5) pin). Mode 3 is identical to mode 2 except for baud rate, which is variable.

The four components of each data frame are:

- Start bit ("0")
- 8 data bits (LSB first)
- Programmable 9th data bit
- Stop bit ("1")

20.8.1 Mode 3 Transmit Procedure

The steps for Mode 3 transmit procedure are:

1. Select the UART 1 clock, UART1CONL.3 and .2.
2. Set the UART 1 transmit parity bit autogeneration enable or disable bit (UART1CONL.7).
3. Select mode 3 operation (9-bit UART) by setting UART1CONH bits 7 and 6 to "11B". Also, select the 9th data bit to be transmitted by writing UART1CONH.3 (TB8) to "0" or "1".
4. Write transmission data to the shift register, UDATA1 (FBH, Set 1, Bank 1), to start the transmit operation.

20.8.2 Mode 3 Receive Procedure

The steps for Mode 3 receive procedure are:

1. Select the UART 1 clock, UART1CONL.3 and .2.
2. Set the UART 1 transmit parity bit autogeneration enable or disable bit (UART1CONL.7).
3. Select mode 3 and set the Receive Enable (RE) bit in the UART1CONH register to "1".
4. The receive operation will be started when the signal at the RxD1 (P2.5) pin enters to low level.

21.5 Sector Erase

You can erase a flash memory partially by using sector erase function only in User Program Mode. The only unit of flash memory that you can erase or program in User Program Mode is called sector.

The program memory of S3F8S39/S3F8S35 is divided into 256/128 sectors for unit of erase and programming, respectively. Every sector has all 128 byte sizes of program memory areas. Therefore, you should erase each sector first to program a new data (byte) into a sector. It requires minimum 10ms delay time for erase after setting sector address and triggering erase start bit (FMCON.0). Tool Program Modes (MDS mode tool or Programming tool) does not supports sector erase.

Figure 21-6 illustrates the sector configurations in user program mode.

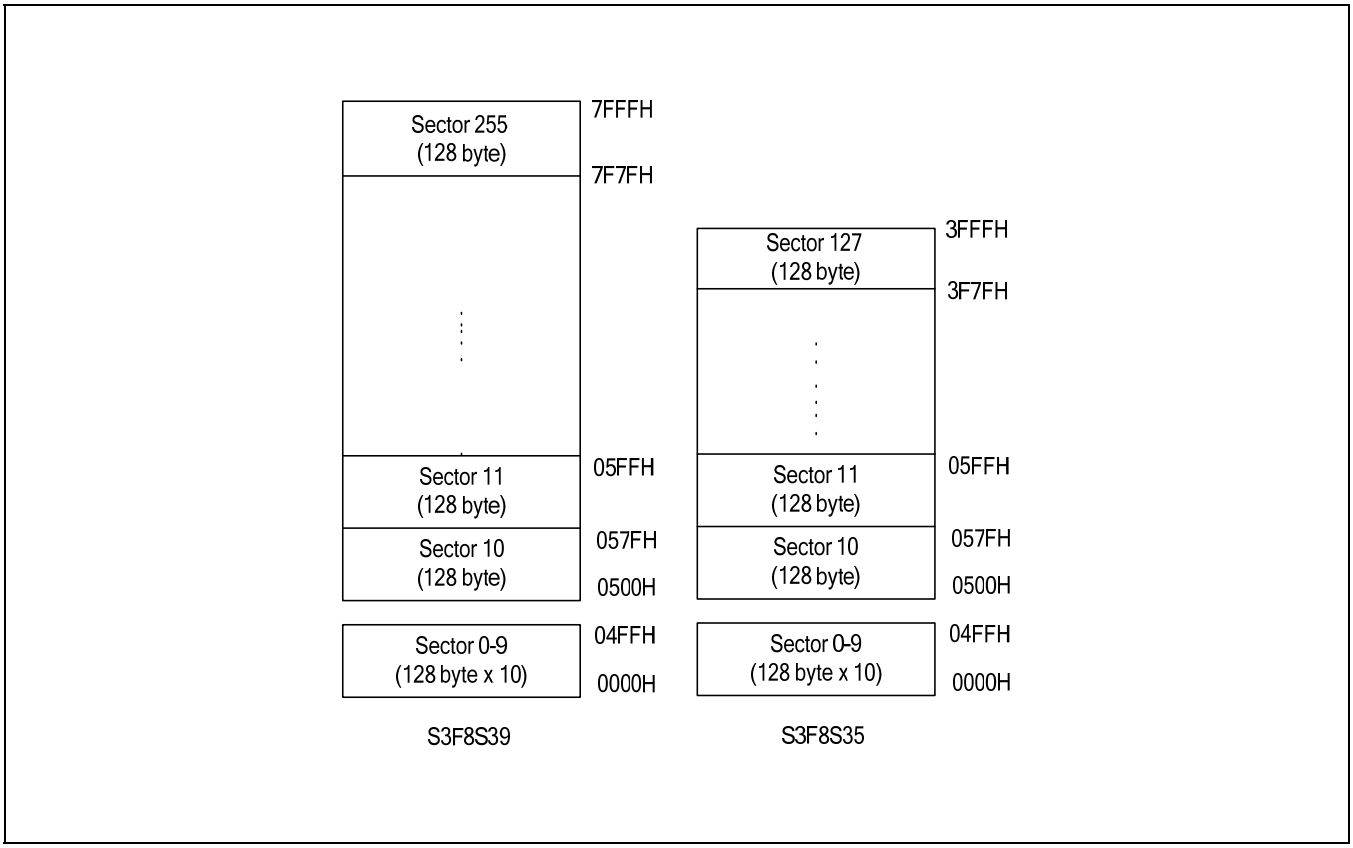

Figure 21-6 Sector Configurations in User Program Mode

Figure 26-4 illustrates the 24-Pin connector for TB8S19/8S28/8S39.

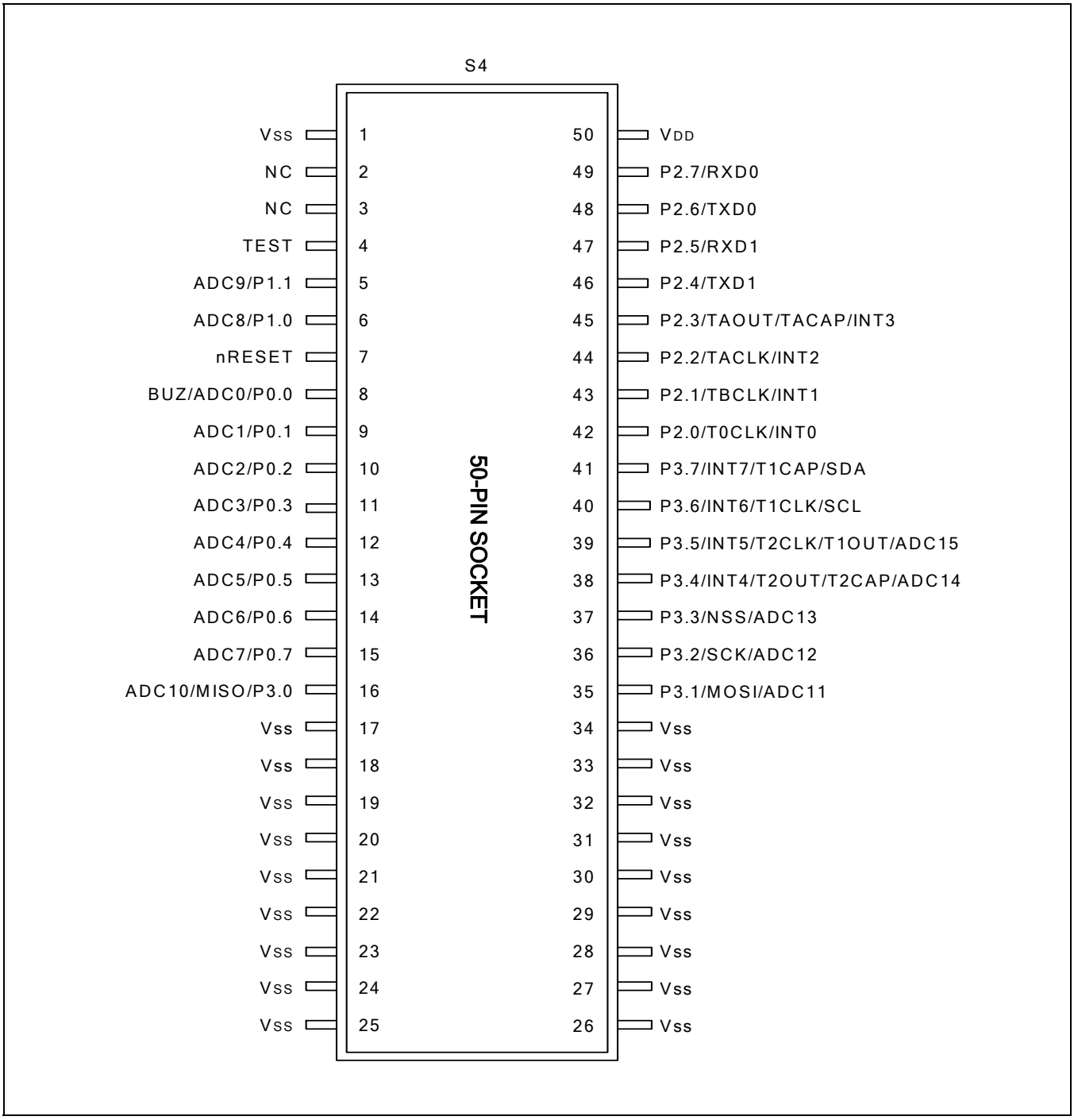

Figure 26-4 50-Pin Connector for TB8S19/8S28/8S39