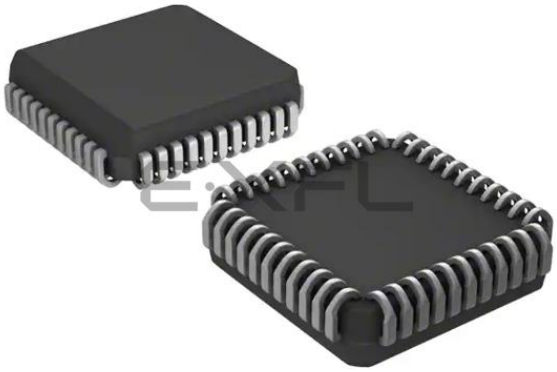


Welcome to E-XFL.COM

Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details	
Product Status	Obsolete
Programmable Type	In System Programmable (min 10K program/erase cycles)
Delay Time tpd(1) Max	10 ns
Voltage Supply - Internal	4.75V ~ 5.25V
Number of Logic Elements/Blocks	4
Number of Macrocells	72
Number of Gates	1600
Number of I/O	34
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	44-PLCC (16.59x16.59)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc9572-10pcg44c

XC9572 In-System Programmable CPLD

DS065 (v4.3) April 3, 2006

Product Specification

Features

- 7.5 ns pin-to-pin logic delays on all pins
- f_{CNT} to 125 MHz
- 72 macrocells with 1,600 usable gates
- Up to 72 user I/O pins
- 5V in-system programmable
  - Endurance of 10,000 program/erase cycles
  - Program/erase over full commercial voltage and temperature range
- Enhanced pin-locking architecture
- Flexible 36V18 Function Block
  - 90 product terms drive any or all of 18 macrocells within Function Block
  - Global and product term clocks, output enables, set and reset signals
- Extensive IEEE Std 1149.1 boundary-scan (JTAG) support
- Programmable power reduction mode in each macrocell
- Slew rate control on individual outputs
- User programmable ground pin capability
- Extended pattern security features for design protection
- High-drive 24 mA outputs
- 3.3V or 5V I/O capability
- Advanced CMOS 5V FastFLASH™ technology
- Supports parallel programming of more than one XC9500 concurrently
- Available in 44-pin PLCC, 84-pin PLCC, 100-pin PQFP, and 100-pin TQFP packages

Description

The XC9572 is a high-performance CPLD providing advanced in-system programming and test capabilities for general purpose logic integration. It is comprised of eight 36V18 Function Blocks, providing 1,600 usable gates with propagation delays of 7.5 ns. See Figure 2 for the architecture overview.

Power Management

Power dissipation can be reduced in the XC9572 by configuring macrocells to standard or low-power modes of operation. Unused macrocells are turned off to minimize power dissipation.

Operating current for each design can be approximated for specific operating conditions using the following equation:

I_{CC} (mA) = MC_{HP} (1.7) + MC_{LP} (0.9) + MC (0.006 mA/MHz) f

Where:

MC_{HP} = Macrocells in high-performance mode

MC_{LP} = Macrocells in low-power mode

MC = Total number of macrocells used

f = Clock frequency (MHz)

Figure 1 shows a typical calculation for the XC9572 device.

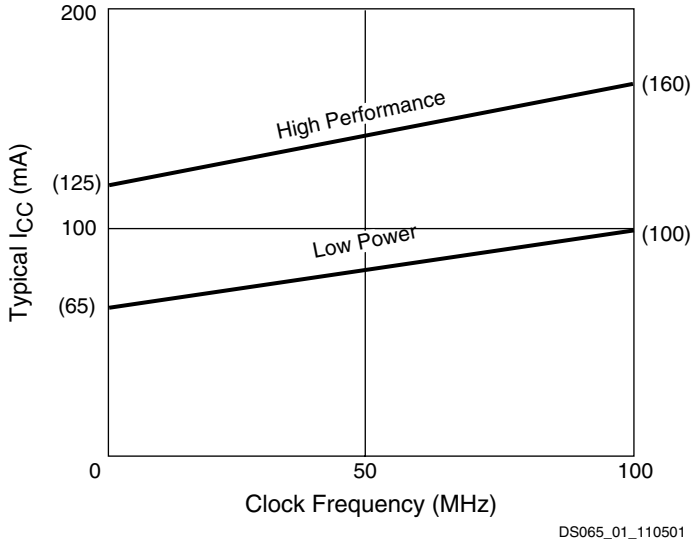


Figure 1: **Typical I_{CC} vs. Frequency for XC9572**

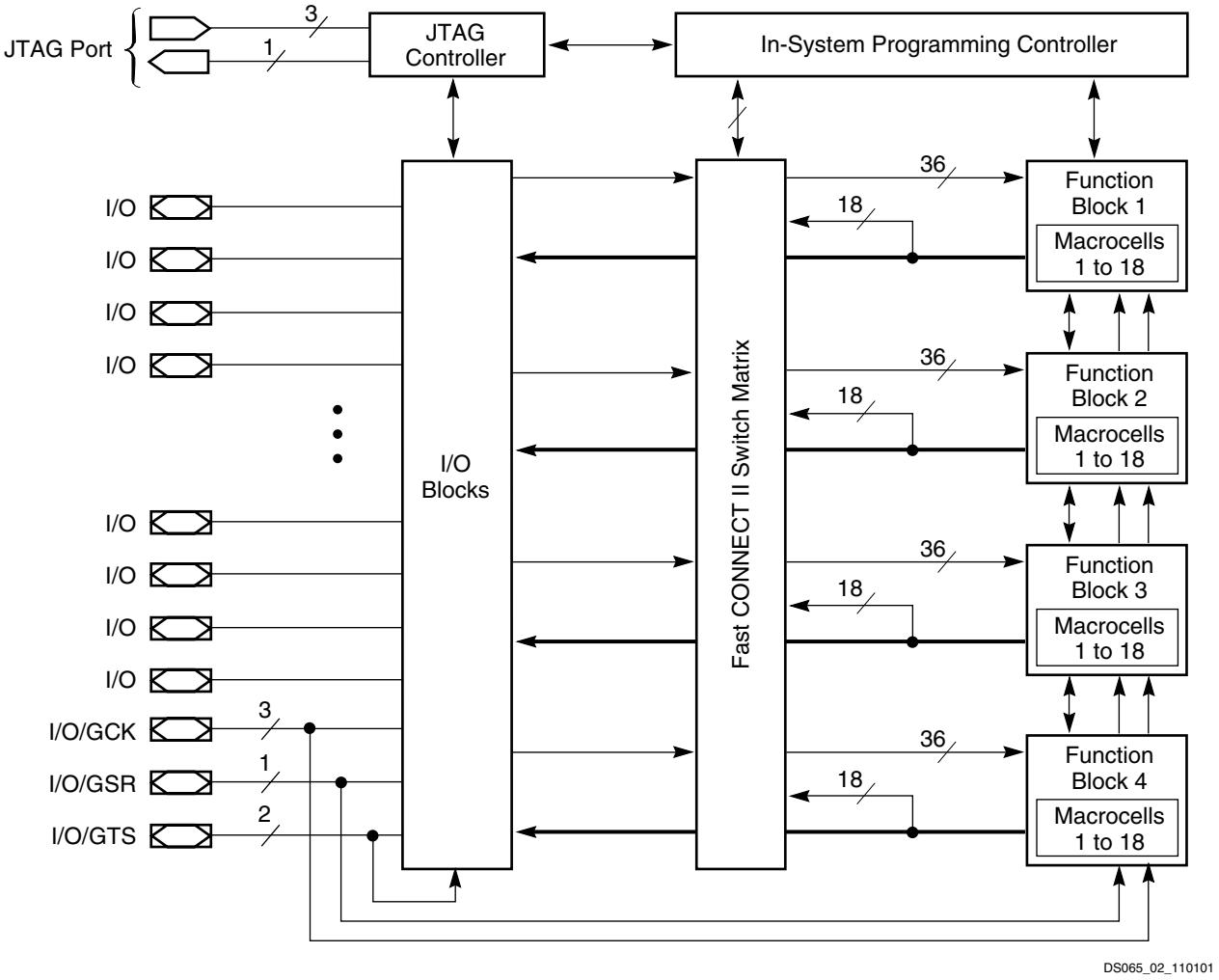


Figure 2: **XC9572 Architecture**
Function block outputs (indicated by the bold line) drive the I/O blocks directly.

Absolute Maximum Ratings

Symbol	Description	Value	Units
V_{CC}	Supply voltage relative to GND	–0.5 to 7.0	V
V_{IN}	Input voltage relative to GND	–0.5 to V_{CC} + 0.5	V
V_{TS}	Voltage applied to 3-state output	–0.5 to V_{CC} + 0.5	V
T_{STG}	Storage temperature (ambient)	–65 to +150	°C
T_J	Junction temperature	+150	°C

Notes:

1. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

Recommended Operation Conditions

Symbol	Parameter		Min	Max	Units
V_{CCINT}	Supply voltage for internal logic and input buffers	Commercial T_A = 0°C to 70°C	4.75	5.25	V
		Industrial T_A = –40°C to +85°C	4.5	5.5	
V_{CCIO}	Supply voltage for output drivers for 5V operation	Commercial T_A = 0°C to 70°C	4.75	5.25	V
		Industrial T_A = –40°C to +85°C	4.5	5.5	
	Supply voltage for output drivers for 3.3V operation		3.0	3.6	
V_{IL}	Low-level input voltage		0	0.80	V
V_{IH}	High-level input voltage		2.0	V_{CCINT} + 0.5	V
V_O	Output voltage		0	V_{CCIO}	V

Quality and Reliability Characteristics

Symbol	Parameter	Min	Max	Units
T_{DR}	Data Retention	20	-	Years
N_{PE}	Program/Erase Cycles (Endurance)	10,000	-	Cycles

DC Characteristic Over Recommended Operating Conditions

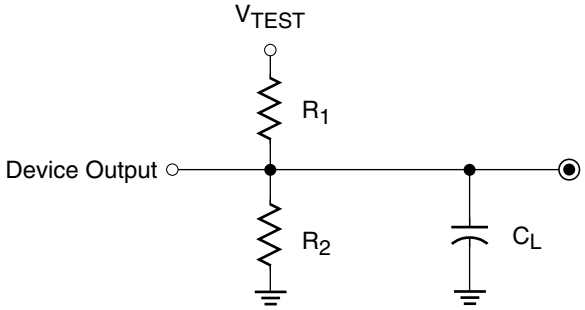
Symbol	Parameter	Test Conditions	Min	Max	Units
V_{OH}	Output high voltage for 5V outputs	I_{OH} = –4.0 mA, V_{CC} = Min	2.4	-	V
	Output high voltage for 3.3V outputs	I_{OH} = –3.2 mA, V_{CC} = Min	2.4	-	V
V_{OL}	Output low voltage for 5V outputs	I_{OL} = 24 mA, V_{CC} = Min	-	0.5	V
	Output low voltage for 3.3V outputs	I_{OL} = 10 mA, V_{CC} = Min	-	0.4	V
I_{IL}	Input leakage current	V_{CC} = Max V_{IN} = GND or V_{CC}	-	±10	µA
I_{IH}	I/O high-Z leakage current	V_{CC} = Max V_{IN} = GND or V_{CC}	-	±10	µA
C_{IN}	I/O capacitance	V_{IN} = GND f = 1.0 MHz	-	10	pF
I_{CC}	Operating supply current (low power mode, active)	V_I = GND, No load f = 1.0 MHz	65 (Typical)		mA

AC Characteristics

Symbol	Parameter	XC9572-7		XC9572-10		XC9572-15		Units
		Min	Max	Min	Max	Min	Max	
T_{PD}	I/O to output valid	-	7.5	-	10.0	-	15.0	ns
T_{SU}	I/O setup time before GCK	4.5	-	6.0	-	8.0	-	ns
T_{H}	I/O hold time after GCK	0	-	0	-	0	-	ns
T_{CO}	GCK to output valid	-	4.5	-	6.0	-	8.0	ns
f_{CNT}(1)	16-bit counter frequency	125.0	-	111.1	-	95.2	-	MHz
f_{SYSTEM}(2)	Multiple FB internal operating frequency	83.3	-	66.7	-	55.6	-	MHz
T_{PSU}	I/O setup time before p-term clock input	0.5	-	2.0	-	4.0	-	ns
T_{PH}	I/O hold time after p-term clock input	4.0	-	4.0	-	4.0	-	ns
T_{PCO}	P-term clock output valid	-	8.5	-	10.0	-	12.0	ns
T_{OE}	GTS to output valid	-	5.5	-	6.0	-	11.0	ns
T_{OD}	GTS to output disable	-	5.5	-	6.0	-	11.0	ns
T_{POE}	Product term OE to output enabled	-	9.5	-	10.0	-	14.0	ns
T_{POD}	Product term OE to output disabled	-	9.5	-	10.0	-	14.0	ns
T_{WLH}	GCK pulse width (High or Low)	4.0	-	4.5	-	5.5	-	ns
T_{APRPW}	Asynchronous preset/reset pulse width (High or Low)	7.0	-	7.5	-	8.0	-	ns

Notes:

1. f_{CNT} is the fastest 16-bit counter frequency available, using the local feedback when applicable. f_{CNT} is also the Export Control Maximum flip-flop toggle rate, f_{TOG}.
2. f_{SYSTEM} is the internal operating frequency for general purpose system designs spanning multiple FBs.



Output Type	V_{CCIO}	V_{TEST}	R_1	R_2	C_L
	5.0V	5.0V	160Ω	120Ω	35 pF
	3.3V	3.3V	260Ω	360Ω	35 pF

DS067_03_110101

Figure 3: **AC Load Circuit**

Internal Timing Parameters

Symbol	Parameter	XC9572-7		XC9572-10		XC9572-15		Units
		Min	Max	Min	Max	Min	Max	
Buffer Delays								
T_{IN}	Input buffer delay	-	2.5	-	3.5	-	4.5	ns
T_{GCK}	GCK buffer delay	-	1.5	-	2.5	-	3.0	ns
T_{GSR}	GSR buffer delay	-	4.5	-	6.0	-	7.5	ns
T_{GTS}	GTS buffer delay	-	5.5	-	6.0	-	11.0	ns
T_{OUT}	Output buffer delay	-	2.5	-	3.0	-	4.5	ns
T_{EN}	Output buffer enable/disable delay	-	0	-	0	-	0	ns
Product Term Control Delays								
T_{PTCK}	Product term clock delay	-	3.0	-	3.0	-	2.5	ns
T_{PTSR}	Product term set/reset delay	-	2.0	-	2.5	-	3.0	ns
T_{PTTS}	Product term 3-state delay	-	4.5	-	3.5	-	5.0	ns
Internal Register and Combinatorial Delays								
T_{PDI}	Combinatorial logic propagation delay	-	0.5	-	1.0	-	3.0	ns
T_{SUI}	Register setup time	1.5	-	2.5	-	3.5	-	ns
T_{HI}	Register hold time	3.0	-	3.5	-	4.5	-	ns
T_{COI}	Register clock to output valid time	-	0.5	-	0.5	-	0.5	ns
T_{AOI}	Register async. S/R to output delay	-	6.5	-	7.0	-	8.0	ns
T_{RAI}	Register async. S/R recover before clock	7.5	-	10.0	-	10.0	-	ns
T_{LOGI}	Internal logic delay	-	2.0	-	2.5	-	3.0	ns
T_{LOGILP}	Internal low power logic delay	-	10.0	-	11.0	-	11.5	ns
Feedback Delays								
T_F	FastCONNECT feedback delay	-	8.0	-	9.5	-	11.0	ns
T_{LF}	Function block local feedback delay	-	4.0	-	3.5	-	3.5	ns
Time Adders								
T_{PTA}(1)	Incremental product term allocator delay	-	1.0	-	1.0	-	1.0	ns
T_{SLEW}	Slew-rate limited delay	-	4.0	-	4.5	-	5.0	ns

Notes:
1. T_{PTA} is multiplied by the span of the function as defined in the XC9500 family data sheet.

XC9572 I/O Pins

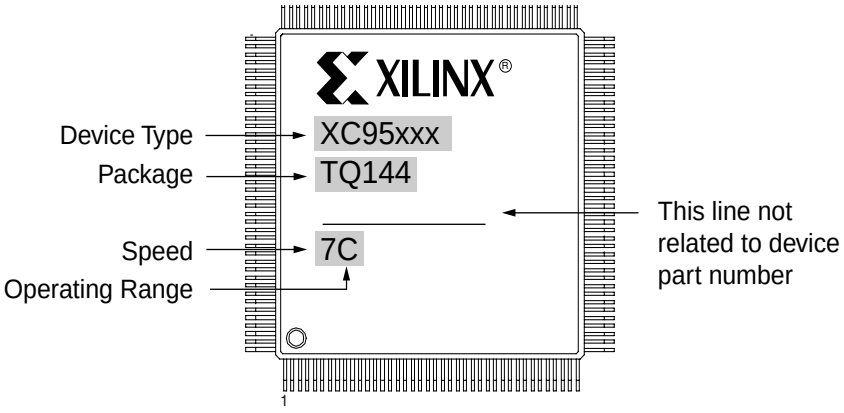
Function Block	Macro-cell	PC44	PC84	PQ100	TQ100	BScan Order
1	1	–	4	18	16	213
1	2	1	1	15	13	210
1	3	–	6	20	18	207
1	4	–	7	22	20	204
1	5	2	2	16	14	201
1	6	3	3	17	15	198
1	7	–	11	27	25	195
1	8	4	5	19	17	192
1	9	5[1]	9[1]	24[1]	22[1]	189
1	10	–	13	30	28	186
1	11	6[1]	10[1]	25[1]	23[1]	183
1	12	–	18	35	33	180
1	13	–	20	38	36	177
1	14	7[1]	12[1]	29[1]	27[1]	174
1	15	8	14	31	29	171
1	16	–	23	41	39	168
1	17	9	15	32	30	165
1	18	–	24	42	40	162
2	1	–	63	89	87	159
2	2	35	69	96	94	156
2	3	–	67	93	91	153
2	4	–	68	95	93	150
2	5	36	70	97	95	147
2	6	37	71	98	96	144
2	7	–	76[2]	5[2]	3[2]	141
2	8	38	72	99	97	138
2	9	39[1]	74[1]	1[1]	99[1]	135
2	10	–	75	3	1	132
2	11	40[1]	77[1]	6[1]	4[1]	129
2	12	–	79	8	6	126
2	13	–	80	10	8	123
2	14	42[3]	81[3]	11[3]	9[3]	120
2	15	43	83	13	11	117
2	16	–	82	12	10	114
2	17	44	84	14	12	111
2	18	–	–	94	92	108
3	1	–	25	43	41	105
3	2	11	17	34	32	102
3	3	–	31	51	49	99
3	4	–	32	52	50	96
3	5	12	19	37	35	93
3	6	–	34	55	53	90
3	7	–	35	56	54	87
3	8	13	21	39	37	84
3	9	14	26	44	42	81
3	10	–	40	62	60	78
3	11	18	33	54	52	75
3	12	–	41	63	61	72
3	13	–	43	65	63	69
3	14	19	36	57	55	66
3	15	20	37	58	56	63
3	16	–	45	67	65	60
3	17	22	39	60	58	57
3	18	–	–	61	59	54
4	1	–	46	68	66	51
4	2	24	44	66	64	48
4	3	–	51	73	71	45
4	4	–	52	74	72	42
4	5	25	47	69	67	39
4	6	–	54	78	76	36
4	7	–	55	79	77	33
4	8	26	48	70	68	30
4	9	27	50	72	70	27
4	10	–	57	83	81	24
4	11	28	53	76	74	21
4	12	–	58	84	82	18
4	13	–	61	87	85	15
4	14	29	56	80	78	12
4	15	33	65	91	89	9
4	16	–	62	88	86	6
4	17	34	66	92	90	3
4	18	–	–	81	79	0

Notes:
1. Global control piN.
2. Global control pin GTS1 for PC84, PQ100, and TQ100.
3. Global control pin GTS1 for PC44.

XC9572 Global, JTAG and Power Pins

Pin Type	PC44	PC84	PQ100	TQ100
I/O/GCK1	5	9	24	22
I/O/GCK2	6	10	25	23
I/O/GCK3	7	12	29	27
I/O/GTS1	42	76	5	3
I/O/GTS2	40	77	6	4
I/O/GSR	39	74	1	99
TCK	17	30	50	48
TDI	15	28	47	45
TDO	30	59	85	83
TMS	16	29	49	47
V_{CCINT} 5V	21,41	38,73,78	7,59,100	5,57,98
V_{CCIO} 3.3V/5V	32	22,64	28,40,53,90	26,38,51,88
GND	10,23,31	8,16,27,42, 49,60	2,23,33,46,64,71, 77,86	100,21,31,44,62,69, 75, 84
No Connects	-	-	4,9,21,26,36,45,48, 75, 82	2,7,19,24,34,43,46, 73, 80

Device Part Marking and Ordering Combination Information



Sample package with part marking.

Device Ordering and Part Marking Number	Speed (pin-to-pin delay)	Pkg. Symbol	No. of Pins	Package Type	Operating Range[1]
XC9572-7PC44C	7.5 ns	PC44	44-pin	Plastic Lead Chip Carrier (PLCC)	C
XC9572-7PCG44C	7.5 ns	PCG44	44-pin	Plastic Lead Chip Carrier (PLCC); Pb-Free	C
XC9572-7PC84C	7.5 ns	PC84	84-pin	Plastic Lead Chip Carrier (PLCC)	C
XC9572-7PCG84C	7.5 ns	PCG84	84-pin	Plastic Lead Chip Carrier (PLCC); Pb-Free	C
XC9572-7PQ100C	7.5 ns	PQ100	100-pin	Plastic Quad Flat Pack (PQFP)	C
XC9572-7PQG100C	7.5 ns	PQG100	100-pin	Plastic Quad Flat Pack (PQFP); Pb-Free	C
XC9572-7TQ100C	7.5 ns	TQ100	100-pin	Thin Quad Flat Pack (TQFP)	C
XC9572-7TQG100C	7.5 ns	TQG100	100-pin	Thin Quad Flat Pack (TQFP); Pb-Free	C
XC9572-10PC44C	10 ns	PC44	44-pin	Plastic Lead Chip Carrier (PLCC)	C
XC9572-10PCG44C	10 ns	PCG44	44-pin	Plastic Lead Chip Carrier (PLCC); Pb-Free	C
XC9572-10PC84C	10 ns	PC84	84-pin	Plastic Lead Chip Carrier (PLCC)	C
XC9572-10PCG84C	10 ns	PCG84	84-pin	Plastic Lead Chip Carrier (PLCC); Pb-Free	C
XC9572-10PQ100C	10 ns	PQ100	100-pin	Plastic Quad Flat Pack (PQFP)	C
XC9572-10PQG100C	10 ns	PQG100	100-pin	Plastic Quad Flat Pack (PQFP); Pb-Free	C
XC9572-10TQ100C	10 ns	TQ100	100-pin	Thin Quad Flat Pack (TQFP)	C
XC9572-10TQG100C	10 ns	TQG100	100-pin	Thin Quad Flat Pack (TQFP); Pb-Free	C
XC9572-10PC44I	10 ns	PC44	44-pin	Plastic Lead Chip Carrier (PLCC)	I
XC9572-10PCG44I	10 ns	PCG44	44-pin	Plastic Lead Chip Carrier (PLCC); Pb-Free	I
XC9572-10PC84I	10 ns	PC84	84-pin	Plastic Lead Chip Carrier (PLCC)	I
XC9572-10PCG84I	10 ns	PCG84	84-pin	Plastic Lead Chip Carrier (PLCC); Pb-Free	I
XC9572-10PQ100I	10 ns	PQ100	100-pin	Plastic Quad Flat Pack (PQFP)	I
XC9572-10PQG100I	10 ns	PQG100	100-pin	Plastic Quad Flat Pack (PQFP); Pb-Free	I
XC9572-10TQ100I	10 ns	TQ100	100-pin	Thin Quad Flat Pack (TQFP)	I
XC9572-10TQG100I	10 ns	TQG100	100-pin	Thin Quad Flat Pack (TQFP); Pb-Free	I
XC9572-15PC44C	15 ns	PC44	44-pin	Plastic Lead Chip Carrier (PLCC)	C
XC9572-15PCG44C	15 ns	PCG44	44-pin	Plastic Lead Chip Carrier (PLCC); Pb-Free	C
XC9572-15PC84C	15 ns	PC84	84-pin	Plastic Lead Chip Carrier (PLCC)	C
XC9572-15PCG84C	15 ns	PCG84	84-pin	Plastic Lead Chip Carrier (PLCC); Pb-Free	C
XC9572-15PQ100C	15 ns	PQ100	100-pin	Plastic Quad Flat Pack (PQFP)	C
XC9572-15PQG100C	15 ns	PQG100	100-pin	Plastic Quad Flat Pack (PQFP); Pb-Free	C
XC9572-15TQ100C	15 ns	TQ100	100-pin	Thin Quad Flat Pack (TQFP)	C
XC9572-15TQG100C	15 ns	TQG100	100-pin	Thin Quad Flat Pack (TQFP); Pb-Free	C
XC9572-15PC44I	15 ns	PC44	44-pin	Plastic Lead Chip Carrier (PLCC)	I

Device Ordering and Part Marking Number	Speed (pin-to-pin delay)	Pkg. Symbol	No. of Pins	Package Type	Operating Range(1)
XC9572-15PCG44I	15 ns	PCG44	44-pin	Plastic Lead Chip Carrier (PLCC); Pb-Free	I
XC9572-15PC84I	15 ns	PC84	84-pin	Plastic Lead Chip Carrier (PLCC)	I
XC9572-15PCG84I	15 ns	PCG84	84-pin	Plastic Lead Chip Carrier (PLCC); Pb-Free	I
XC9572-15PQ100I	15 ns	PQ100	100-pin	Plastic Quad Flat Pack (PQFP)	I
XC9572-15PQG100I	15 ns	PQG100	100-pin	Plastic Quad Flat Pack (PQFP); Pb-Free	I
XC9572-15TQ100I	15 ns	TQ100	100-pin	Thin Quad Flat Pack (TQFP)	I
XC9572-15TQG100I	15 ns	TQG100	100-pin	Thin Quad Flat Pack (TQFP); Pb-Free	I

Notes:
1. C = Commercial: T_A = 0° to +70°C; I = Industrial: T_A = –40° to +85°C

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Revision History

The following table shows the revision history for this document.

Date	Version	Revision
12/04/98	3.0	Update AC characteristics and internal parameters.
06/18/03	4.0	Updated format.
08/21/03	4.1	Updated Package Device Marking Pin 1 orientation.
04/15/05	4.2	Added asynchronous preset/reset pulse width specification (T_{APRPW})
04/03/06	4.3	Added Warranty Disclaimer. Added Pb-Free package information.