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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM1136JF-S
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	400MHz
Co-Processors/DSP	Multimedia; GPU, IPU, MPEG-4, VFP
RAM Controllers	DDR
Graphics Acceleration	Yes
Display & Interface Controllers	Keyboard, Keypad, LCD
Ethernet	-
SATA	-
USB	USB 2.0 (3)
Voltage - I/O	1.8V, 2.0V, 2.5V, 2.7V, 3.0V
Operating Temperature	-40°C ~ 85°C (TA)
Security Features	Random Number Generator, RTIC, Secure Fusebox, Secure JTAG, Secure Memory
Package / Case	473-LFBGA
Supplier Device Package	473-MAPBGA (19x19)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mcimx31cjmn4c

MCIMX31C provides the optimal performance versus leakage current balance.

The performance of the MCIMX31C is boosted by a multi-level cache system, and features peripheral devices such as an MPEG-4 Hardware Encoder (VGA, 30 fps), an Autonomous Image Processing Unit, a Vector Floating Point (VFP11) co-processor, and a RISC-based SDMA controller.

The MCIMX31C supports connections to various types of external memories, such as DDR, NAND Flash, NOR Flash, SDRAM, and SRAM. The MCIMX31C can be connected to a variety of external devices using technology, such as high-speed USB2.0 OTG, ATA, MMC/SDIO, and compact flash.

1.1 Features

The MCIMX31C is designed for automotive and industrial markets where extended operating temperature is required. They provide low-power solutions for high-performance demanding multimedia and graphics applications.

The MCIMX31C is built around the ARM11 MCU core and implemented in the 90 nm technology.

The systems include the following features:

- Multimedia and floating-point hardware acceleration supporting:
  - MPEG-4 real-time encode of up to VGA at 30 fps
  - MPEG-4 real-time video post-processing of up to VGA at 30 fps
  - Video conference call of up to QCIF-30 fps (decoder in software), 128 kbps
  - Video streaming (playback) of up to VGA-30 fps, 384 kbps
  - 3D graphics and other applications acceleration with the ARM® tightly-coupled Vector Floating Point co-processor
  - On-the-fly video processing that reduces system memory load (for example, the power-efficient viewfinder application with no involvement of either the memory system or the ARM CPU)
- Advanced power management
  - Dynamic voltage and frequency scaling
  - Multiple clock and power domains
  - Independent gating of power domains
- Multiple communication and expansion ports including a fast parallel interface to an external graphic accelerator (supporting major graphic accelerator vendors)
- Security

1.2 Ordering Information

Table 1 provides the ordering information for the MCIMX31C.

Table 1. MCIMX31C and MCIMX31LC Ordering Information[1]

Part Number	Silicon Revision	Operating Temperature Range (°C)	Package[2]
MCIMX31CVMN4C!	2.0	–40 to 85	19 x 19 mm, 0.8 mm pitch, Case 1931
MCIMX31LCVMN4C!	2.0	–40 to 85	
MCIMX31CVMN4D!	2.0.1	–40 to 85	
MCIMX31LCVMN4D!	2.0.1	–40 to 85	
MCIMX31CJMN4C	2.0.1	–40 to 85	
MCIMX31LCJMN4D	2.0.1	–40 to 85	
MCIMX31CJMN4D	2.0.1	–40 to 85	

1 Because of an order from the United States International Trade Commission, BGA-packaged product lines and part numbers indicated here currently are not available from Freescale for import or sale in the United States prior to September 2010: Indicated by the Icon (!)

2 Case 1931 is RoHS compliant, lead-free, MSL = 3.

1.2.1 Feature Differences Between TO2.0 and TO 2.0.1

The following is a summary of the differences between silicon Revision 2.0 and Revision 2.0.1:

- Revision 2.0.1 - iROM updated to support boot from USB HS and SD/MMC.

- Instruction and data memory management units (MMUs), managed using micro TLB structures backed by a unified main TLB
- Instruction and data L1 caches, including a non-blocking data cache with Hit-Under-Miss
- Virtually indexed/physically addressed L1 caches
- 64-bit interface to both L1 caches
- Write buffer (bypassable)
- High-speed Advanced Micro Bus Architecture (AMBA)™ L2 interface
- Vector Floating Point co-processor (VFP) for 3D graphics and other floating-point applications hardware acceleration
- ETM™ and JTAG-based debug support

2.1.1 Memory System

The ARM1136JF-S complex includes 16 KB Instruction and 16 KB Data L1 caches. It connects to the MCIMX31C L2 unified cache through 64-bit instruction (read-only), 64-bit data read/write (bi-directional), and 64-bit data write interfaces.

The embedded 16K SRAM can be used for audio streaming data to avoid external memory accesses for the low-power audio playback, for security, or for other applications. There is also a 32-KB ROM for bootstrap code and other frequently-used code and data.

A ROM patch module provides the ability to patch the internal ROM. It can also initiate an external boot by overriding the boot reset sequence by a jump to a configurable address.

Table 2 shows information about the MCIMX31C core in tabular form.

Table 2. MCIMX31C Core

Core Acronym	Core Name	Brief Description	Integrated Memory Includes
ARM11 or ARM1136	ARM1136 Platform	The ARM1136™ Platform consists of the ARM1136JF-S core, the ETM real-time debug modules, a 6 x 5 multi-layer AHB crossbar switch (MAX), and a Vector Floating Processor (VFP). The MCIMX31C provides a high-performance ARM11 microprocessor core and highly integrated system functions. The ARM Application Processor (AP) and other subsystems address the needs of the personal, wireless, and portable product market with integrated peripherals, advanced processor core, and power management capabilities.	• 16 Kbyte Instruction Cache • 16 Kbyte Data Cache • 128 Kbyte L2 Cache • 32 Kbyte ROM • 16 Kbyte RAM

1 In read mode, FUSE_VDD should be floated or grounded.

2 Fuses might be inadvertently blown if written to while the voltage is below the minimum.

Table 9 provides information for interface frequency limits. For more details about clocks characteristics, see Section 4.3.8, “DPLL Electrical Specifications” on page 31 and Section 4.3.3, “Clock Amplifier Module (CAMP) Electrical Characteristics” on page 19.

Table 9. Interface Frequency

ID	Parameter	Symbol	Min	Typ	Max	Units
1	JTAG TCK Frequency	f_{JTAG}	DC	5	10	MHz
2	CKIL Frequency[1]	f_{CKIL}	32	32.768	38.4	kHz
3	CKIH Frequency[2]	f_{CKIH}	15	26	75	MHz

1 CKIL must be driven by an external clock source to ensure proper start-up and operation of the device. CKIL is needed to clock the internal reset synchronizer, the watchdog, and the real-time clock.

2 DPTC functionality, specifically the voltage/frequency relation table, is dependent on CKIH frequency. At the time of publication, standard tables used by Freescale OSs provided for a CKIH frequency of 26 MHz only. Any deviation from this frequency requires an update to the OS. For more details, refer to the particular OS user's guide documentation. DPTC/DVFS are not supported for fARM ≤ 400MHz.

Table 10 shows the fusebox supply current parameters.

Table 10. Fusebox Supply Current Parameters

Ref. Num	Description	Symbol	Minimum	Typical	Maximum	Units
1	eFuse Program Current.[1] Current to program one eFuse bit: efuse_pgm = 3.0V	$I_{program}$	—	35	60	mA

1 The current $I_{program}$ is during program time ($t_{program}$).

Table 14. AC Electrical Characteristics of Slow[1] General I/O

ID	Parameter	Symbol	Test Condition	Min	Typ	Max	Units
PA1	Output Transition Times (Max Drive)	tpr	25 pF 50 pF	0.92 1.5	1.95 2.98	3.17 4.75	ns
	Output Transition Times (High Drive)	tpr	25 pF 50 pF	1.52 2.75	—	4.81 8.42	ns
	Output Transition Times (Std Drive)	tpr	25 pF 50 pF	2.79 5.39	—	8.56 16.43	ns

1 Fast/slow characteristic is selected per GPIO (where available) by “slew rate” control. See reference manual.

Table 15. AC Electrical Characteristics of Fast[1] General I/O [2]

ID	Parameter	Symbol	Test Condition	Min	Typ	Max	Units
PA1	Output Transition Times (Max Drive)	tpr	25 pF 50 pF	0.68 1.34	1.33 2.6	2.07 4.06	ns
	Output Transition Times (High Drive)	tpr	25 pF 50 pF	.91 1.79	1.77 3.47	2.74 5.41	ns
	Output Transition Times (Std Drive)	tpr	25 pF 50 pF	1.36 2.68	2.64 5.19	4.12 8.11	ns

1 Fast/slow characteristic is selected per GPIO (where available) by “slew rate” control. See reference manual.

2 Use of GPIO in fast mode with the associated NVCC > 1.95 V can result in excessive overshoot and ringing.

Table 16. AC Electrical Characteristics of DDR I/O

ID	Parameter	Symbol	Test Condition	Min	Typ	Max	Units
PA1	Output Transition Times (DDR Drive)[1]	tpr	25 pF 50 pF	0.51 0.97	0.82 1.58	1.28 2.46	ns
	Output Transition Times (Max Drive)	tpr	25 pF 50 pF	0.67 1.29	1.08 2.1	1.69 3.27	ns
	Output Transition Times (High Drive)	tpr	25 pF 50 pF	.99 1.93	1.61 3.13	2.51 4.89	ns
	Output Transition Times (Std Drive)	tpr	25 pF 50 pF	1.96 3.82	3.19 6.24	4.99 9.73	ns

1 Use of DDR Drive can result in excessive overshoot and ringing.

4.3.3 Clock Amplifier Module (CAMP) Electrical Characteristics

This section outlines the Clock Amplifier Module (CAMP) specific electrical characteristics. Table 17 shows clock amplifier electrical characteristics.

Table 17. Clock Amplifier Electrical Characteristics for CKIH Input

Parameter	Min	Typ	Max	Units
Input Frequency	15	—	75	MHz
VIL (for square wave input)	0	—	0.3	V
VIH (for square wave input)	(VDD [1] – 0.25)	—	3	V
Sinusoidal Input Amplitude	0.4 [2]	—	VDD	Vp-p
Duty Cycle	45	50	55	%

1 VDD is the supply voltage of CAMP. See reference manual.

2 This value of the sinusoidal input will be measured through characterization.

4.3.4 1-Wire Electrical Specifications

Figure 6 depicts the RPP timing, and Table 18 lists the RPP timing parameters.

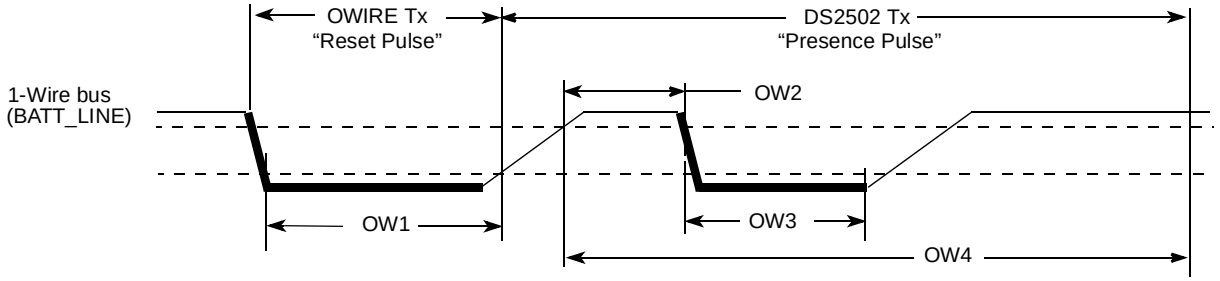


Figure 6. Reset and Presence Pulses (RPP) Timing Diagram

Table 18. RPP Sequence Delay Comparisons Timing Parameters

ID	Parameters	Symbol	Min	Typ	Max	Units
OW1	Reset Time Low	t_{RSTL}	480	511	—	µs
OW2	Presence Detect High	t_{PDH}	15	—	60	µs
OW3	Presence Detect Low	t_{PDL}	60	—	240	µs
OW4	Reset Time High	t_{RSTH}	480	512	—	µs

Figure 7 depicts Write 0 Sequence timing, and Table 19 lists the timing parameters.

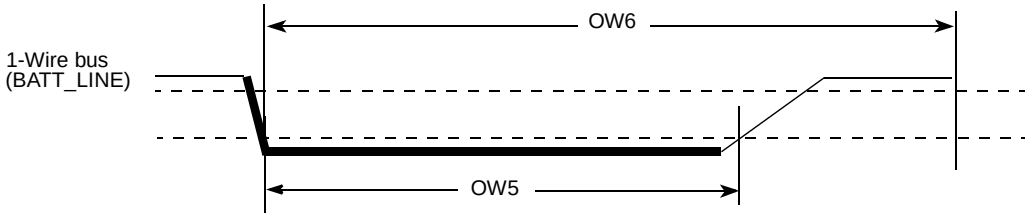


Figure 7. Write 0 Sequence Timing Diagram

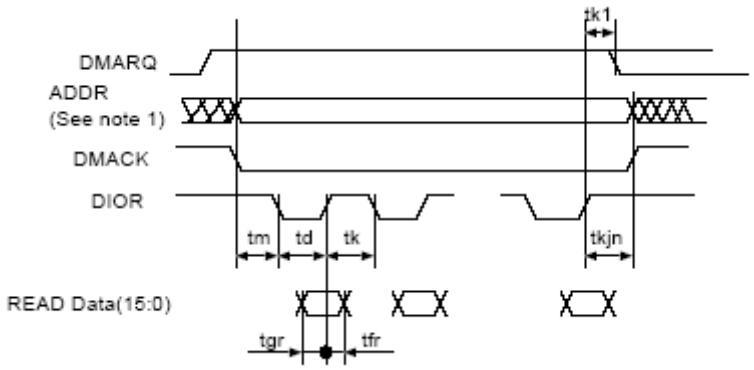


Figure 12. MDMA Read Timing Diagram

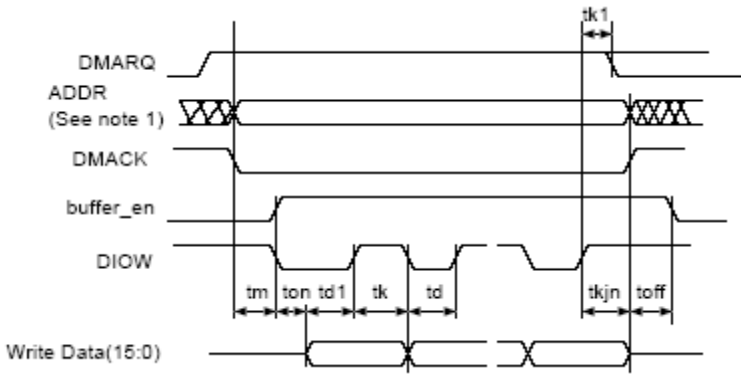


Figure 13. MDMA Write Timing Diagram

Table 24. MDMA Read and Write Timing Parameters

ATA Parameter	Parameter from Figure 12, Figure 13	Value	Controlling Variable
tm, ti	tm	tm (min) = ti (min) = time_m * T – (tskew1 + tskew2 + tskew5)	time_m
td	td, td1	td1.(min) = td (min) = time_d * T – (tskew1 + tskew2 + tskew6)	time_d
tk	tk	tk.(min) = time_k * T – (tskew1 + tskew2 + tskew6)	time_k
t0	—	t0 (min) = (time_d + time_k) * T	time_d, time_k
tg(read)	tgr	tgr (min-read) = tco + tsu + tbuf + tbuf + tcable1 + tcable2 tgr.(min-drive) = td – te(drive)	time_d
tf(read)	tfr	tfr (min-drive) = 0	—
tg(write)	—	tg (min-write) = time_d * T – (tskew1 + tskew2 + tskew5)	time_d
tf(write)	—	tf (min-write) = time_k * T – (tskew1 + tskew2 + tskew6)	time_k
tL	—	tL (max) = (time_d + time_k–2)*T – (tsu + tco + 2*tbuf + 2*tcable2)	time_d, time_k
tn, tj	tkjn	tn= tj= tkjn = (max(time_k,. time_jn) * T – (tskew1 + tskew2 + tskew6)	time_jn
—	ton toff	ton = time_on * T – tskew1 toff = time_off * T – tskew1	—

4.3.6 AUDMUX Electrical Specifications

The AUDMUX provides a programmable interconnect logic for voice, audio and data routing between internal serial interfaces (SSI) and external serial interfaces (audio and voice codecs). The AC timing of AUDMUX external pins is hence governed by the SSI module. Please refer to their respective electrical specifications.

4.3.7 CSPI Electrical Specifications

This section describes the electrical information of the CSPI.

4.3.7.1 CSPI Timing

Figure 20 and Figure 21 depict the master mode and slave mode timings of CSPI, and Table 27 lists the timing parameters.

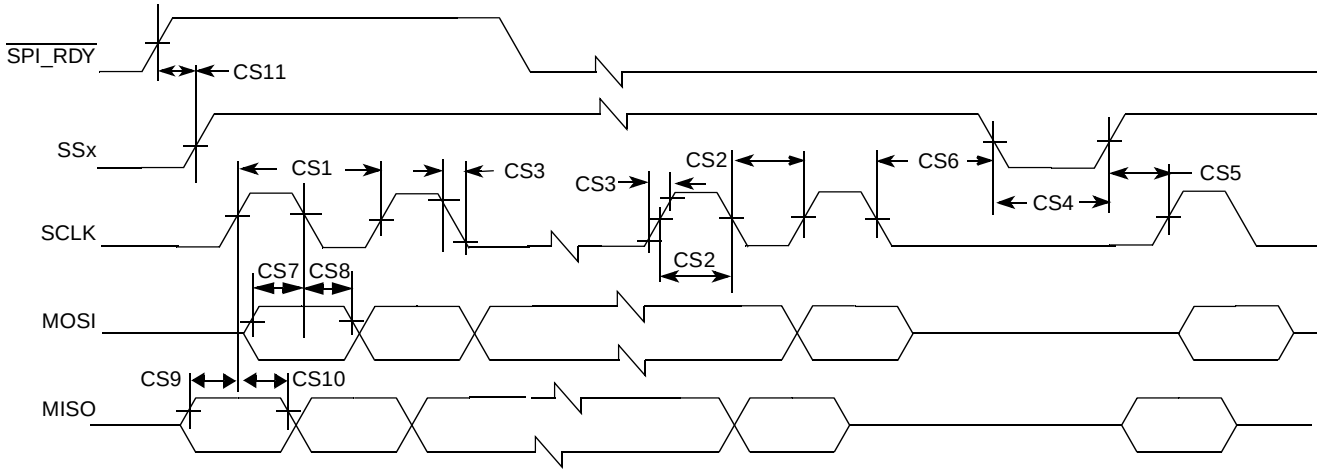


Figure 20. CSPI Master Mode Timing Diagram

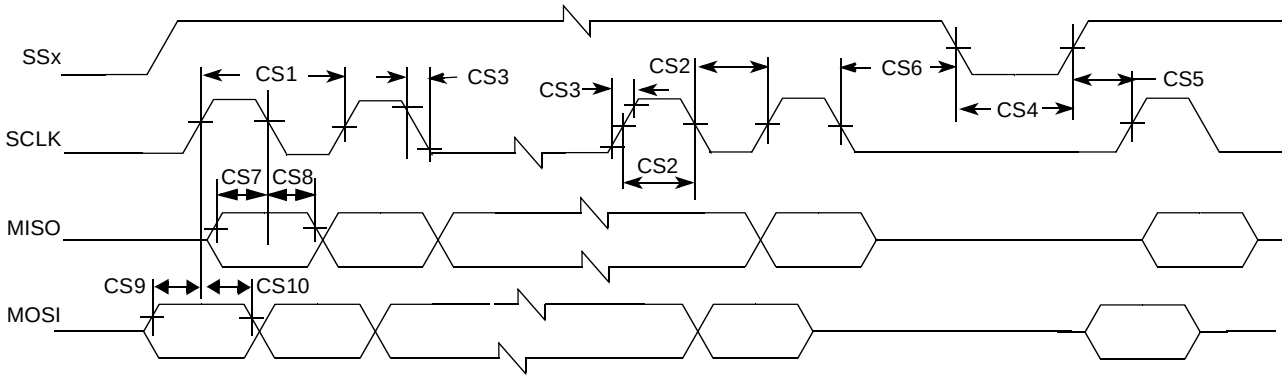


Figure 21. CSPI Slave Mode Timing Diagram

Table 27. CSPI Interface Timing Parameters

ID	Parameter	Symbol	Min	Max	Units
CS1	SCLK Cycle Time	t_{clk}	60	—	ns
CS2	SCLK High or Low Time	t_{SW}	30	—	ns
CS3	SCLK Rise or Fall	$t_{RISE/FALL}$	—	7.6	ns
CS4	SSx pulse width	t_{CSLH}	25	—	ns
CS5	SSx Lead Time (CS setup time)	t_{SCS}	25	—	ns
CS6	SSx Lag Time (CS hold time)	t_{HCS}	25	—	ns
CS7	Data Out Setup Time	t_{Smosi}	5	—	ns
CS8	Data Out Hold Time	t_{Hmosi}	5	—	ns
CS9	Data In Setup Time	t_{Smiso}	6	—	ns
CS10	Data In Hold Time	t_{Hmiso}	5	—	ns
CS11	$\overline{\text{SPI\_RDY}}$ Setup Time[1]	t_{SRDY}	—	—	ns

1 SPI_RDY is sampled internally by ipg_clk and is asynchronous to all other CSPI signals.

4.3.8 DPLL Electrical Specifications

The three PLL's of the MCIMX31C (MCU, USB, and Serial PLL) are all based on same DPLL design. The characteristics provided herein apply to all of them, except where noted explicitly. The PLL characteristics are provided based on measurements done for both sources—external clock source (CKIH), and FPM (Frequency Pre-Multiplier) source.

4.3.8.1 Electrical Specifications

Table 28 lists the DPLL specification.

Table 28. DPLL Specifications

Parameter	Min	Typ	Max	Unit	Comments
CKIH frequency	15	26[1]	75[2]	MHz	—
CKIL frequency (Frequency Pre-multiplier (FPM) enable mode)	—	32; 32.768, 38.4	—	kHz	FPM lock time ≈ 480 µs.
Predivision factor (PD bits)	1	—	16	—	—
PLL reference frequency range after Predivider	15	—	35	MHz	15 ≤ CKIH frequency/PD ≤ 35 MHz 15 ≤ FPM output/PD ≤ 35 MHz
PLL output frequency range: MPLL and SPLL UPLL	 52 190	—	 400 240	MHz	—
Maximum allowed reference clock phase noise.	—	—	± 100	ps	—
Frequency lock time (FOL mode or non-integer MF)	—	—	398	—	Cycles of divided reference clock.

Table 32. SDR SDRAM Write Timing Parameters (continued)

ID	Parameter	Symbol	Min	Max	Unit
SD13	Data setup time	tDS	2.0	—	ns
SD14	Data hold time	tDH	1.3	—	ns

1 SD11 and SD12 are determined by SDRAM controller register settings.

NOTE

SDR SDRAM CLK parameters are being measured from the 50% point—that is, high is defined as 50% of signal value and low is defined as 50% of signal value.

NOTE

The timing parameters are similar to the ones used in SDRAM data sheets—that is, Table 32 indicates SDRAM requirements. All output signals are driven by the ESDCTL at the negative edge of SDCLK and the parameters are measured at maximum memory frequency.

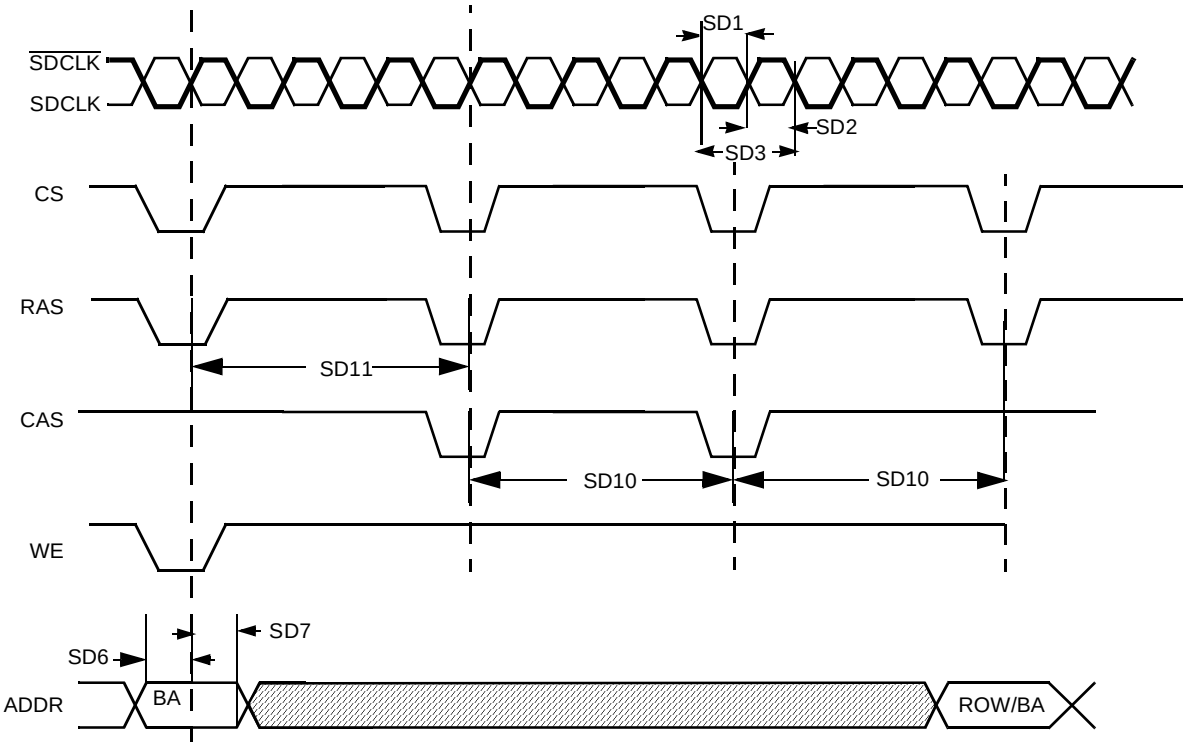


Figure 35. SDRAM Refresh Timing Diagram

Table 33. SDRAM Refresh Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
SD1	SDRAM clock high-level width	tCH	3.4	4.1	ns
SD2	SDRAM clock low-level width	tCL	3.4	4.1	ns
SD3	SDRAM clock cycle time	tCK	7.5	—	ns
SD6	Address setup time	tAS	1.8	—	ns
SD7	Address hold time	tAH	1.8	—	ns
SD10	Precharge cycle period[1]	tRP	1	4	clock
SD11	Auto precharge command period[1]	tRC	2	20	clock

1 SD10 and SD11 are determined by SDRAM controller register settings.

NOTE

SDR SDRAM CLK parameters are being measured from the 50% point—that is, high is defined as 50% of signal value and low is defined as 50% of signal value.

NOTE

The timing parameters are similar to the ones used in SDRAM data sheets—that is, Table 33 indicates SDRAM requirements. All output signals are driven by the ESDCTL at the negative edge of SDCLK and the parameters are measured at maximum memory frequency.

4.3.14 IPU—Sensor Interfaces

4.3.14.1 Supported Camera Sensors

Table 41 lists the known supported camera sensors at the time of publication.

Table 41. Supported Camera Sensors[1]

Vendor	Model
Conexant	CX11646, CX20490[2], CX20450[2]
Agilant	HDCP–2010, ADCS–1021[2], ADCS–1021[2]
Toshiba	TC90A70
ICMedia	ICM202A, ICM102[2]
iMagic	IM8801
Transchip	TC5600, TC5600J, TC5640, TC5700, TC6000
Fujitsu	MB86S02A
Micron	MI–SOC–0133
Matsushita	MN39980
STMicro	W6411, W6500, W6501[2], W6600[2], W6552[2], STV0974[2]
OmniVision	OV7620, OV6630
Sharp	LZ0P3714 (CCD)
Motorola	MC30300 (Python)[2], SCM20014[2], SCM20114[2], SCM22114[2], SCM20027[2]
National Semiconductor	LM9618[2]

1 Freescale Semiconductor does not recommend one supplier over another and in no way suggests that these are the only camera suppliers.

2 These sensors not validated at time of publication.

4.3.14.2 Functional Description

There are three timing modes supported by the IPU.

4.3.14.2.1 Pseudo BT.656 Video Mode

Smart camera sensors, which include imaging processing, usually support video mode transfer. They use an embedded timing syntax to replace the SENSB_VSYNC and SENSB_HSYNC signals. The timing syntax is defined by the BT.656 standard.

This operation mode follows the recommendations of ITU BT.656 specifications. The only control signal used is SENSB_PIX_CLK. Start-of-frame and active-line signals are embedded in the data stream. An active line starts with a SAV code and ends with a EAV code. In some cases, digital blanking is inserted in between EAV and SAV code. The CSI decodes and filters out the timing-coding from the data stream, thus recovering SENSB_VSYNC and SENSB_HSYNC signals for internal use.

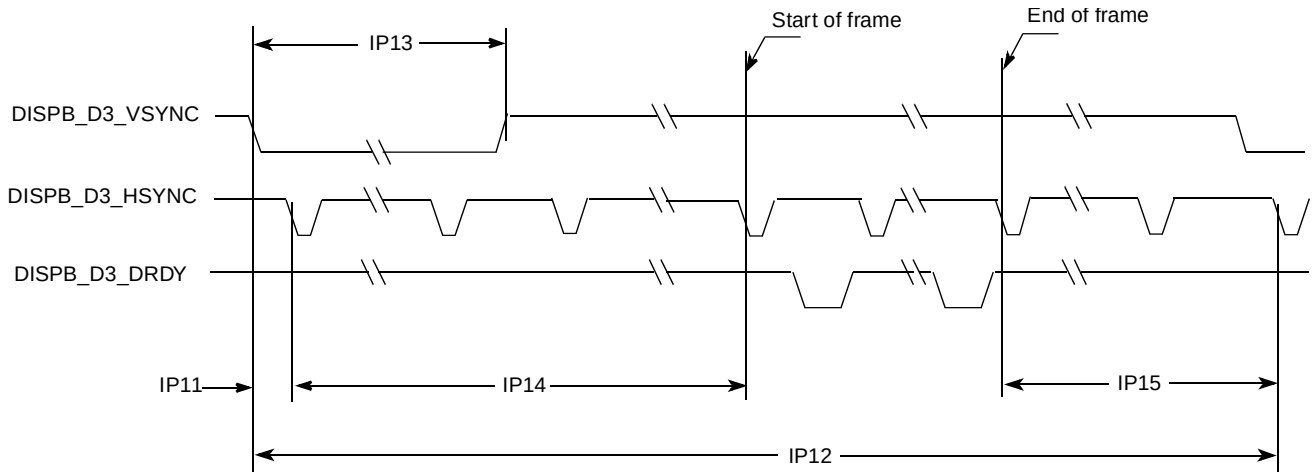


Figure 47. TFT Panels Timing Diagram—Vertical Sync Pulse

Table 44 shows timing parameters of signals presented in Figure 46 and Figure 47.

Table 44. Synchronous Display Interface Timing Parameters—Pixel Level

ID	Parameter	Symbol	Value	Units
IP5	Display interface clock period	Tdicp	Tdicp[1]	ns
IP6	Display pixel clock period	Tdpcp	(DISP3_IF_CLK_CNT_D+1) * Tdicp	ns
IP7	Screen width	Tsw	(SCREEN_WIDTH+1) * Tdpcp	ns
IP8	HSYNC width	Thsw	(H_SYNC_WIDTH+1) * Tdpcp	ns
IP9	Horizontal blank interval 1	Thbi1	BGXP * Tdpcp	ns
IP10	Horizontal blank interval 2	Thbi2	(SCREEN_WIDTH – BGXP – FW) * Tdpcp	ns
IP11	HSYNC delay	Thsd	H_SYNC_DELAY * Tdpcp	ns
IP12	Screen height	Tsh	(SCREEN_HEIGHT+1) * Tsw	ns
IP13	VSYNC width	Tvsw	if V_SYNC_WIDTH_L = 0 than (V_SYNC_WIDTH+1) * Tdpcp else (V_SYNC_WIDTH+1) * Tsw	ns
IP14	Vertical blank interval 1	Tvbi1	BGYP * Tsw	ns
IP15	Vertical blank interval 2	Tvbi2	(SCREEN_HEIGHT – BGYP – FH) * Tsw	ns

1 Display interface clock period immediate value.

$$Tdicp = \begin{cases} T_{HSP\_CLK} \cdot \frac{DISP3\_IF\_CLK\_PER\_WR}{HSP\_CLK\_PERIOD}, & \text{for integer } \frac{DISP3\_IF\_CLK\_PER\_WR}{HSP\_CLK\_PERIOD} \\ T_{HSP\_CLK} \cdot \left(floor\left[\frac{DISP3\_IF\_CLK\_PER\_WR}{HSP\_CLK\_PERIOD} \right] + 0.5 \pm 0.5 \right), & \text{for fractional } \frac{DISP3\_IF\_CLK\_PER\_WR}{HSP\_CLK\_PERIOD} \end{cases}$$

Display interface clock period average value.

$$\overline{T}dicp = T_{HSP\_CLK} \cdot \frac{DISP3\_IF\_CLK\_PER\_WR}{HSP\_CLK\_PERIOD}$$

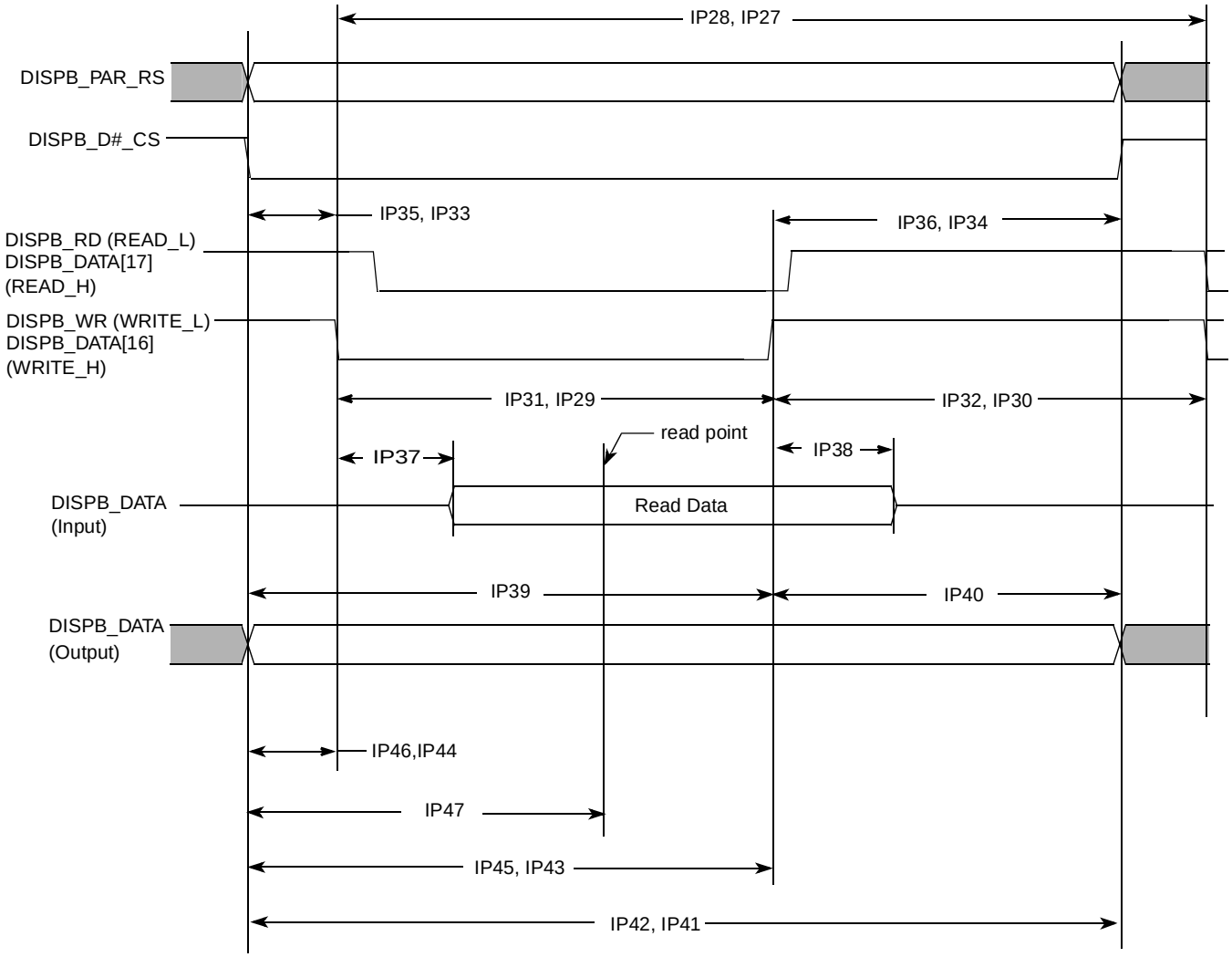


Figure 57. Asynchronous Parallel System 80 Interface (Type 2) Timing Diagram

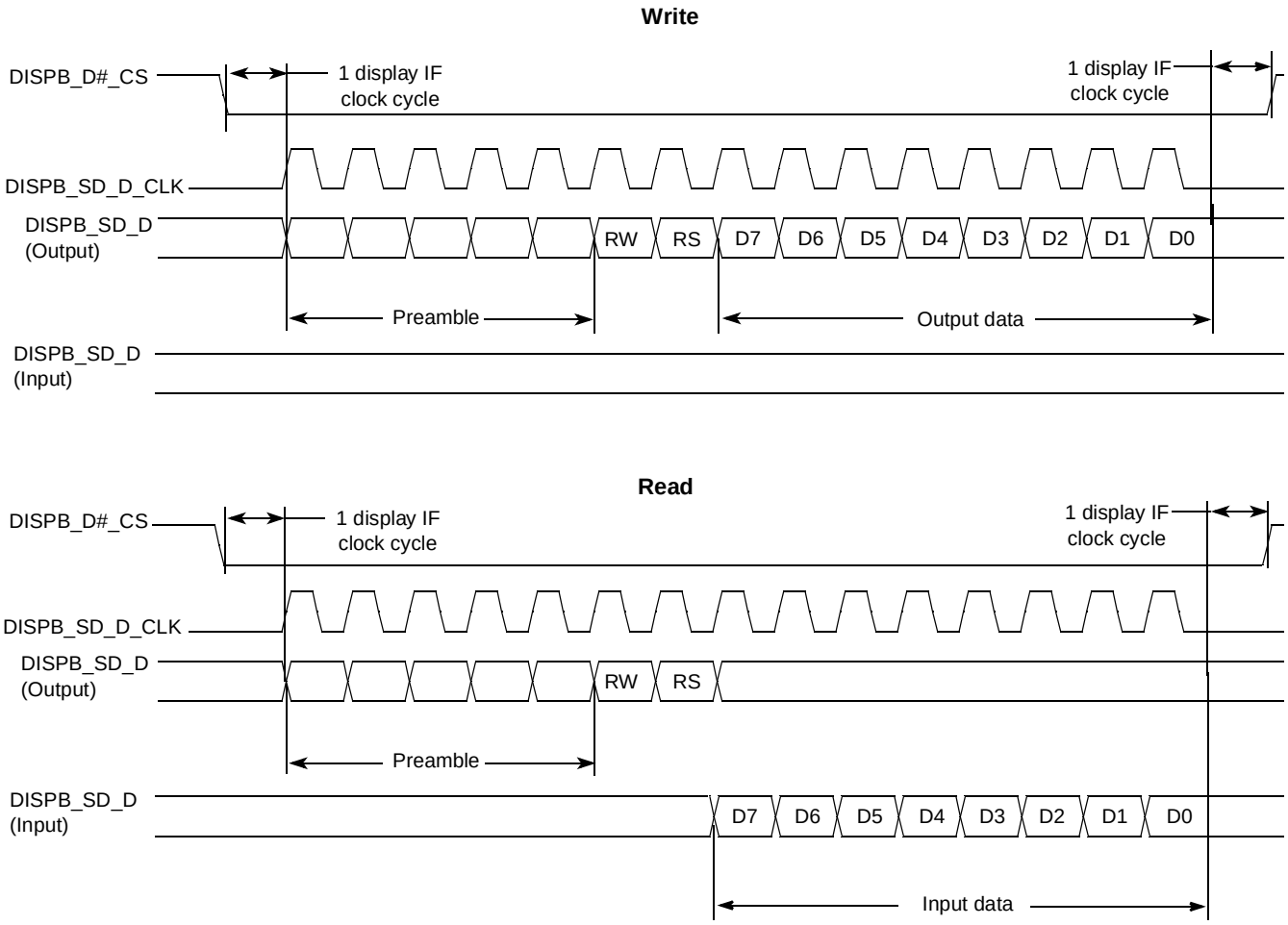


Figure 61. 4-Wire Serial Interface Timing Diagram

Figure 62 depicts timing of the 5-wire serial interface (Type 1). For this interface, a separate RS line is added. When a burst is transmitted within single active chip select interval, the RS can be changed at boundaries of words.

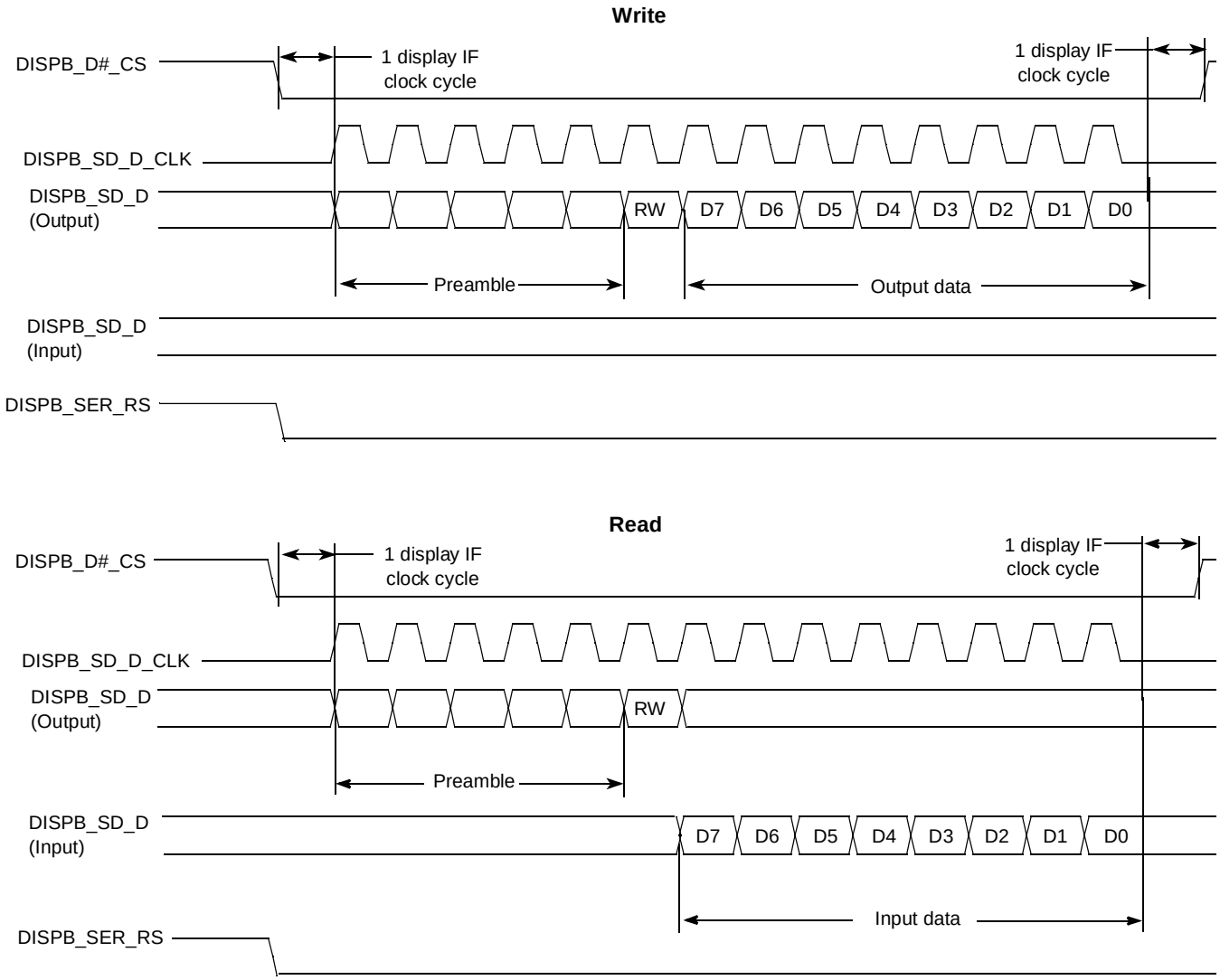


Figure 62. 5-Wire Serial Interface (Type 1) Timing Diagram

Table 48. Asynchronous Serial Interface Timing Parameters—Access Level (continued)

ID	Parameter	Symbol	Min.	Typ.[1]	Max.	Units
IP56	Controls setup time for write	Tdcsw	Tdicuw–1.5	Tdicuw	—	ns
IP57	Controls hold time for write	Tdchw	Tdicpw–Tdicdw–1.5	Tdicpw–Tdicdw	—	ns
IP58	Slave device data delay[8]	Tracc	0	—	Tdrp[9]–Tlbd[10]–Tdicur–1.5	ns
IP59	Slave device data hold time[8]	Troh	Tdrp–Tlbd–Tdicdr+1.5	—	Tdicpr–Tdicdr–1.5	ns
IP60	Write data setup time	Tds	Tdicdw–1.5	Tdicdw	—	ns
IP61	Write data hold time	Tdh	Tdicpw–Tdicdw–1.5	Tdicpw–Tdicdw	—	ns
IP62	Read period[2]	Tdicpr	Tdicpr–1.5	Tdicpr	Tdicpr+1.5	ns
IP63	Write period[3]	Tdicpw	Tdicpw–1.5	Tdicpw	Tdicpw+1.5	ns
IP64	Read down time[4]	Tdicdr	Tdicdr–1.5	Tdicdr	Tdicdr+1.5	ns
IP65	Read up time[5]	Tdicur	Tdicur–1.5	Tdicur	Tdicur+1.5	ns
IP66	Write down time[6]	Tdicdw	Tdicdw–1.5	Tdicdw	Tdicdw+1.5	ns
IP67	Write up time[7]	Tdicuw	Tdicuw–1.5	Tdicuw	Tdicuw+1.5	ns
IP68	Read time point[9]	Tdrp	Tdrp–1.5	Tdrp	Tdrp+1.5	ns

1 The exact conditions have not been finalized, but will likely match the current customer requirement for their specific display. These conditions may be device specific.

2 Display interface clock period value for read:

$$Tdicpr = T_{HSP\_CLK} \cdot ceil\left[\frac{DISP\#\_IF\_CLK\_PER\_RD}{HSP\_CLK\_PERIOD}\right]$$

3 Display interface clock period value for write:

$$Tdicpw = T_{HSP\_CLK} \cdot ceil\left[\frac{DISP\#\_IF\_CLK\_PER\_WR}{HSP\_CLK\_PERIOD}\right]$$

4 Display interface clock down time for read:

$$Tdicdr = \frac{1}{2}T_{HSP\_CLK} \cdot ceil\left[\frac{2 \cdot DISP\#\_IF\_CLK\_DOWN\_RD}{HSP\_CLK\_PERIOD}\right]$$

5 Display interface clock up time for read:

$$Tdicur = \frac{1}{2}T_{HSP\_CLK} \cdot ceil\left[\frac{2 \cdot DISP\#\_IF\_CLK\_UP\_RD}{HSP\_CLK\_PERIOD}\right]$$

6 Display interface clock down time for write:

$$Tdicdw = \frac{1}{2}T_{HSP\_CLK} \cdot ceil\left[\frac{2 \cdot DISP\#\_IF\_CLK\_DOWN\_WR}{HSP\_CLK\_PERIOD}\right]$$

7 Display interface clock up time for write:

$$Tdicuw = \frac{1}{2}T_{HSP\_CLK} \cdot ceil\left[\frac{2 \cdot DISP\#\_IF\_CLK\_UP\_WR}{HSP\_CLK\_PERIOD}\right]$$

8 This parameter is a requirement to the display connected to the IPU.

9 Data read point:

$$Tdrp = T_{HSP\_CLK} \cdot ceil\left[\frac{DISP\#\_READ\_EN}{HSP\_CLK\_PERIOD}\right]$$

10 Loopback delay Tlbd is the cumulative propagation delay of read controls and read data. It includes an IPU output delay, a device-level output delay, board delays, a device-level input delay, an IPU input delay. This value is device specific.

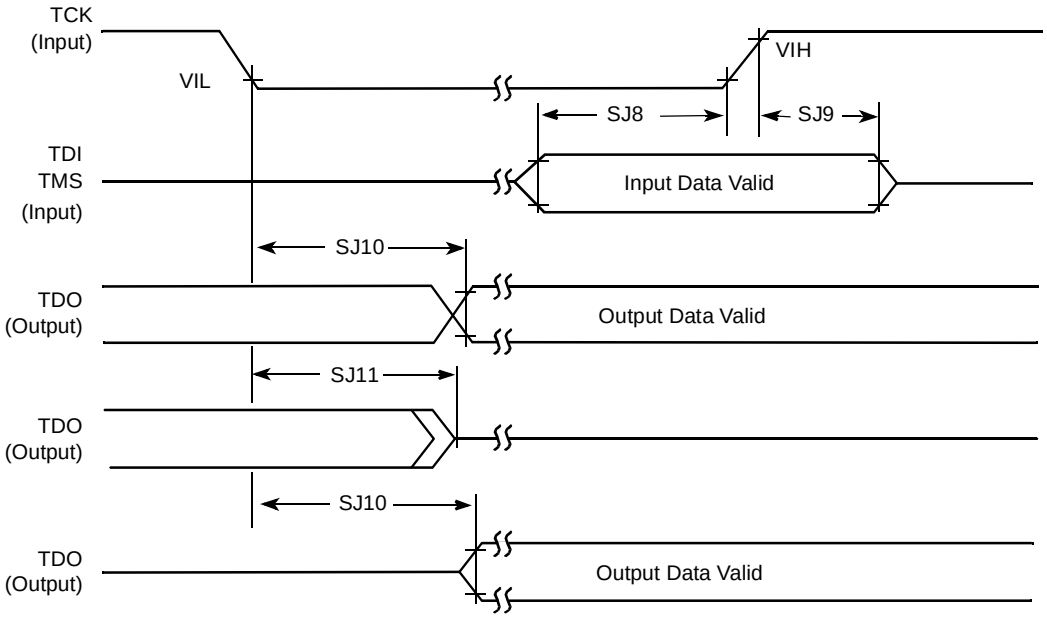


Figure 78. Test Access Port Timing Diagram

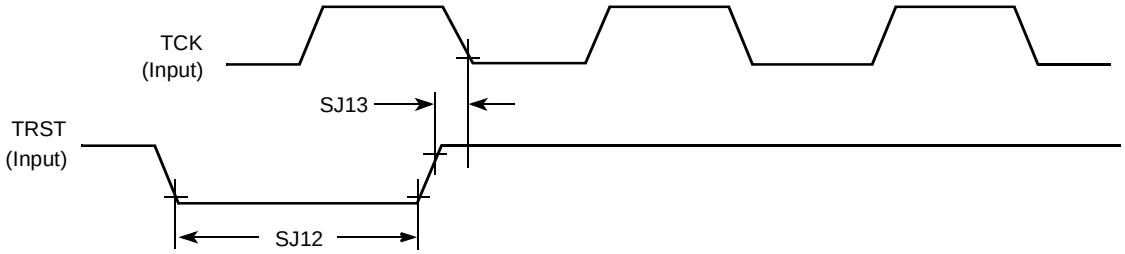
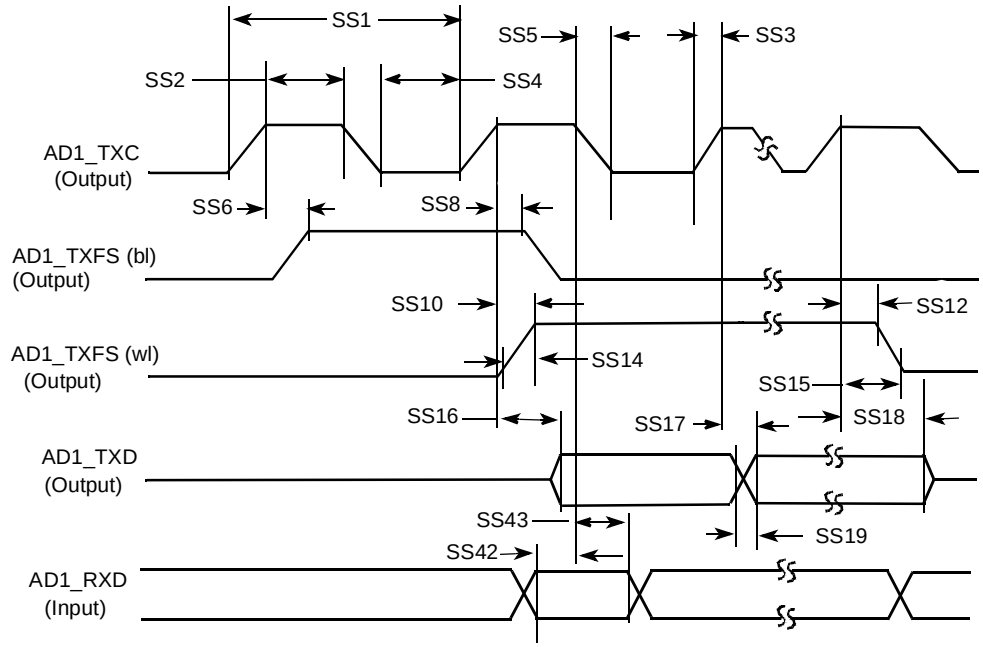


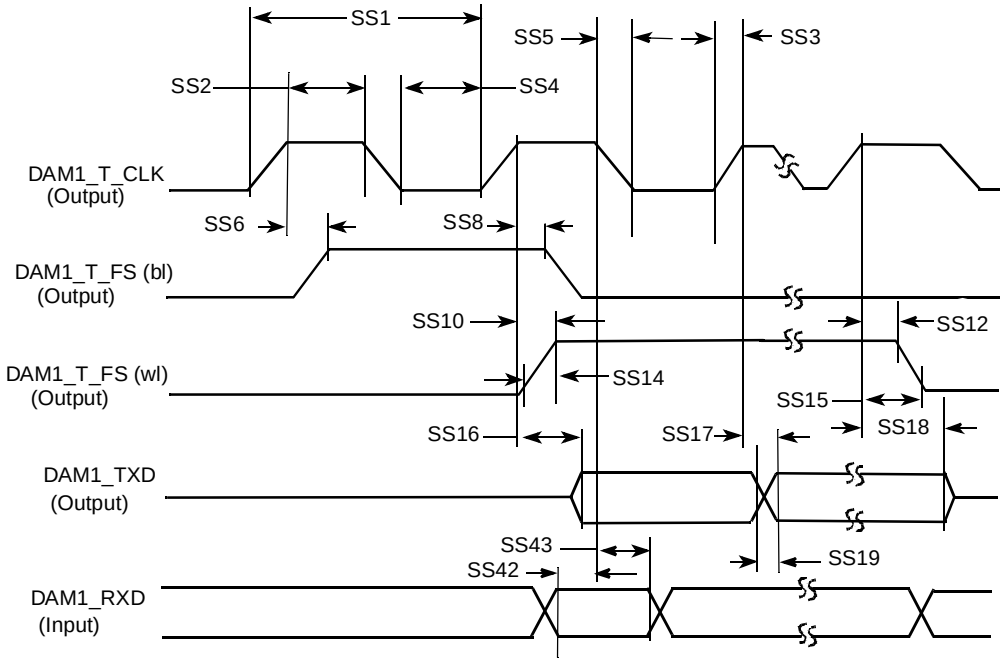
Figure 79. $\overline{\text{TRST}}$ Timing Diagram

Table 56. SJC Timing Parameters

ID	Parameter	All Frequencies		Unit
		Min	Max	
SJ1	TCK cycle time	100[1]	—	ns
SJ2	TCK clock pulse width measured at V_M[2]	40	—	ns
SJ3	TCK rise and fall times	—	3	ns
SJ4	Boundary scan input data set-up time	10	—	ns
SJ5	Boundary scan input data hold time	50	—	ns
SJ6	TCK low to output data valid	—	50	ns
SJ7	TCK low to output high impedance	—	50	ns
SJ8	TMS, TDI data set-up time	10	—	ns
SJ9	TMS, TDI data hold time	50	—	ns
SJ10	TCK low to TDO data valid	—	44	ns



Note: SRXD Input in Synchronous mode only



Note: SRXD Input in Synchronous mode only

Figure 80. SSI Transmitter with Internal Clock Timing Diagram

Table 64. 19 x 19 BGA Signal ID by Ball Grid Location (continued)

Signal ID	Ball Location
RXD1	C9
RXD2	A12
SCK3	P1
SCK4	G6
SCK5	D4
SDCKE0	Y17
SDCKE1	V16
SDCLK	AC20
$\overline{\text{SDCLK}}$	AC19
SDQS0	AB16
SDQS1	AB12
SDQS2	AB9
SDQS3	AB6
SDWE	AB20
SER_RS	P23
SFS3	P2
SFS4	D3
SFS5	G7
SFS6	P4
SIMPD0	B18
SJC_MOD	C17
SRST0	C18
SRX0	A19
SRXD3	N3
SRXD4	C3
SRXD5	C4
SRXD6	R1
STX0	F16
STXD3	N4
STXD4	B3
STXD5	D1
STXD6	P3
SVEN0	D17
TCK	F14
TDI	A18
TDO	B17
TMS	C16

Signal ID	Ball Location
SD7	AB15
SD8	AC15
SD9	AA14
SDBA0	AA6
SDBA1	Y7
TRSTB	F15
TXD1	D9
TXD2	F11
USB_BYP	C8
USB_OC	B8
USB_PWR	A8
USBH2_CLK	L1
USBH2_DATA0	M6
USBH2_DATA1	K1
USBH2_DIR	L2
USBH2_NXT	L4
USBH2_STP	L3
USBOTG_CLK	D8
USBOTG_DATA0	G8
USBOTG_DATA1	C7
USBOTG_DATA2	A6
USBOTG_DATA3	F8
USBOTG_DATA4	D7
USBOTG_DATA5	B6
USBOTG_DATA6	A5
USBOTG_DATA7	C6
USBOTG_DIR	A7
USBOTG_NXT	B7
USBOTG_STP	F9
VPG0	G21
VPG1	G22
VSTBY	H18
VSYNC0	L22
VSYNC3	N20
WATCHDOG_RST	B21
WRITE	N22

6 Product Documentation

This Data Sheet is labeled as a particular type: Product Preview, Advance Information, or Technical Data. Definitions of these types are available at: http://www.freescale.com.

- *MCIMX31 Product Brief* (order number MCIMX31PB)
- *MCIMX31 Reference Manual* (order number MCIMX31RM)